YAO WANG

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EDUCATION

Cornell University, Ithaca, NY

Ph.D. candidate, Computer Engineering, minor in Computer Science — expected May 2016
CUMULATIVE GPA: 3.86/4.00 — advisor: G. Edward Suh

Select coursework: computer architecture, parallel computer architecture, memory systems, digital VLSI, operating system, advanced microprocessor architecture, system security, introduction to compilers

Tsinghua University, Beijing, China

B.S. degree in Electronic Engineering — June 2010
CUMULATIVE GPA: 91/100 — research advisor: Yu Wang

PUBLICATIONS

Danfeng Zhang, **Yao Wang**, Edward G. Suh, Andrew C. Myers, "A Hardware Design Language for Timing-Sensitive Information-Flow Security", To appear: 20th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS 2015), March 2015.

Yao Wang, Andrew Ferraiuolo, G. Edward Suh, "Timing Channel Protection for a Shared Memory Controller", Proceedings of the 20th International Symposium on High Performance Computer Architecture (HPCA 2014), February 2014.

Nithin Michael, **Yao Wang**, Edward G. Suh, Ao Tang, "Quadrisection-Based Task Mapping on Many-Core Processors for Energy-Efficient On-Chip Communication", Proceedings of the 7th ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2013), April 2013.

Yao Wang, Edward G. Suh, "Efficient Timing Channel Protection for On-chip Networks", Proceedings of the 6th ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2012), May 2012.

Yao Wang, Yu Wang, Jiang Xu, Huazhong Yang, "Performance Evaluation of On-Chip Sensor Network (SENoC) in MPSoC", in International Conference on Green Circuits and Systems (ICGCS 2010), June 2010.

SELECTED RESEARCH PROJECTS

Software-Hardware Combined Approach to Control Information Flow

- Control information flow through the cooperation between software and hardware
- Software provides annotations to control information flow and hardware enforces the software annotations
- Developed a hardware design language SecVerilog based on Verilog that can track information flow
- Designed a secure microprocessor using SecVerilog
- **Publications: ASPLOS'15**

Full System Timing Channel Protection

- Proposed Timing Compartments as a hardware abstraction to control timing channels
- Added timing channel protection for critical system components (cache, on-chip network, memory controller)
- Identified new timing channel threats through the component interfaces and cache coherence protocols
- Showed the importance of coordinating the timing channel protections for different components
- **Publications: under submission**

Timing Channel Protection for Memory Controllers

- Demonstrated the existence of timing channels in a shared memory controller
- Modified the queueing structure of memory controllers to avoid interference
- Used TDM-based scheduling algorithm, added dead time to drain memory requests
- **Publications: HPCA'14**

Energy-Efficient Task Mapping Algorithm for Many-Core Processors

- Map streaming tasks on many-core processors to reduce the total communication power (NP hard)

- Applied a heuristic VLSI layout methodology called Quardrisection to the task mapping problem
- **Publications: NOCS'13**

Efficient Timing Channel Protection for On-Chip Networks

- Showed the timing channel problem for on-chip networks
- Proposed an efficient timing channel protection mechanism using one-way protection that prevents information flow from high security level to low security level
- **Publication: NOCS'12**

Power-Efficient Routing Algorithm for On-Chip Networks

- Proposed a routing algorithm called "backtrack" that can maximize the number of unused routers which can then be turned off to save power
- The proposed routing algorithm is deadlock free and incurs little to no performance overhead

ACADEMIC HONORS

- Cornell University Fellowship Sep 2010
- Outstanding Graduate Award, Tsinghua University May 2010
- Guanghua Scholarship, Tsinghua University May 2009
- Huangqianxiang Scholarship, Tsinghua University May 2008
- National Scholarship, Tsinghua University May 2007

PROFESSIONAL ACTIVITIES

- Reviewers for HPCA2014, CCS2014 2014
- Teaching Assistant, ENGRD 2300 Fall 2012
- Registration Assistant for ISA2012 June 2012
- Student Member in IEEE

TECHNICAL SKILLS

- Relevant software: Gem5, DRAMSim2, SimpleScalar, MARSSx86, Orion, Darsim, McSim, Quartus
- Programming: C/C++, VHDL/Verilog, Python, Java, Ruby, Matlab, HTML