XIAODONG WANG

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Research Interests

- Scalable resource management in chip-multiprocessors
- Architecture-aware system design
- Memory systems

Education

Ph.D. candidate, School of Electrical and Computer Engineering 08/2011-present
Cornell University Ithaca, NY, USA

- Cumulative GPA: 4.07/4.0
- Advisor: José F. Martínez

Exchange student, School of Electrical and Computer Engineering 08/2010-12/2010
Georgia Institute of Technology Atlanta, GA, USA

- Cumulative GPA: 4.00/4.0
- Research Advisor: Hsien-Hsin S. Lee

B.S., Department of Electronic Engineering, 2011 09/2007-06/2011
Shanghai Jiao Tong University Shanghai, P.R. China

- Major GPA: 94.05/100 Cumulative GPA: 90.51/100
- Rank: 1st/78

Honors and Awards

- Cavium ThunderX Trophy Award, 2015-2016
- Best Paper Finalist, HPCA 2015
- Cavium OCTEON Trophy Winner, 2014
- McMullen Fellowship, Cornell University, 2011
- National Scholarship, Ministry of Education of P.R. China, 2008, 2009, 2010 (top 3%)
- First Prize, Excellent Academic Scholarship, Shanghai Jiao Tong University, 2009, 2010 (top 1%)

Research Experience

Research Assistant, M3 Architecture Research Group 08/2011-present
Cornell University Ithaca, NY, USA

Topic: Market-based Resource Allocation in Chip Multiprocessor (CMP) [**p2**][**p3**]

- Investigate the scalability challenge of resource management in future large-scale CMP systems
- Design a predictive model to accurately characterize the resource demand of applications
- Establish a largely distributed market in CMP to allocated resources among the cores
- Develop a technique to trade off system efficiency and fairness to meet different system targets

Topic: Scalable Cache Management in Chip Multiprocessor (CMP) [**p1**]

- Propose a hardware and software co-design to manage shared cache in large-scale CMPs
- Evaluate the proposal in ThunderX™ 48-core CMP running Linux
- Guarantee QoS of online cloud applications while maximizing the throughput of batch workloads

Summer Internship, Architecture Group 05/2015-08/2015
Cavium Networks San Jose, CA, USA
Topic: Scalable Cache Management in ThunderX^{TM} 48-core chip

- Developed a tool to monitor and analyze the dynamic cache behavior of SPEC applications
- Investigated biased cache allocation technique to improve SPECrate in ThunderX
- Proposed a novel cache replacement policy for the next generation processor

Research Assistant, Microprocessor Architecture Research Society (MARS) 08/2010-12/2010
Georgia Institute of Technology Atlanta, GA, USA
Topic: Memory Built-in Self-Repair (BISR) for 3D Memories [**p4**]

- Improved the current 2D BISR algorithm and fault model for 3D memory
- Parallelized the built-in self-test (BIST) of 3D memory in each memory layer
- Designed a novel 3D redundancy structure

Summer Internship, School of Microelectronics 07/2010-08/2010
Shanghai Jiao Tong University Shanghai, P.R. China
Topic: Programming and Optimization for Reconfigurable Systems

- Participated in designing a SOC system with ARM9 and reconfigurable computing array (RCA)
- Programmed and configured RCA to run DCT/IDCT algorithm
- Optimized memory system for efficient configuration and data transfer of RCA

Publications

[p1] **Xiaodong Wang**, Shuang Chen, Jeff Setter, and José F. Martínez,
″SWAP: Effective Fine-Grain Management of Shared Last-Level Caches with Minimum Hardware Support″
To appear in *Intl. Symp. on High-Performance Computer Architecture (HPCA),* Austin, TX, Feb. 2017.

[p2] **Xiaodong Wang** and José F. Martínez,
″ReBudget: Trading off efficiency vs. fairness in market-based multicore resource allocation via runtime budget reassignment″
In *Intl. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS),* Atlanta, GA, Apr. 2016.

[p3] **Xiaodong Wang** and José F. Martínez,
″XChange: Scalable Dynamic Multi-Resource Allocation in Multicore Architectures″
In *Intl. Symp. on High-Performance Computer Architecture (HPCA),* Bay Area, CA, Feb. 2015.
(best paper session)

[p4] **Xiaodong Wang**, Dilip Vasudevan, and Hsien-Hsin S. Lee
″Global Built-In Self-Repair for 3-D Memories with Redundancy Sharing and Parallel Testing″
In *IEEE Intl. Conf. on 3D System Integration,* Osaka, Japan, 2012

Teaching Experience

Teaching Assistant, Cornell University Ithaca, NY, USA

- CS4410 Operating Systems (Fall 2014)
- ECE3140 Embedded Systems (Spring 2013, Spring 2016)
- ECE2300 Digital Logic and Computer Organization (Fall 2016)

Technical Knowledge

- Simulator: SESC, Gem5
- Programming Language: C/C++, Python
- Hardware Description Language: VHDL, Verilog, Vivado HLS