# FPGA Design of Low-Complexity Joint Channel Estimation and Data Detection for Large SIMO Wireless Systems

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Abstract-Joint channel estimation and data detection (JED) enables near-optimal error-rate performance in realistic wireless communication systems that suffer from channel estimation errors. In this paper, we propose a new JED algorithm and a corresponding FPGA design for large single-input multiple-output (SIMO) wireless systems that use constantmodulus constellations. Our algorithm, referred to as PrOX (short for PRojection Onto conveX hull), relies on biconvex relaxation (BCR) in order to efficiently compute an approximate solution of the maximumlikelihood JED problem that exhibits prohibitive complexity. PrOX is a simple and hardware-friendly algorithm that achieves near-optimal error-rate performance for a wide-range of system configurations. To demonstrate the efficacy of PrOX, we develop a scalable VLSI architecture and present reference implementation results on a Xilinx Virtex-7 FPGA. Compared to a recently-reported reference JED design, PrOX achieves  $3 \times$  higher throughput,  $20 \times$  better hardware-efficiency (in terms of throughput per look-up tables), and  $8 \times$  improved energy-efficiency.

#### I. INTRODUCTION

Large wireless systems, in which the base-station (BS) is equipped with hundreds or thousands of antenna elements, have recently gained significant attention. The large number of BS antennas enables fine-grained beamforming and improved spectral-efficiency within each cell compared to traditional, small scale single-input multipleoutput (SIMO) and multiple-input multiple-output (MIMO) wireless systems [1], [2]. Pilot contamination is known to be a limiting factor in such large wireless systems, i.e., channel training is contaminated by pilot or data transmission of users communicating in adjacent cells [3]. To mitigate the effects of pilot contamination, one can rely on joint channel estimation and data detection (JED), which is capable of approaching the performance of idealistic systems with perfect channel-state information [4], [5]. While a few JED algorithms have been proposed for traditional, small-scale SIMO and MIMO wireless systems [4]-[7], their complexity is typically very high and not much is known about their efficacy for systems with hundreds or thousands of antennas. Moreover, with the exception of the VLSI design in [8], no hardware designs for JED have been described in the literature.

#### A. Contributions

We develop a novel JED algorithm and a VLSI design for large SIMO wireless systems that use constant-modulus constellations. Our algorithm, referred to as PrOX (short for PRojection Onto conveX hull), relies on the biconvex relaxation (BCR) framework [9], a general method for computing approximate solutions to semidefinite problems at low complexity. PrOX solves the biconvex problem that arises after relaxing and regularizing the optimal maximum-likelihood (ML) JED problem, enabling near ML-JED performance at low complexity. We develop a scalable VLSI architecture for PrOX that achieves highthroughput and low implementation complexity. We show reference implementation results on a Xilinx Virtex-7 FPGA and compare our solution to the recently-reported JED design in [8].

#### B. Notation

Lowercase and uppercase boldface letters stand for column vectors and matrices, respectively. For the matrix **A**, the Hermitian is  $\mathbf{A}^H$ and the *k*th row and  $\ell$ th column entry is  $A_{k,\ell}$ . For the vector **a**, the *k*th entry is  $a_k$ . The Euclidean norm of **a** and the Frobenius norm of **A** are  $\|\mathbf{a}\|_2$  and  $\|\mathbf{A}\|_F$ , respectively. The real and imaginary parts of the vector **a** are  $\Re(\mathbf{a})$  and  $\Im(\mathbf{a})$ , respectively.

## II. SYSTEM MODEL AND ML-OPTIMAL JED

## A. Large SIMO System Model

We consider a large SIMO wireless uplink system in which a singleantenna user transmits data over K + 1 time slots to B BS antennas. We model the input-output relation of a narrow-band, flat-fading wireless channel as follows [4]–[6]:  $\mathbf{Y} = \mathbf{hs}^{H} + \mathbf{N}$ . Here, the matrix  $\mathbf{Y} \in \mathbb{C}^{B \times (K+1)}$  contains the B-dimensional receive vectors for the K + 1 time slots,  $\mathbf{h} \in \mathbb{C}^{B}$  is the unknown SIMO channel vector (assumed block fading over K+1 time slots),  $\mathbf{s} \in \mathcal{O}^{K+1}$  contains the transmitted data symbols for all K+1 time slots, and  $\mathbf{N} \in \mathbb{C}^{B \times (K+1)}$ is i.i.d. complex circularly-symmetric Gaussian noise with variance  $N_0$ per entry. We assume constant-modulus constellations for the set  $\mathcal{O}$ .

#### B. Joint Channel Estimation and Data Detection (JED)

Let **h** be a deterministic, but unknown, channel vector with unknown statistics. Then, we have the following ML-JED problem [6]:

$$\left\{\hat{\mathbf{s}}^{\text{JED}}, \hat{\mathbf{h}}\right\} = \underset{\mathbf{s}\in\mathcal{O}^{K+1}, \, \mathbf{h}\in\mathbb{C}^{B}}{\arg\min} \left\|\mathbf{Y} - \mathbf{hs}^{H}\right\|_{F}.$$
 (1)

Note that, if  $\hat{\mathbf{s}}^{\text{JED}} e^{j\phi} \in \mathcal{O}^{K+1}$  for  $\phi \in [0, 2\pi)$ , then  $\hat{\mathbf{h}} e^{j\phi}$  is also a solution to (1). To avoid this ambiguity, we set the first entry of the transmit vector to  $\check{s} \in \mathcal{O}$  and exploit this knowledge at the receiver.<sup>1</sup>

Since we assumed the entries in s to be constant-modulus, the ML-JED estimate for the transmit vector can be written as [6]:

$$\mathbf{\hat{s}}^{\text{JED}} = \underset{\mathbf{s}\in\mathcal{O}^{K+1}}{\arg\max} \|\mathbf{Y}\mathbf{s}\|_2.$$
(2)

This problem resembles the famous MaxCut problem that is known to be NP-hard [10]. For a small number of time slots K + 1, the problem in (2) can be solved exactly at low average complexity using sphere decoding (SD) methods [6]. For a large number of time slots, however, SD entails prohibitive complexity. Moreover, linear methods (which are widely used for coherent data detection in MIMO systems) are not useful for this case, since the entries of s grow unbounded when relaxing the constraint  $s \in O^{K+1}$  to  $s \in \mathbb{C}^{K+1}$ . To enable JED

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<sup>&</sup>lt;sup>1</sup>This approach differs from traditional, pilot-based schemes as all transmitted symbols are used to improve the channel estimate, which significantly improves the error-rate performance (see Section V for simulation results).

for SIMO systems with a large number of time slots, the design of novel, low-complexity algorithms is necessary. Recently, an algorithm and VLSI design that relies on semidefinite relaxation (SDR) was reported in [8]. We next propose a simpler and faster method to compute approximate solutions to the ML-JED problem in (2).

#### III. PROX: PROJECTION ONTO CONVEX HULL

# A. Biconvex Relaxation (BCR) of the ML-JED Problem

We start by reformulating the ML-JED problem in (2) using BCR [9]. We first include a regularization term that forces the transmit vector  $\mathbf{s} \in \mathcal{O}^{K+1}$  to be close to a copy  $\mathbf{q} \in \mathbb{C}^{K+1}$  as follows:

$$\underset{\mathbf{s}\in\mathcal{O}^{K+1},\mathbf{q}\in\mathbb{C}^{K+1}}{\arg\min} - \|\mathbf{Y}\mathbf{q}\|_{2}^{2} + \alpha\|\mathbf{q} - \mathbf{s}\|_{2}^{2},$$
(3)

where  $\alpha$  is a suitably chosen regularization parameter. To ensure that the problem in (3) is convex in  $\mathbf{q}$ ,  $\alpha$  must be larger than the maximum singular value of the Gram matrix  $\mathbf{G} = \mathbf{Y}^H \mathbf{Y}$ . We next relax the finite-alphabet constraint to the convex hull  $\mathcal{C}_{\mathcal{O}}$  of the set  $\mathcal{O}$  [11]

$$\mathcal{C}_{\mathcal{O}} = \left\{ \sum_{i=1}^{|\mathcal{O}|} \alpha_i s_i \, | \, (\alpha_i \in \mathbb{R}^+, \forall i) \land \sum_{i=1}^{|\mathcal{O}|} \alpha_i = 1 \right\},\,$$

with  $s_i$ ,  $i = 1, ..., |\mathcal{O}|$ , being the constellation points in  $\mathcal{O}$ . The convex hull of the BPSK constellation set  $C_{\text{BPSK}}$  is the line along the real axis in [-1, +1]; the convex hull  $C_{\text{QPSK}}$  for QPSK is the square with the four constellation points as corners. By relaxing  $\mathcal{O}$  to  $C_{\mathcal{O}}$ , we arrive at the following relaxed ML-JED problem:

$$\underset{\in \mathcal{C}_{\mathcal{O}}^{K+1}, \mathbf{q} \in \mathbb{C}^{K+1}}{\arg \min} - \|\mathbf{Y}\mathbf{q}\|_{2}^{2} + \alpha \|\mathbf{q} - \mathbf{s}\|_{2}^{2}$$

Finally, we include a norm constraint that promotes large values in s, with the goal of forcing the entries of s to the boundary of the convex hull. This leads to the final BCR formulation:

$$\hat{\mathbf{s}}^{\text{BCR}} = \underset{\mathbf{s} \in \mathcal{C}_{\mathcal{O}}^{K+1}, \mathbf{q} \in \mathbb{C}^{K+1}}{\arg \min} - \|\mathbf{Y}\mathbf{q}\|_{2}^{2} + \alpha \|\mathbf{q} - \mathbf{s}\|_{2}^{2} - \beta \|\mathbf{s}\|_{2}^{2}, \quad (4)$$

where  $\beta < \alpha$  is a suitably chosen algorithm parameter.

# B. Alternating Optimization

We solve the BCR problem in (4) using alternating minimization, in which we keep one of the variables fixed while solving for the other. The resulting iterative algorithm is given by

$$\mathbf{q}^{(t)} = \underset{\mathbf{q} \in \mathbb{C}^{K+1}}{\arg\min} - \|\mathbf{Y}\mathbf{q}\|_2^2 + \alpha \|\mathbf{q} - \mathbf{s}^{(t-1)}\|_2^2$$
$$\mathbf{s}^{(t)} = \underset{\mathbf{s} \in \mathcal{C}^{K+1}_{\alpha}}{\arg\min} \alpha \|\mathbf{q}^{(t)} - \mathbf{s}\|_2^2 - \beta \|\mathbf{s}\|_2^2,$$

where  $t = 1, 2, ..., t_{\text{max}}$  is the iteration counter. We initialize the above iterative procedure with  $\mathbf{s}^{(0)} = \check{s}(G_{1,1})^{-1}\mathbf{g}_1$ , where  $\mathbf{g}_1$  is the first column of  $\mathbf{G}$ , and  $\check{s} \in \mathcal{O}$  is the fixed symbol transmitted in the first time slot and known at the receiver.

Since the problem in (4) is biconvex in s and q, both of the above steps are convex and can be solved optimally and in closed form. Concretely, we get the following simple algorithm:

$$\mathbf{q}^{(t)} = (\mathbf{I} - \alpha^{-1} \mathbf{G})^{-1} \mathbf{s}^{(t-1)}$$
  
$$\mathbf{s}^{(t)} = \operatorname{prox}_{\mathcal{C}^{K+1}}(\theta \mathbf{q}^{(t)}), \qquad (5)$$

where  $\theta = \frac{\alpha}{\alpha - \beta} > 0$ , **I** is the identity, and the proximal operator [12]

$$\operatorname{prox}_{\mathcal{C}_{\mathcal{O}}^{K+1}}(\mathbf{v}) = \underset{\mathbf{s}\in\mathcal{C}_{\mathcal{O}}^{K+1}}{\operatorname{arg min}} \|\mathbf{v} - \mathbf{s}\|_{2}^{2}$$
(6)

is the element-wise orthogonal projection onto the convex hull  $C_{\mathcal{O}}$ . For BPSK, the proximal operator in (6) is given by  $\operatorname{prox}_{\mathcal{C}_{\text{BPSK}}}(v_b) =$ 

#### Algorithm 1 PRojection Onto conveX hull (PrOX)

1: inputs: 
$$\widehat{\mathbf{G}}$$
,  $\mathbf{s}^{(0)}$ , and  $\varrho$ 

2: for  $t = 1, ..., t_{\max}$  do

3: 
$$\mathbf{q}^{(0)} = \mathbf{Gs}^{(0-1)}$$
  
4:  $\mathbf{s}^{(t)} = \operatorname{prox}_{\mathbf{s}, K+1}(\rho \tilde{\mathbf{q}}^{(t)})$ 

$$\mathbf{s}^{(t)} = \operatorname{prox}_{\mathcal{C}^{K+1}_{\mathcal{O}}}(\varrho \mathbf{q}^{(t)})$$

5: 
$$s_1^{(t)} =$$

6: end for

7: **outputs:**  $\hat{s}_k = \arg\min_{s \in \mathcal{O}} |s_k^{(t_{\max})} - s|, k = 2, \dots, K+1$ 



Fig. 1. Block diagram of PrOX. We use a linear array of processing elements (PEs) that achieves high throughput at low hardware complexity.

max {min { $\Re(v_b), +1$ }, -1}; for QPSK, (6) corresponds to applying the same operation, independently, to  $\Re(v_b)$  and  $\Im(v_b)$ . In the case of (5),  $\mathbf{v} = \theta \mathbf{q}^{(t)}$ , so the proximal operator in (6) projects a scaled version of  $\mathbf{q}^{(t)}$  onto the convex hull of the constellation—this is why we call our algorithm "PRojection Onto conveX hull" (PrOX).

# C. Hardware Optimizations for PrOX

We now modify the algorithm in (5) to make it more hardwarefriendly. Since the receiver knows the first entry of s, there is no need to apply the algorithm on this particular entry—instead, we force  $s_1^{(t)}$ to be  $\check{s}$  at the end of each iteration. The matrix  $(\mathbf{I} - \alpha^{-1}\mathbf{G})^{-1}$ exhibits a large dynamic range for different system configurations and channel realizations. To facilitate fixed-point design, we divide all of its elements by a constant  $\gamma > 0$ , so that the entries of the resulting matrix are close to one in absolute value. This scaling procedure requires us to introduce a new vector  $\tilde{\mathbf{q}} = \gamma^{-1}\mathbf{q}$ , resulting in

$$\tilde{\mathbf{q}}^{(t)} = \gamma^{-1} \mathbf{q}^{(t)} = \gamma^{-1} (\mathbf{I} - \alpha^{-1} \mathbf{G})^{-1} \mathbf{s}^{(t-1)}$$
$$\mathbf{s}^{(t)} = \operatorname{prox}_{\mathcal{C}_{\mathcal{O}}^{K+1}}(\theta \gamma \tilde{\mathbf{q}}^{(t)}) = \operatorname{prox}_{\mathcal{C}_{\mathcal{O}}^{K+1}}(\varrho \tilde{\mathbf{q}}^{(t)}),$$
(7)

where  $\rho = \theta \gamma$ . By defining  $\widehat{\mathbf{G}} = \gamma^{-1} (\mathbf{I} - \alpha^{-1} \mathbf{G})^{-1}$ , we arrive at the hardware-friendly version of PrOX summarized in Algorithm 1. We note that  $\alpha > 0$  and  $\rho > 0$  are both algorithm parameters that can be tuned to empirically improve the performance of PrOX.

# IV. VLSI ARCHITECTURE

A. Architecture Overview

Figure 1 shows the proposed VLSI architecture for PrOX in a system with QPSK modulation. Our architecture is a linear array formed of N = K + 1 processing elements (PEs), each associated with an entry of s and  $\tilde{\mathbf{q}}$ . To execute Algorithm 1, each PE consists of three key components. The first component is the  $\hat{\mathbf{G}}$ -matrix memory: The *k*th PE contains memory for the real and imaginary parts of  $\hat{\mathbf{g}}_{K}^{r}$ ,



Fig. 2. Uncoded packet error rate (PER) for a SIMO system with B = 16 BS antennas and transmission over K = 16 time slots. PrOX achieves nearoptimal PER performance (close-to perfect CSIR) and exhibits a performance similar to ML-JED. TASER [8] entails a 1 dB SNR loss for the QPSK case, while conventional MRC with CHEST suffers a 4 dB SNR loss.

the *k*th row of  $\widehat{\mathbf{G}}$ . This memory is implemented using FPGA lookup tables (LUTs) as distributed RAM. We assume that the memory contents were computed during a preprocessing step. The second component is a complex-valued multiply-accumulate (MAC) unit, used to compute the matrix-vector product in line 3 of Algorithm 1. The third component is the projection unit, which executes line 4 of Algorithm 1. The hard-output estimates (see line 7 of Algorithm 1) are extracted from the sign bits of the outputs of the projection unit. As  $s_1^{(t)} = \check{s}$  is forced at the end of each iteration (line 5 of Algorithm 1), the first PE only contains two multiplexers and flip-flops that store  $\check{s}$ .

# B. Architecture Operation

We now detail the operating principle of the PrOX architecture shown in Figure 1. To prevent a high fan out, the entries of the  $\widehat{\mathbf{G}}$  matrix are stored in a way that, for the *k*th PE, the first address of its memories contains  $\widehat{G}_{k,k}$ ; the second address,  $\widehat{G}_{k,k+1}$ , and so on. In the first clock cycle, the *k*th PE has access to  $s_k^{(t-1)}$ , so it can compute the product  $\widehat{G}_{k,k}s_k^{(t-1)}$  and store the result in its accumulator. At the same time, this PE sends  $s_k^{(t-1)}$  to the (k-1)th PE. In the second clock cycle, the *k*th PE receives  $s_{k+1}^{(t-1)}$  from the (k+1)th PE, so it can compute  $\widehat{G}_{k,k+1}s_{k+1}^{(t-1)}$  and add it to the previous result. This clock cycle is also used by this PE to transmit  $s_{k+1}^{(t-1)}$  to the (k-1)th PE. In the third clock cycle, the *k*th PE receives  $s_{k+2}^{(t-1)}$  from the (k+1)th PE (which received this value from the (k+2)th PE during the second cycle), so the *k*th PE can continue executing its complex-valued MAC operation. This process is replicated in all PEs, enabling each entry of  $\mathbf{s}^{(t-1)}$  to circulate through the linear array. After K + 1 cycles, all PEs have had access to all entries of  $\mathbf{s}^{(t-1)}$  and used them to compute their respective entry of  $\widetilde{\mathbf{q}}^{(t)}$ . During this process, the first PE (which differs from the other PEs) executes the same procedure: it first sends  $\check{s}$  to the (K+1)th PE. to the (K+1)th PE.



Fig. 3. Throughput vs. performance trade-off for K = 16 time slots. Vertical solid lines represent MRC with CSIR; dashed lines represent ML-JED. The numbers next to the markers correspond to the number of PrOX iterations  $t_{max}$ .

As the MAC units contain three pipeline stages, two clock cycles are required to flush the pipeline. Hence, the matrix-vector multiplication on line 3 of Algorithm 1 is computed in K + 3 clock cycles.

We now describe the operation of the projection unit. For QPSK constellations, the unit consists of two identical modules (cf. Figure 1). One of these modules takes  $\bar{q} = \Re(\tilde{q}^{(t)})$  as its input, while the other takes  $\bar{q} = \Im(\tilde{q}^{(t)})$ . Each module checks whether its input  $\bar{q}$ , after being multiplied with  $\varrho$ , is below -1, above +1 or in-between these numbers, and outputs -1, +1, or  $\varrho\bar{q}$ , respectively. To do so, each module takes its input and adds, separately,  $-1/\varrho$  and  $+1/\varrho$  to it. The two results are used to select the output value. The quantity  $\varrho\bar{q}$  is computed in parallel. By restricting  $\varrho$  to be a power of two, the multiplication can be carried out with arithmetic shifts. The projection unit uses one clock cycle to complete its operation, but it can start only after the K + 3 cycles used by the complex MAC unit. After the projection unit has finished, the new  $s_k^{(t)}$  will be available at the inputs of the complex-valued MAC unit, ready to start a new iteration. Consequently, each PrOX iteration requires K + 4 clock cycles.

## C. Fixed-Point Parameters

We use 6 bit fixed-point values for representing the  $s^{(t)}$  entries, with 3 fraction bits. For the elements of  $\hat{G}$ , 12 bit fixed-point values are used, with 11 fraction bits. The intermediate values and outputs of the complex-valued MAC unit use 15 bits with 11 fraction bits.

# V. IMPLEMENTATION RESULTS AND COMPARISON

#### A. Error-Rate Performance

Figures 2(a) and 2(b) show packet error rate (PER) simulation results for PrOX as in (5) for  $t_{max} = 5$  iterations. The results are obtained from 50,000 Monte-Carlo trials in a B = 16 BS antenna SIMO system with K = 16 time slots, using an i.i.d. flat Rayleigh blockfading channel model. We show the performance of maximum ratio combining (MRC) detection with both perfect receive-side channel state information (CSIR) and channel estimation (CHEST), ML-JED

 TABLE I

 IMPLEMENTATION RESULTS ON A XILINX VIRTEX-7

 XC7VX690T FPGA FOR DIFFERENT PROX ARRAY SIZES

Array size $(N = K+1)$ Time slots $(K = N-1)$	N = 5 K = 4	N = 9 K = 8	$\substack{N=17\\K=16}$	N = 33 K = 32
Slices	327	658	1 491	3 0 1 8
LUTs	990	1 991	4818	9861
FFs	515	989	1953	3 857
DSP48s	16	32	64	128
Max. clock freq. [MHz]	358	341	297	240
Min. latency [cycles]	8	12	20	36
Max. throughput <sup>a</sup> [Mb/s]	358	454	475	426
Power estimate <sup>b</sup> [W]	0.45	0.47	0.79	1.14

<sup>*a*</sup>Assuming QPSK modulation; for BPSK, the throughput is halved. <sup>*b*</sup>Statistical power estimation at max. clock freq. and 1.0 V supply voltage.

detection using the method in [7], and the recent TASER algorithm [8] with 20 iterations. Note that MRC with perfect CSIR is optimal for this scenario. However, the assumption of perfect CSIR cannot be realized in practice and one must resort to CHEST, which entails a performance loss of more than 4 dB at 1% PER. PrOX significantly outperforms MRC with CHEST and approaches near-ML-JED performance but, in contrast to ML-JED detection, at very low complexity. We also show the performance of the VLSI design of PrOX as in Algorithm 1; our fixed-point design exhibits virtually no implementation loss.

Figures 3(a) and 3(b) show the trade-off between the throughput of PrOX and the minimum SNR required to achieve 1% PER, for SIMO systems with K = 16 time slots and different numbers of BS antennas. As a reference, we include the performance of MRC with CSIR and that of an optimal ML-JED detector. By increasing the number of PrOX iterations  $t_{max}$ , the desired PER is achieved at a lower SNR at the expense of lower throughput. Note that for BPSK modulation, 2 iterations are typically enough to reach near-ML-JED performance, which leads to a throughput of 118 Mb/s. For QPSK, 3 iterations are sufficient and achieve 158 Mb/s.

#### **B.** Implementation Results

To demonstrate the efficacy of PrOX, we developed FPGA designs for various array sizes  $N \in \{5, 9, 17, 33\}$  that support JED for  $K \in \{4, 8, 16, 32\}$  time slots, respectively. Our FPGA implementation results are shown in Table I. As expected, the resource utilization scales linearly with the array size N. For the  $N \in \{5, 9, 17\}$  arrays, the critical path is in the PEs' projection unit; for the N = 33 array, the critical path is in the distribution of control signals.

Table II compares PrOX with TASER [8], which has been implemented on the same FPGA for a SIMO system with B = 128 BS antennas and communication through K = 8 time slots. PrOX requires significantly fewer resources and a lower power than TASER, while achieving a higher throughput. This makes this design superior to TASER in terms of both hardware-efficiency (measured in throughput per FPGA LUTs) and energy per bit: PrOX is  $20 \times$  more hardwareefficient and  $8 \times$  more energy-efficient than TASER for the considered scenario. At the same time, PrOX exhibits a similar (for BPSK) or better (for QPSK) PER performance than TASER, while using fewer iterations, as shown in Figures 2(a) and 2(b). We note that while PrOX is only suitable for JED in large SIMO, TASER can also perform near-ML data detection in coherent massive MIMO systems [8].

#### VI. CONCLUSIONS

We have proposed PrOX, a novel joint channel estimation and data detection (JED) algorithm for large SIMO systems with constant-

Detection algorithm Error-rate performance Iterations $t_{max}$	PrOX Near ML-JED 3	TASER [8] Near ML-JED 3
Slices LUTs FFs DSP48s Clock frequency [MHz] Latency [clock cycles] Throughout [Mb/c]	658 (0.61%) 1991 (0.46%) 989 (0.11%) 32 (0.89%) 341 12	4 350 (4.02%) 13 779 (3.18%) 6 857 (0.79%) 168 (4.67%) 225 72 50
Power estimate <sup><i>a</i></sup> [W]	0.47	1.30
Throughput/LUTs Energy/bit [nJ/b]	75 841 3.09	3 629 26.0

<sup>a</sup>Statistical power estimation at max. clock freq. and 1.0 V supply voltage.

modulus constellations, as well as a VLSI architecture. The low complexity of PrOX translates into a low-area, high-throughput, and low-power FPGA design. Our FPGA implementation for a SIMO system with K = 8 time slots achieves a maximum throughput of 454 Mb/s, while using only 2k FPGA LUTs. In addition, PrOX significantly outperforms TASER [8], the only other existing JED design, in all performance metrics.

We conclude by noting that PrOX is a first step towards hardware accelerators that are able to find approximate solutions to the MaxCut problem at low complexity and in a hardware-efficient manner. The design of accelerators for MIMO JED is part of ongoing research.

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