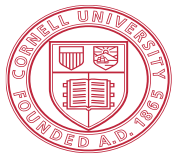
LAMDA: Learning-Assisted Multi-Stage Autotuning for FPGA Design Closure

Ecenur Ustun, Shaojie Xiang, Jinny Gui, Cunxi Yu, Zhiru Zhang

Electrical and Computer Engineering, Cornell University



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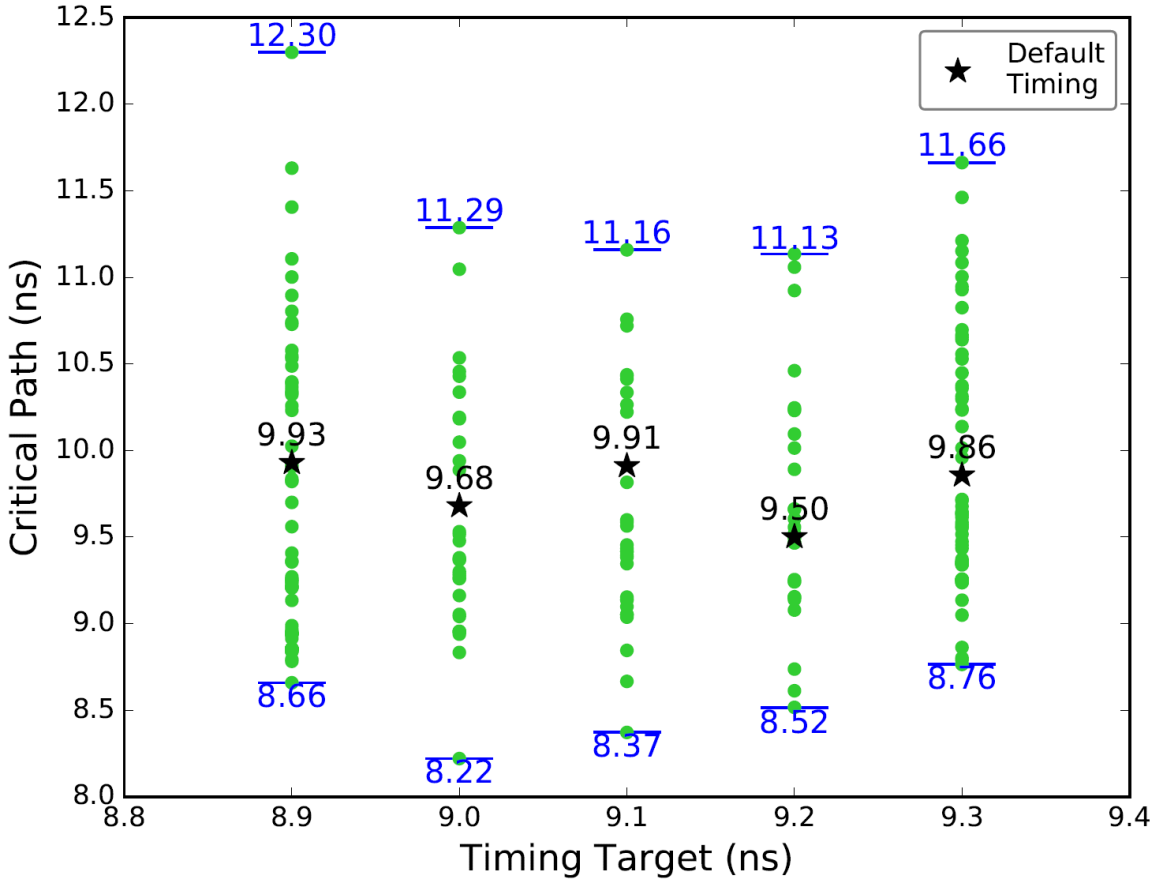
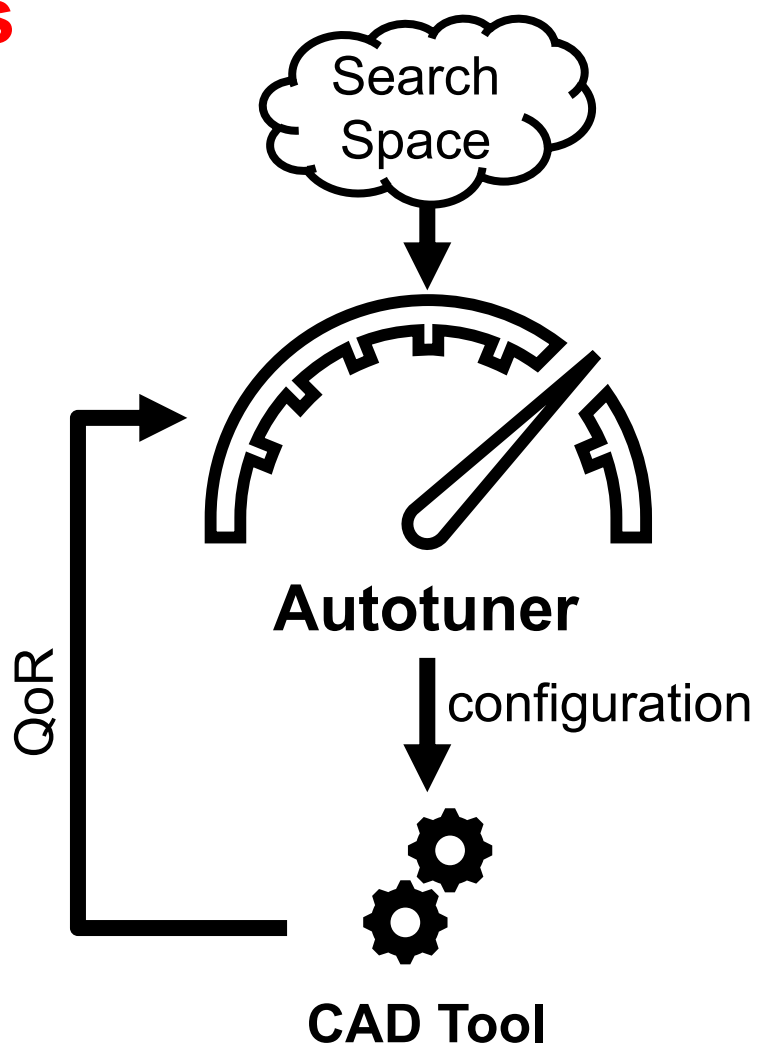
Auto-Configuring FPGA CAD Tools

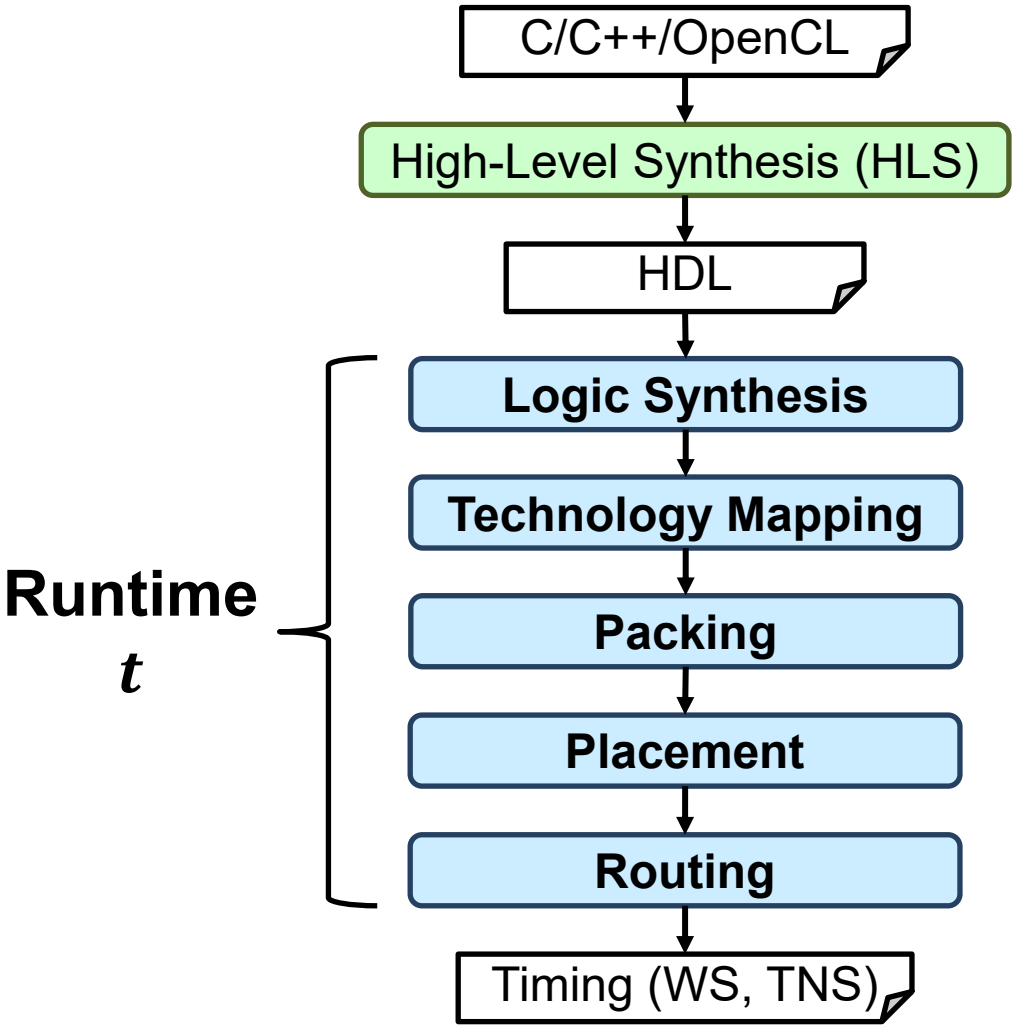


Timing distribution for various tool configurations and timing constraints



- InTime [Kapre et al., FPGA'15] [Yanghua et al., FPL'16]
- DATuner [Xu et al., FPGA'17]
- Nautilus [Papamichael et al., DAC'15]

Leveraging Multi-Stage ML Inference



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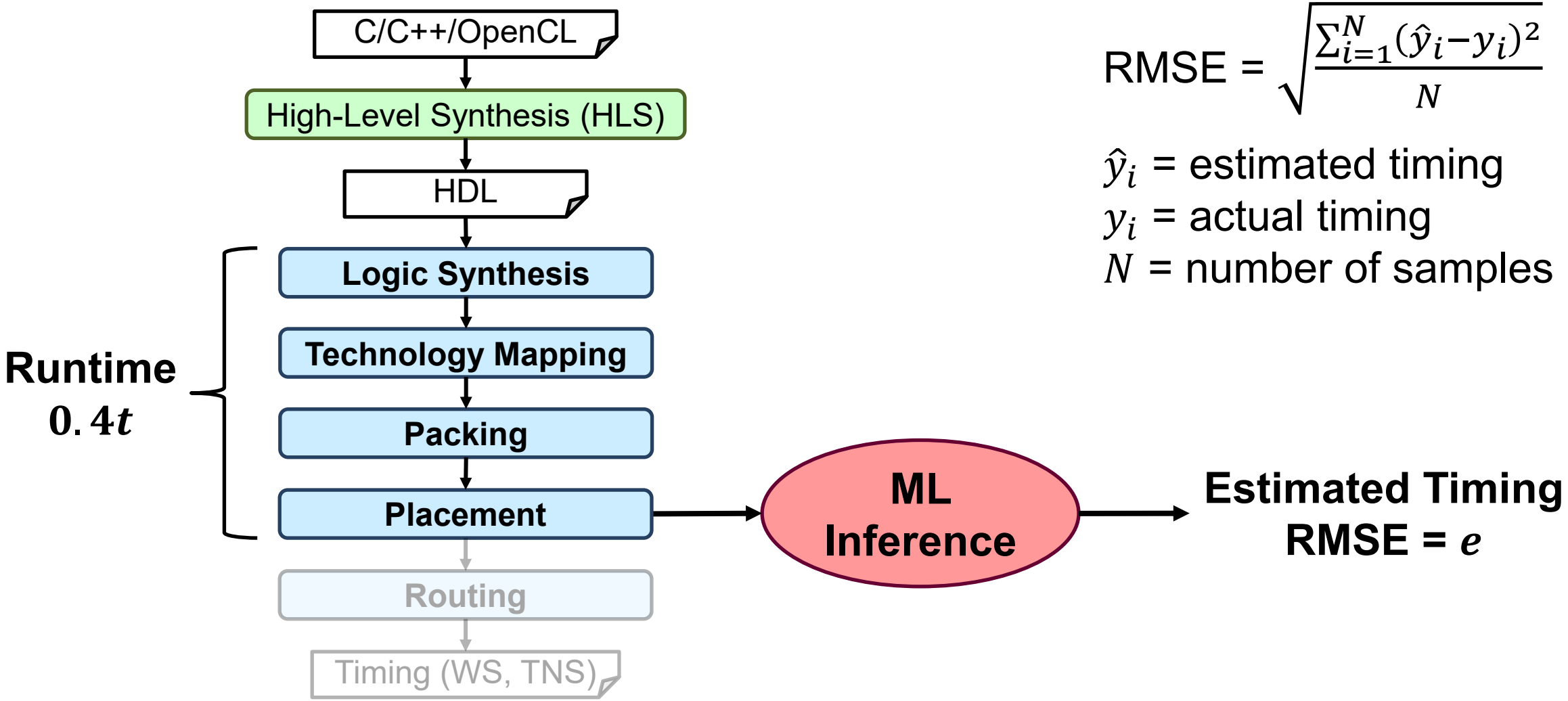
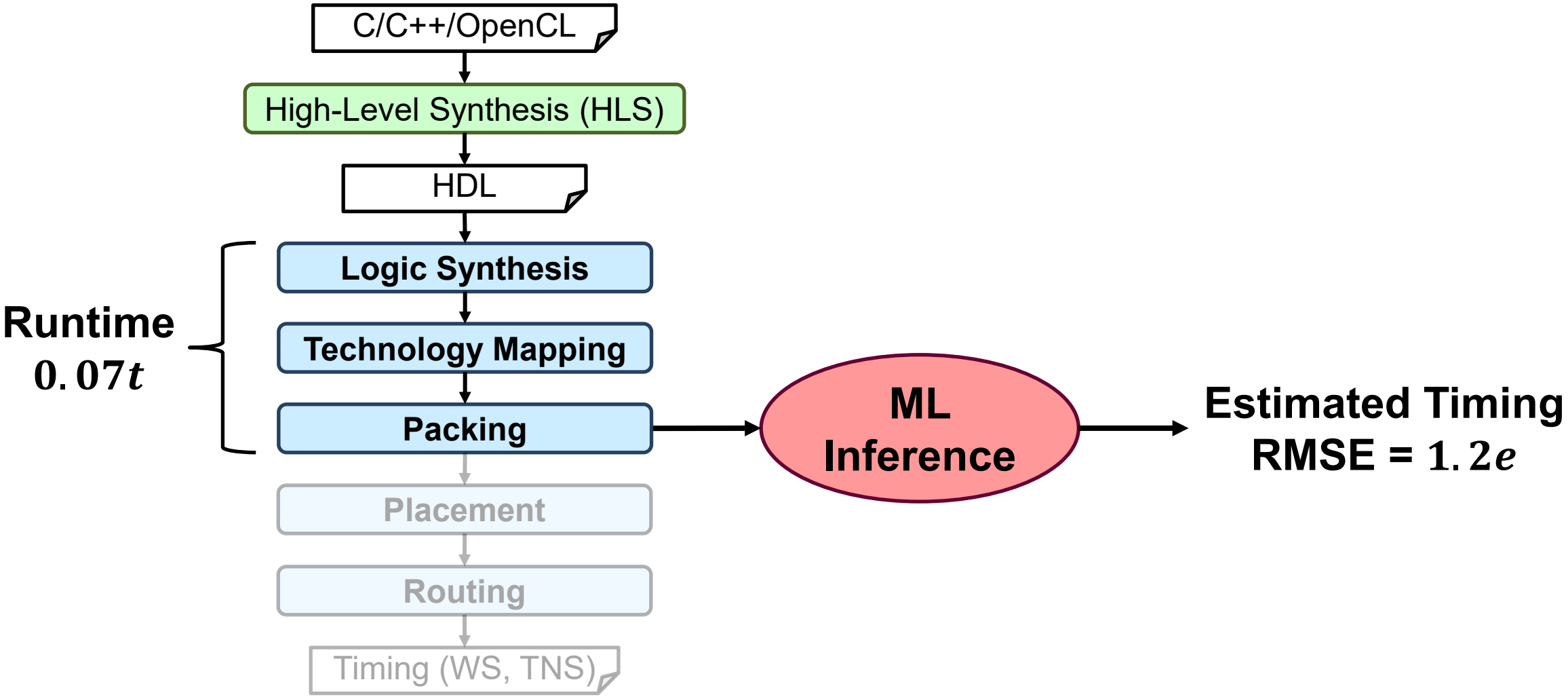


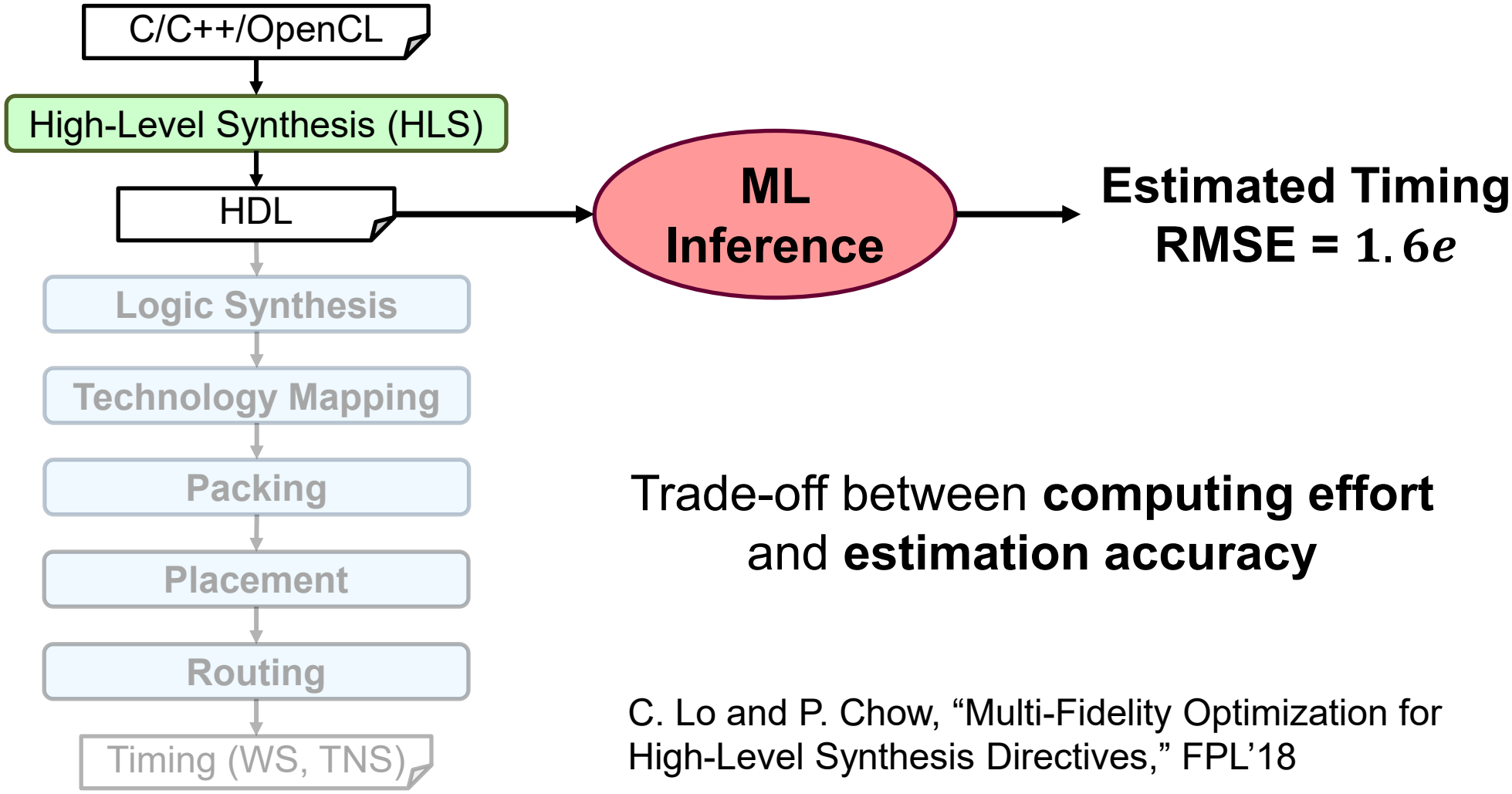
$$\text{RMSE} = \sqrt{\frac{\sum_{i=1}^{N}(\hat{y}_i - y_i)^2}{N}}$$

$\hat{y}_i$ = estimated timing
y_i = actual timing
N = number of samples

Leveraging Multi-Stage ML Inference



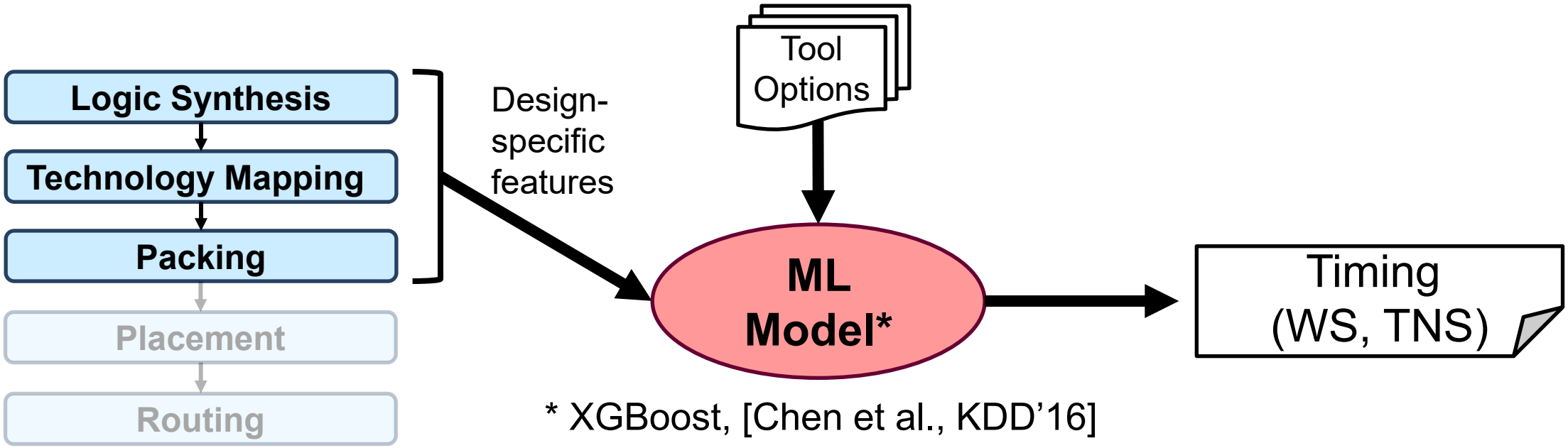
Leveraging Multi-Stage ML Inference



Trade-off between **computing effort** and **estimation accuracy**

C. Lo and P. Chow, "Multi-Fidelity Optimization for High-Level Synthesis Directives," FPL'18

ML-Based Timing Estimation Framework



Design Stage	Feature Type	Design-Specific Features
Logic Synthesis, Technology Mapping, and Packing	Resource	#ALM, #LUT, #registers, #DSP, #I/O pins, #fan-out, etc.
	Timing	WS, TNS

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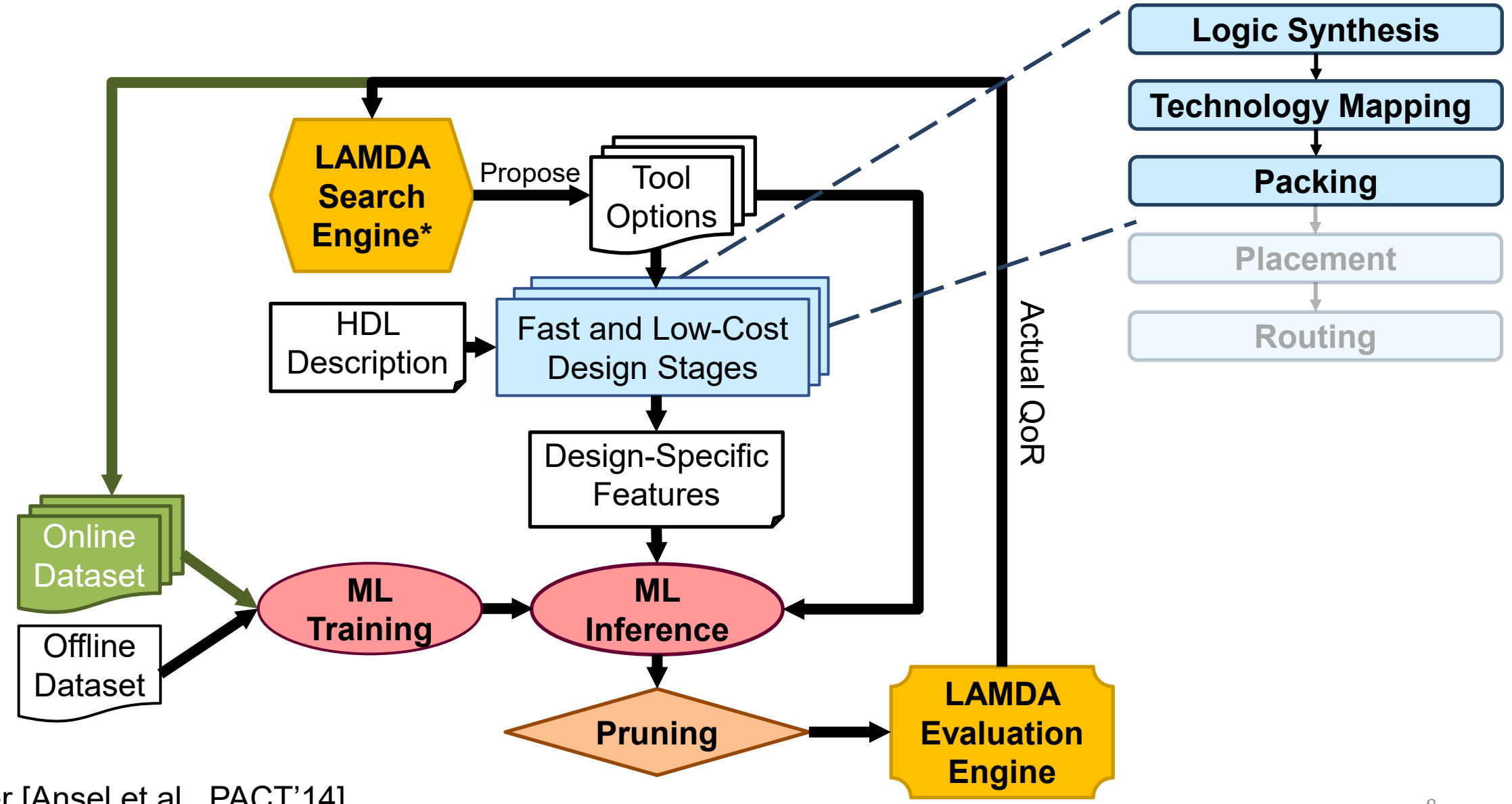


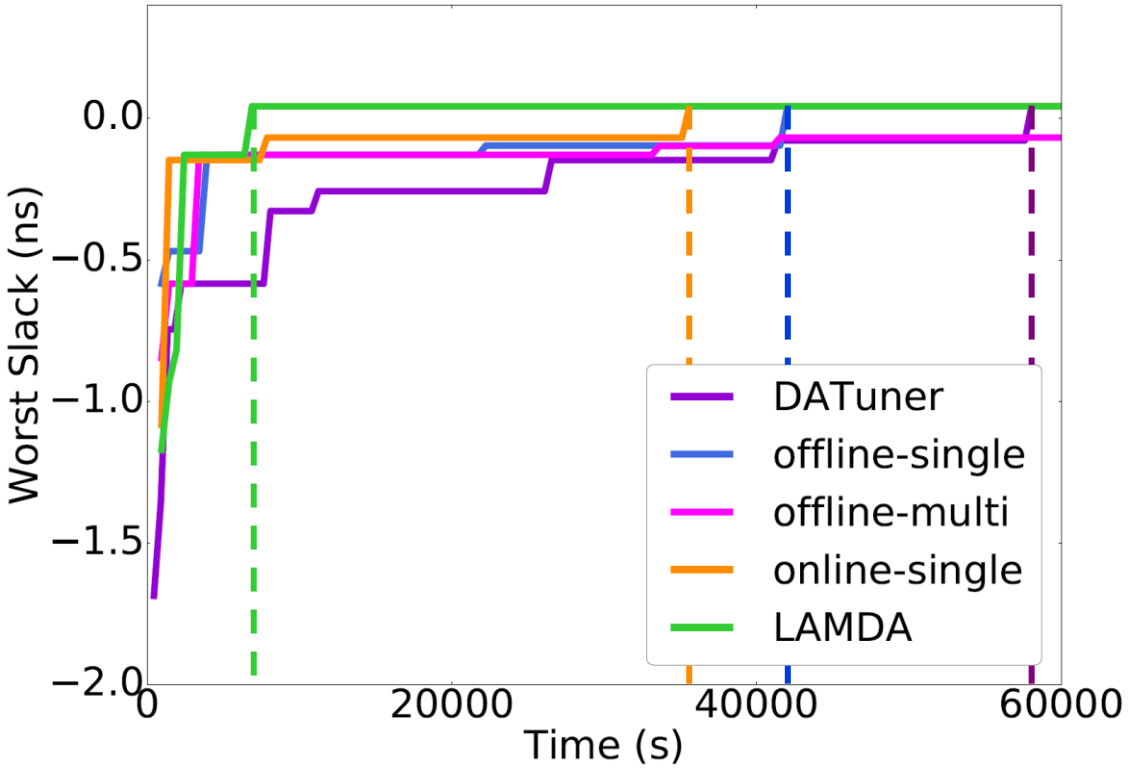
* OpenTuner [Ansel et al., PACT'14]

LAMDA – Evaluation I

Design	#ALUT	#FF	#DSP
dscg	6246	1679	4

		Online learning?	
		Yes	No
Leveraging design-specific features from early stages?	Yes	online-multi (LAMDA)	offline-multi
	No	online-single	offline-single

Global Best



On average;

- 5.43x speedup compared to DATuner*
- 4.38x speedup compared to offline-single

* DATuner [Xu et al., FPGA'17]

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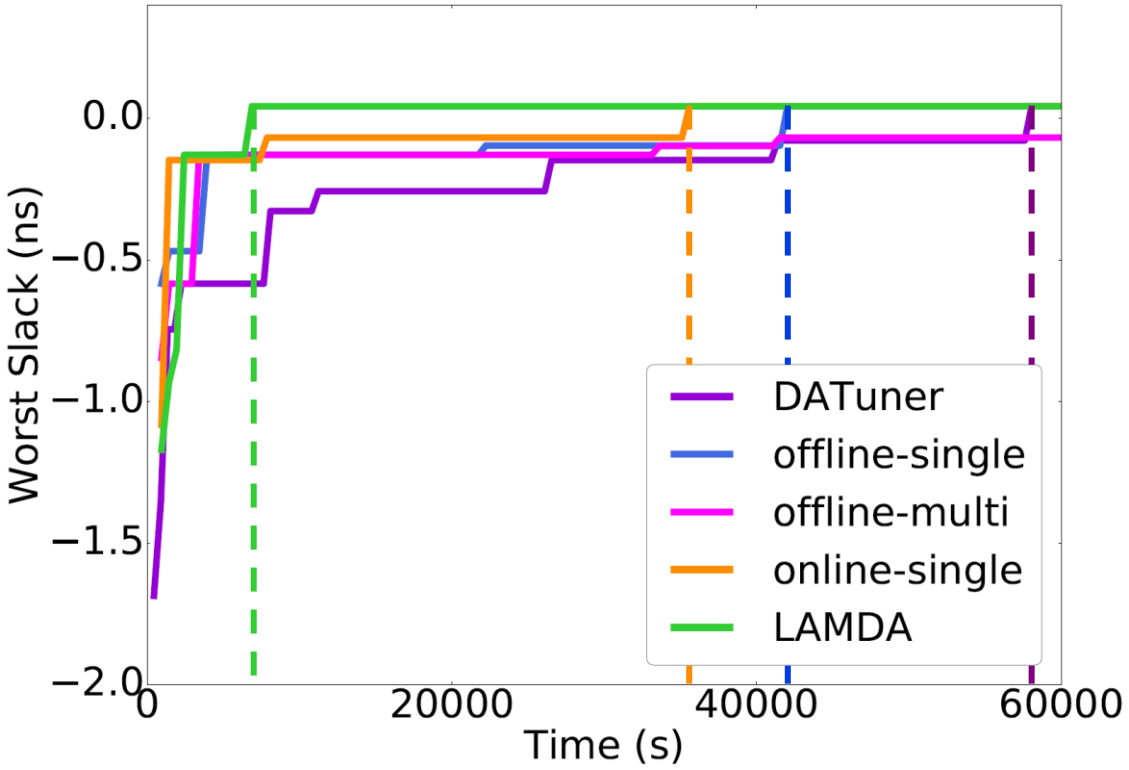
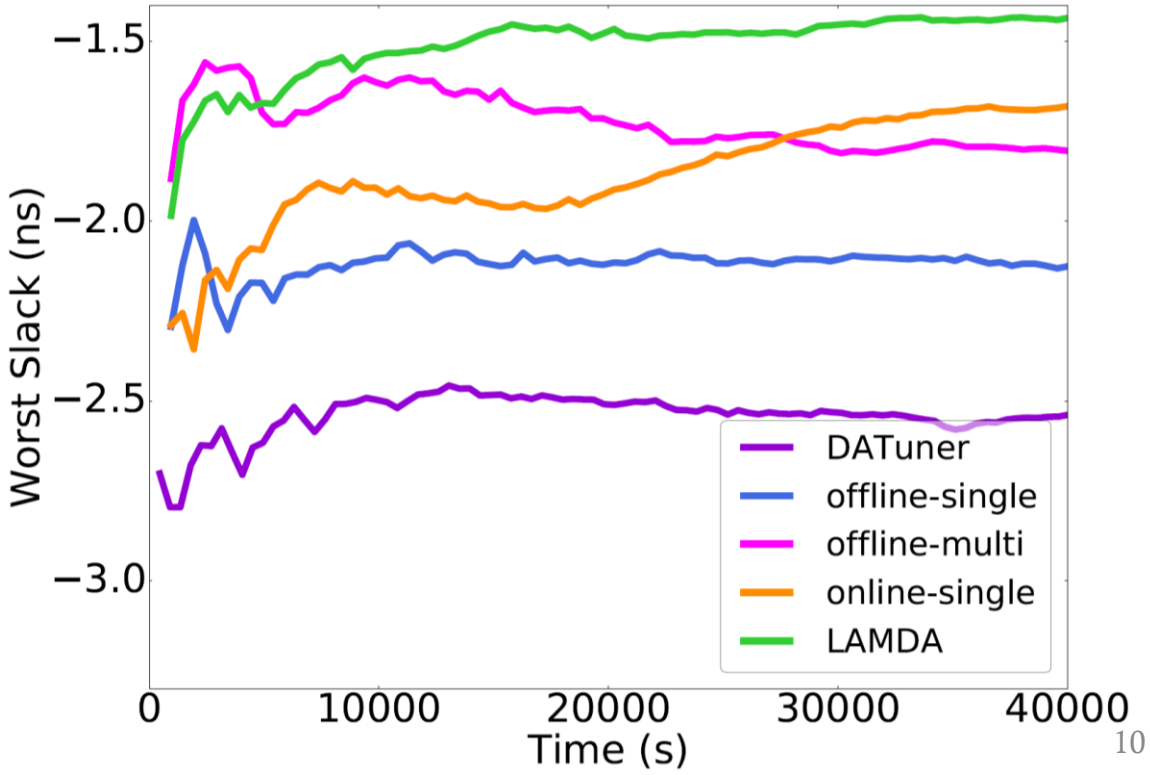
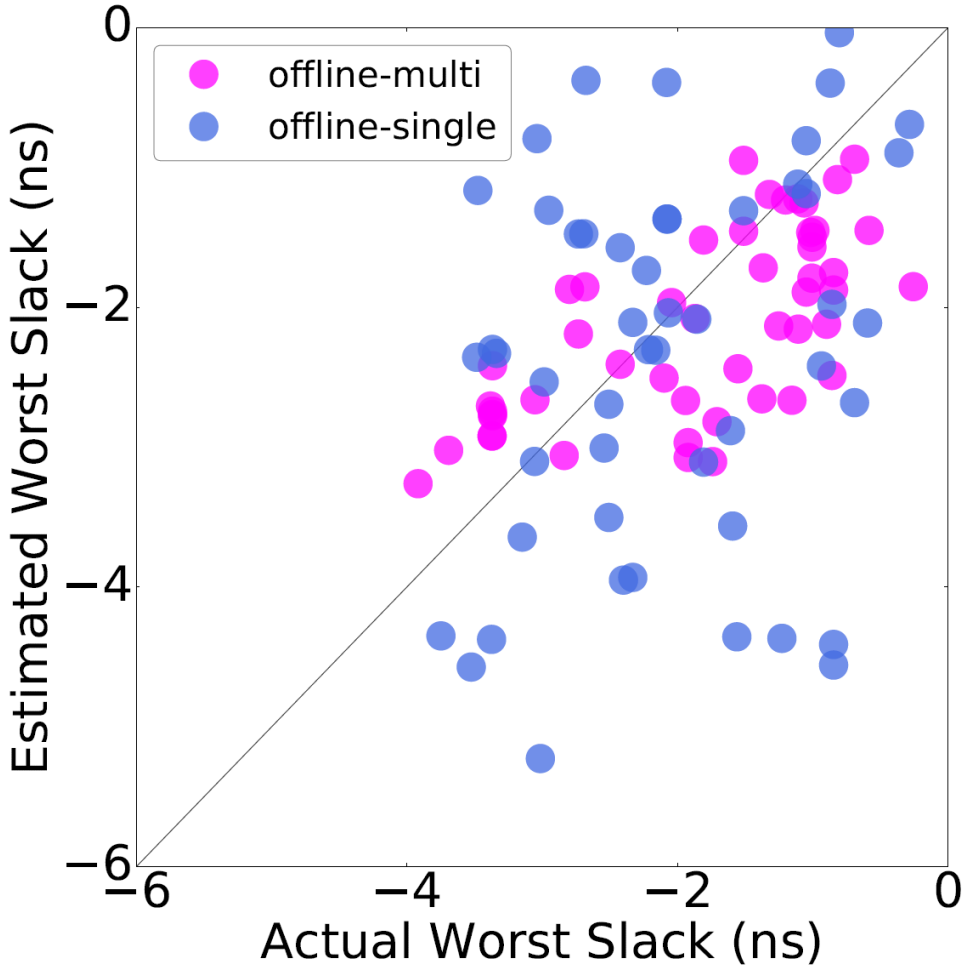
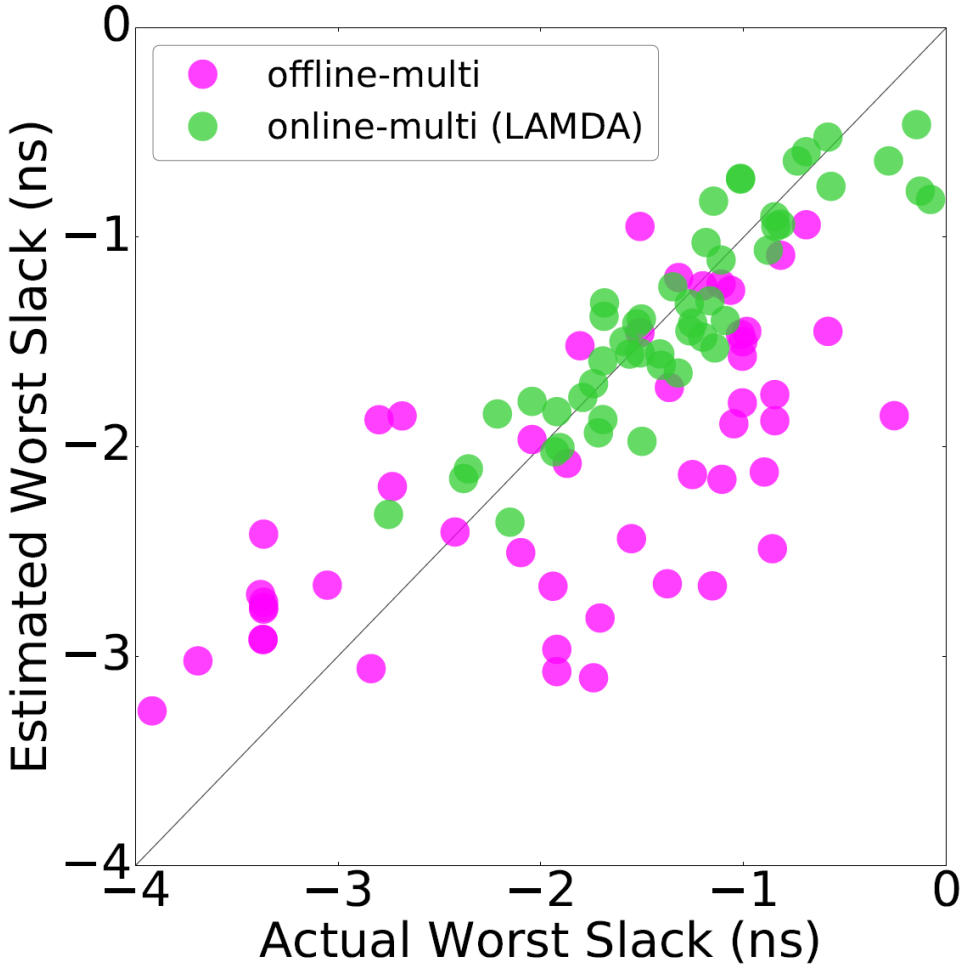


Global Mean



LAMDA – Evaluation II





Estimated versus actual QoR of design points visited

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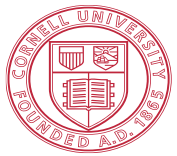
Thank you!



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