# ECE 6745 Digital ASIC Design

Instructor: Prof. Christopher Batten
TAs: Elton Shih, Parker Schless, Irwin Wang, Vayun Tiwari

*Cornell's first tape-out course in over 20 years!*

## 1 Course Overview

This course aims to provide a strong foundation for students to understand the principle and practice of designing, implementing, fabricating, testing, and evaluating standard-cell ASIC chips using automated electronic design automation tools. The course is structured around three projects each of which is 4–5 weeks long and completed in groups of 2–3 students. **This structure is unique among tape-out courses at other Universities and gives students deep experience in: (1) RTL-to-GDS flows; (2) a tape-out through a commercial foundry; and (3) designing more complex ASIC systems too large to tape-out.**

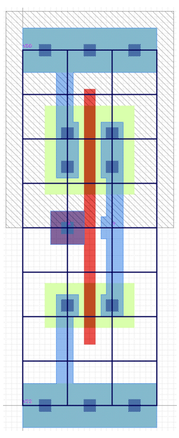
During the Spring 2026 offering, 47 students (3 PhD, 25 MEng, 19 seniors) taped-out a total of 20 1×1 mm chips in TSMC 180nm. These chips are being fabricated and packaged during the summer, and students will test their chips in the fall.

## 2 Project 1: Tiny Flow Tape-Out

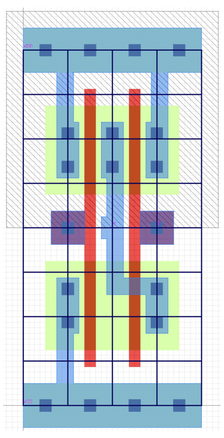
In the first project, students built their own simple standard-cell-based flow. They developed four standard cells using KLayout and 180nm lambda rules including behavioral, schematic, layout, extracted schematic, front-end, and back-end views. They implemented simple algorithms for synthesis and place-and-route:

- **Technology mapping** using tree covering and dynamic programming
- **Static timing analysis** to find the critical path using multiple tree traversals
- **Standard-cell placement** using simulated annealing and HPWL cost function
- **Interconnect routing** using 3D maze routing across metal layers 2–4

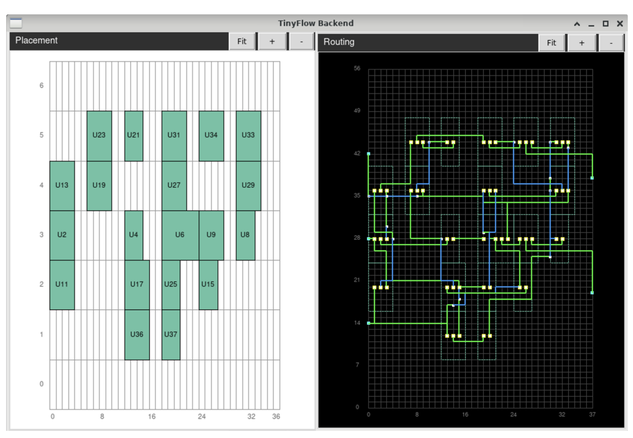
Finally, they combined this work with open-source Verilog RTL and gate-level simulators and an open-source LVS/DRC tool to create a Tiny RTL-to-GDS Flow. Even though their Tiny Flows only supported a very small combinational subset of Verilog, the project still gave students a unique hands-on opportunity to appreciate every step required in more sophisticated commercial flows. Each group created a macro using their Tiny Flow and these macros were aggregated by the teaching assistants into a single unified 1×1 mm tape-out in TSMC 180nm.



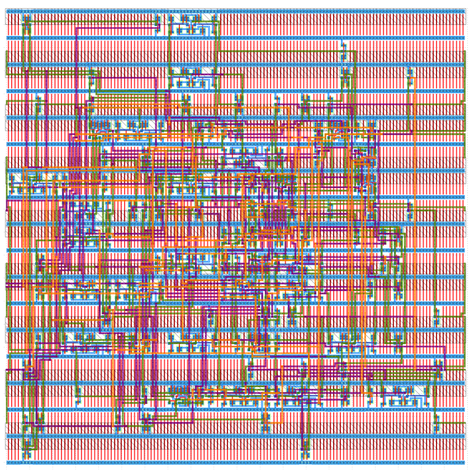
INVX1



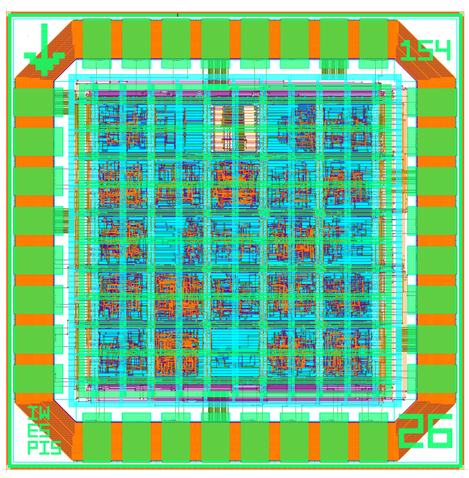
NAND2X1




Tiny Flow Place-and-Route GUI



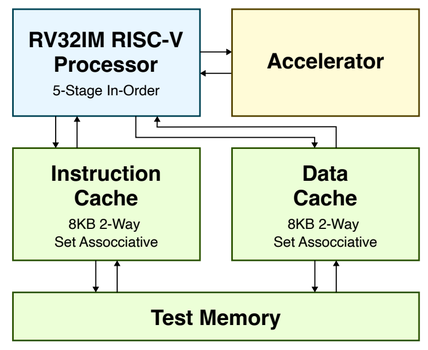
*Two students implemented a **four-bit multiplier** as a 100x100µm macro using their Tiny Flow with 544 cell instances including optional XOR2X1 standard cell; input/output pins fixed on left/right*

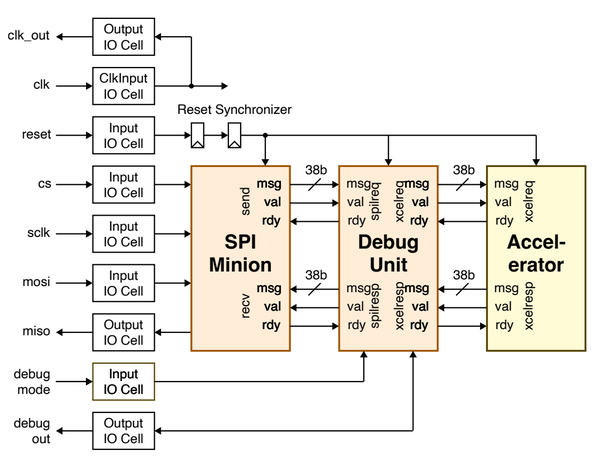


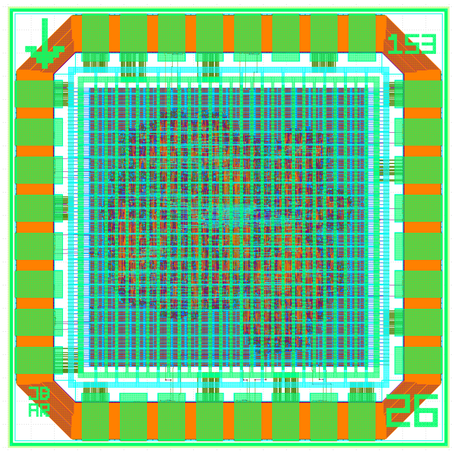
***Tiny Flow tape-out** integrating 25 macros sharing eight global input and eight global ouput pins; used commercial standard cells and tools for macro placement, power routing, and muxing logic*

## 3 Project 2: Accelerator Tape-Out

Students leveraged what they learned in the first project to transition to using a commercial standard-cell library and commercial electronic design automation tools for RTL simulation, synthesis, place-and-route, gate-level simulation, static-timing analysis, power analysis, DRC, and LVS. Students developed a co-processor accelerator in Verilog RTL and evaluated the performance, area, and energy of using this accelerator compared to their own baseline software implementation on a RISC-V processor. Students then combined just their accelerator with an SPI interface and used the commercial library and tools to turn this accelerator+SPI into a complete 1×1 mm chip layout in TSMC 180nm. Projects included hardware accelerators for binary neural networks, matrix multiplication, encryption, image processing, approximate multiplication, DNA alignment, vector processing, CORDIC, and priority queues.



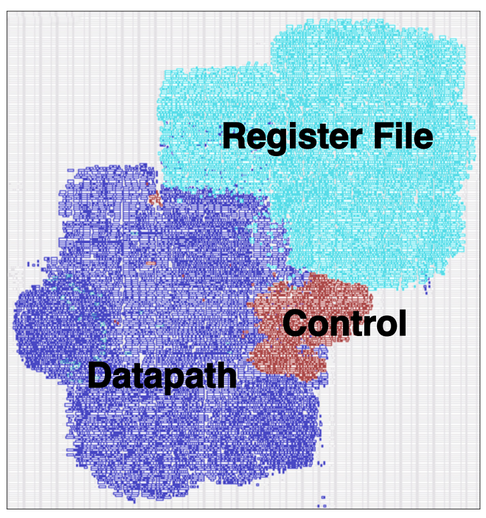



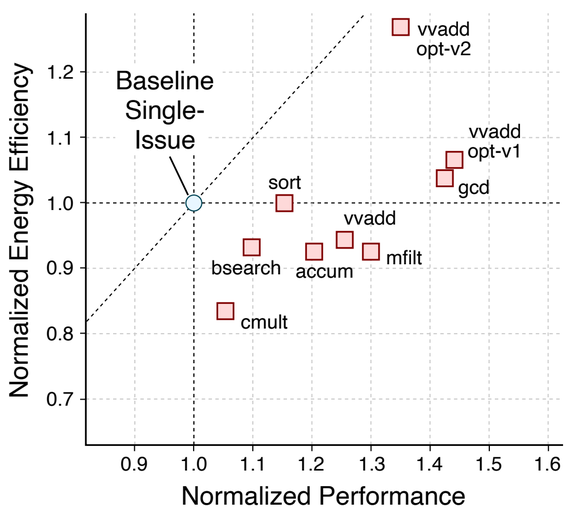



*Two students taped out a **digital leaky integrate-and-fire neural network accelerator** with an SPI interface; accelerator included a fixed two-layer 4×4 fully connected network that processed input spike streams one time step at a time*

## 4 Project 3: System-on-Chip Tape-In

The second projects were relatively simple owing to the small silicon area per tape-out. In the final project, students were free to explore any design they wished including advanced processor, memory, and/or network microarchitecture as well as various accelerators with a strong emphasis on a rigorous comparative analysis of performance, area, and energy. Projects included an optical flow accelerator, multiple end-to-end MLP accelerators, an in-order superscalar processor, a single-issue out-of-order processor, a floating point unit, a coarse grain reconfigurable array, and a graphics rendering accelerator.



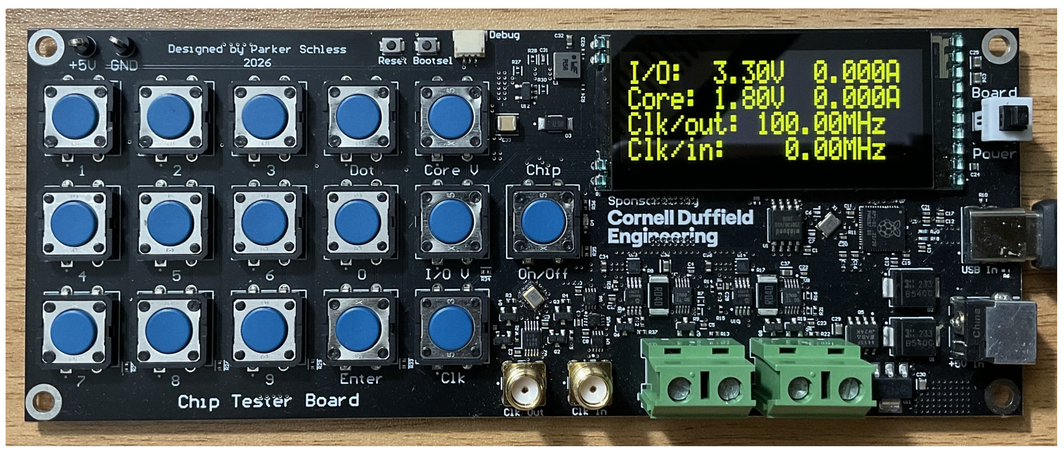

*Three students implemented a **dual-issue in-order superscalar processor** tape-in which would have been too large to fit on a 1×1 mm tape-out; students completed a detailed comparison of the energy and performance across various microbenchmarks*

## 5 Digital ASIC Chip Testing Practicum (Fall 2026)

Each chip will be packaged in a ceramic pin-grid-array (CPGA) package with glass lids to enable students to inspect their chips under the microscope. We have designed two custom boards:

- **Chip tester board** with two configurable voltage supplies with current sense, configurable clock generator with SMA connector, and a frequency counter with SMA connector
- **CPGA breakout board** that connects 30 I/Os to male header and connects the clock input and output pins to SMA connectors for high-speed clocking

The chip tester board, breakout board, USB-to-SPI adapter board, and two breadboards will be integrated into a unified chip testing platform. This fall, each group will wire up various components on their chip testing platform to enable: (1) clock loop-back testing; (2) SPI interface testing; and (3) accelerator testing. Students will also measure the energy consumption of their accelerator and create a shmoo plot to characterize their chip's operating regime.




Funding provided by the Cornell College of Engineering, the Center for Education of Microchip Designers, and the Taiwan Semiconductor Manufacturing Company.