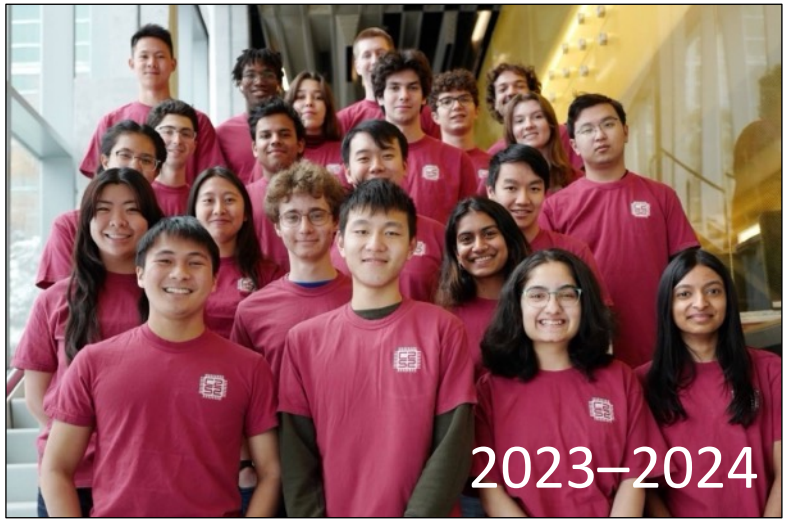
Experiential Learning for Semiconductor Chip Design through Student-Led Project Teams

Christopher Batten, Cornell University

NORDTECH Lunch & Learn, June 2025



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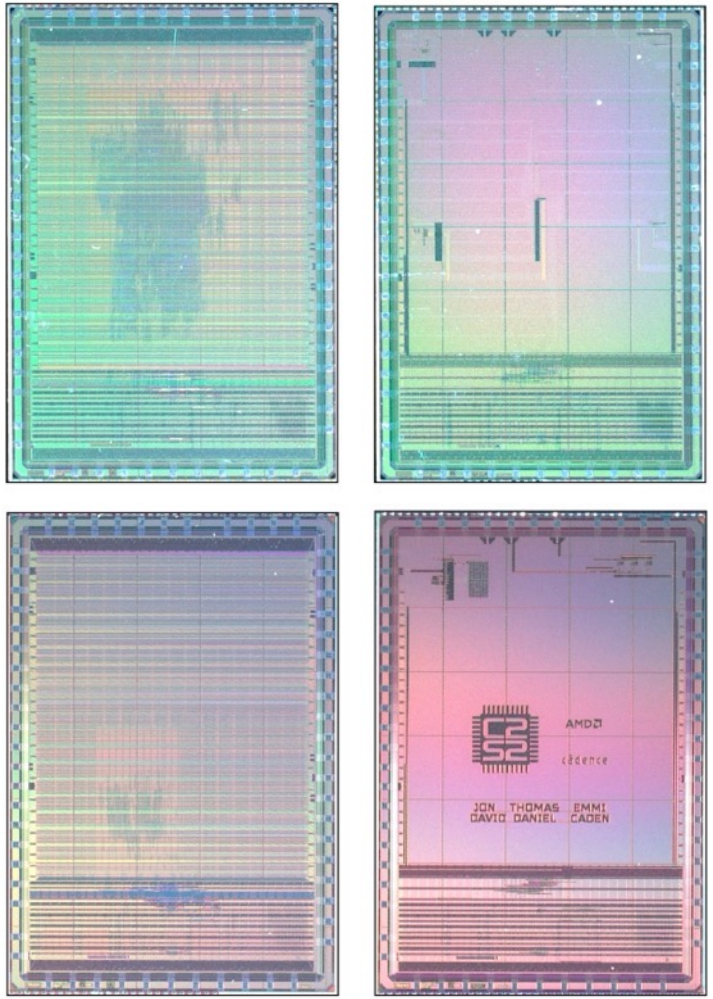
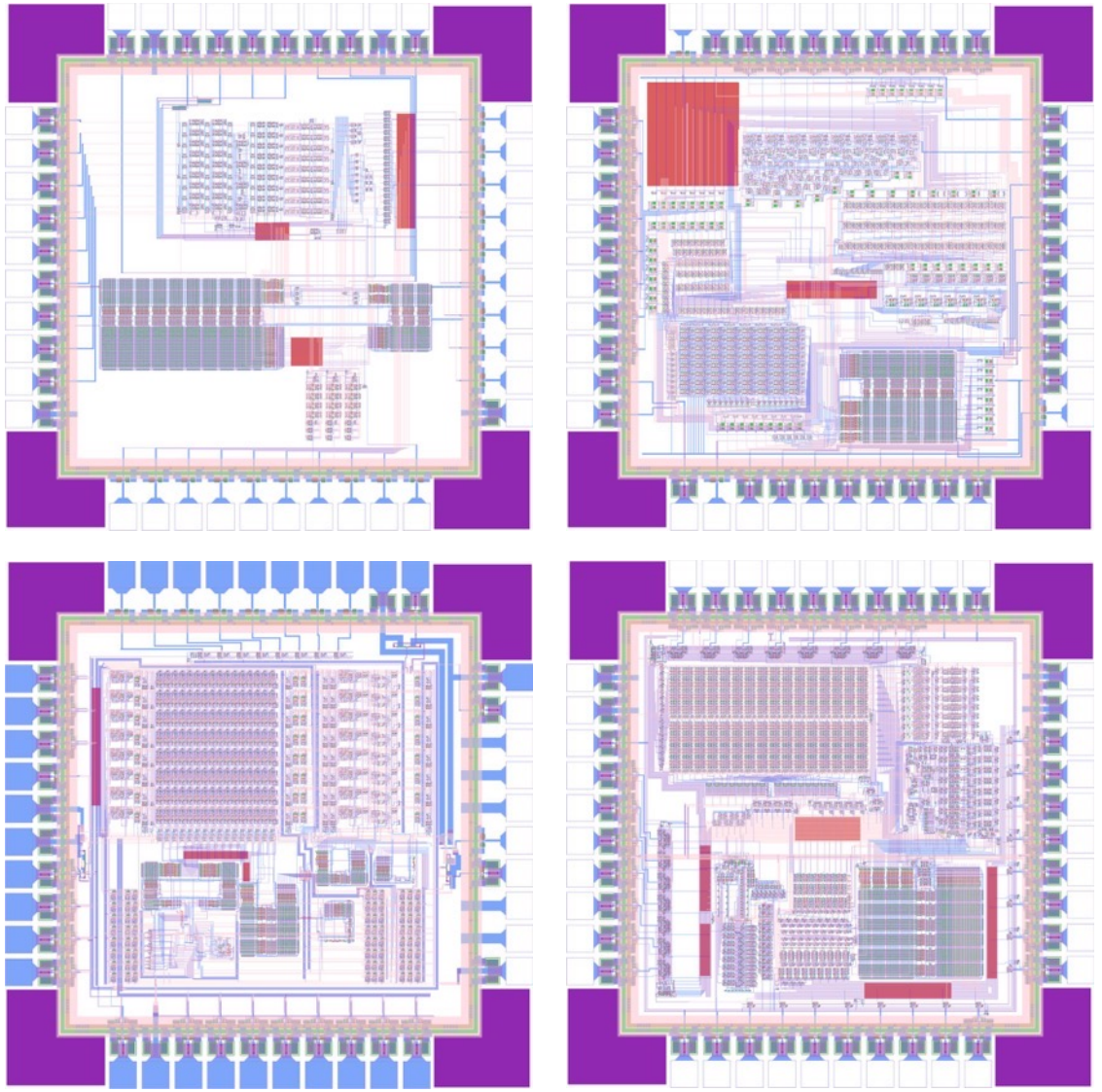


- Cornell Tape-Out Courses
- C2S2 Founding
- C2S2 Year 1: Campus Partner & Two Chips
- C2S2 Year 2: Two More SkyWater 130nm Chips
- C2S2 Year 3: Pivot to TSMC 180nm
- C2S2 Lessons Learned

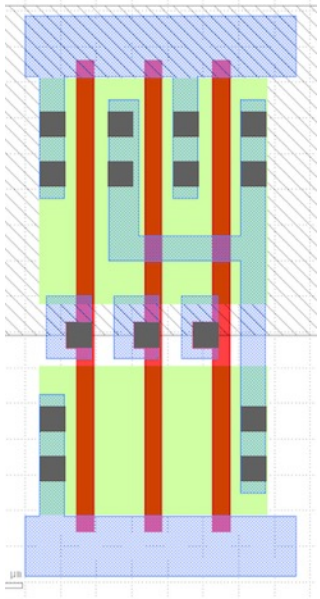
ECE 4750 Digital VLSI Tape-Out Option

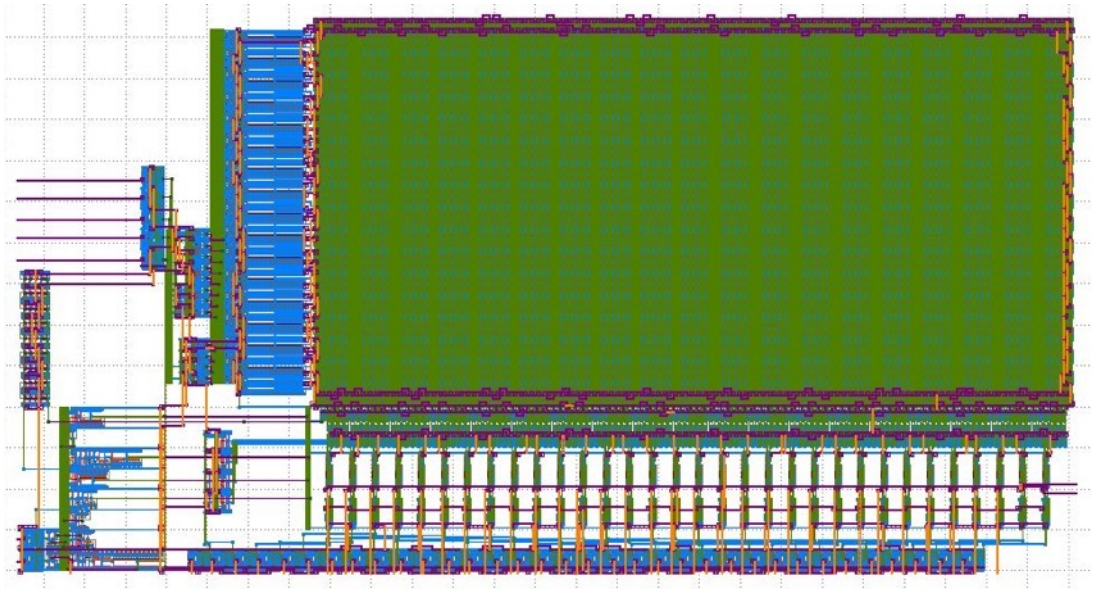
- ECE 4740 included a tape-out option in early 2000s when taught by Rajit Manohar (now at Yale)
- 1.5x1.5mm in AMI 0.5um
- Full-custom digital design using Magic and open-source tools
- Fully funded through MOSIS instructional program
- 2003 was the final year of the tape-out option due to funding and few instructors who could teach the course

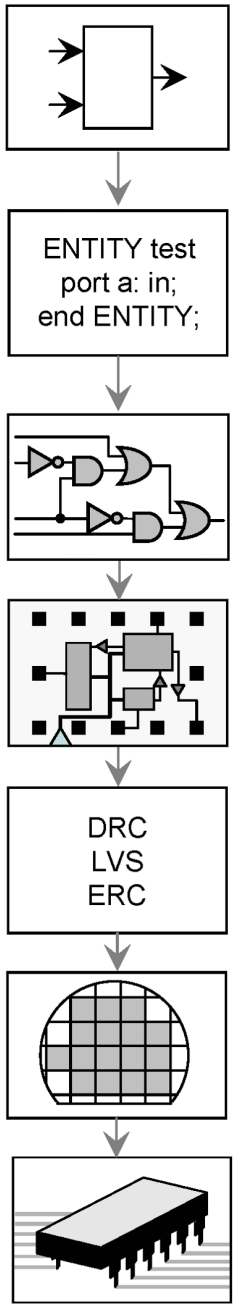


ECE 6745 Digital ASIC Design

- ECE 6745 teaches digital ASIC design using automated standard-cell-based methodologies
- Students "tape-in" design projects using state-of-the-art commercial tools from Synopsys and Cadence with FreePDK45, Nangate standard cells, and OpenRAM SRAM generator





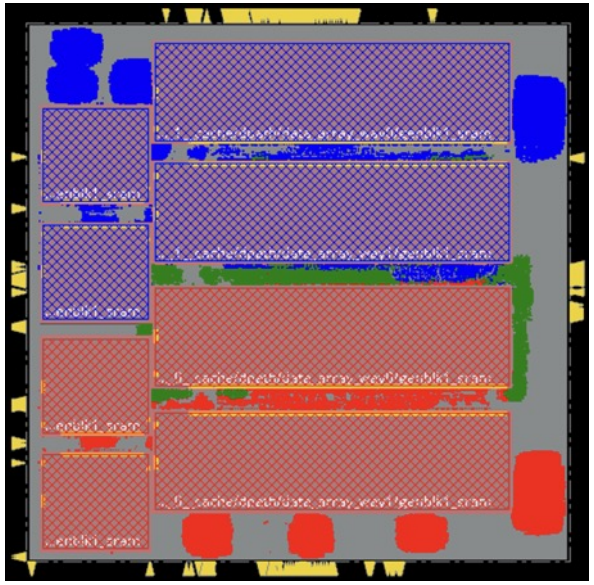


System Specification
↓
Architectural Design
↓
Functional Design and Logic Design
↓
Circuit Design
↓
Physical Design
↓
Physical Verification and Signoff
↓
Fabrication
↓
Packaging and Testing
↓
Chip

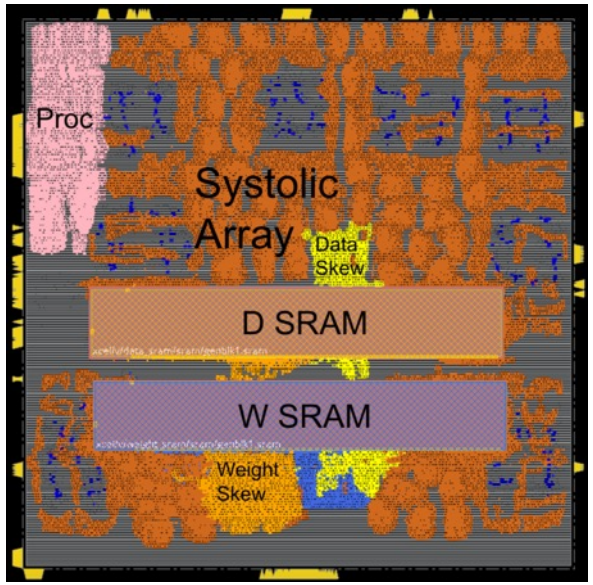
Tape-in Class

Tape-out Class

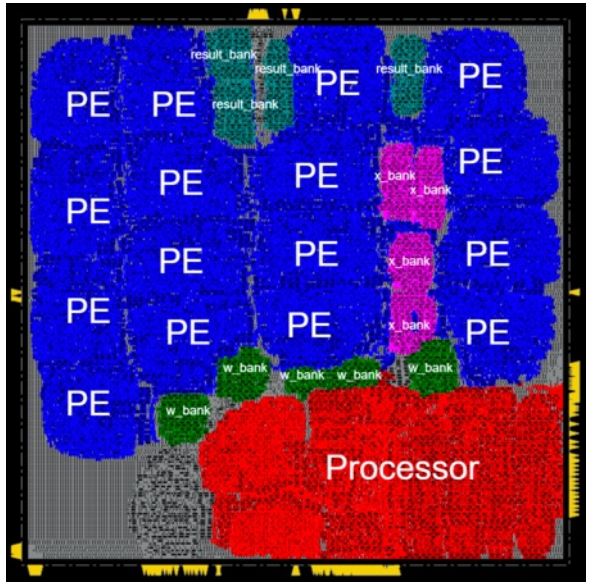
ECE 6745 Digital ASIC Design Tape-In Projects



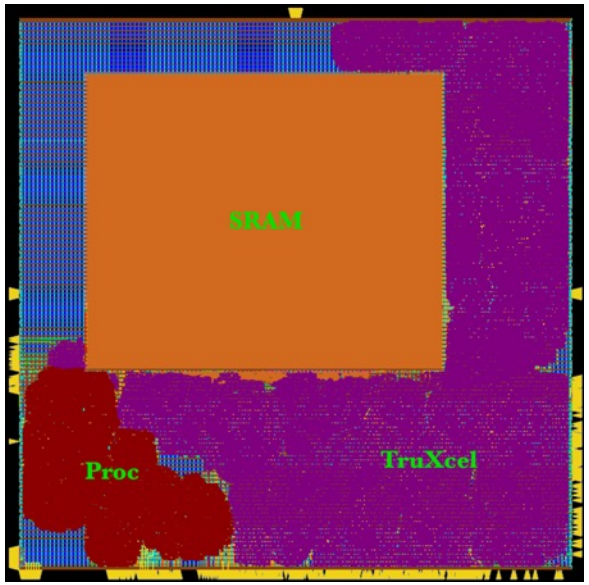
Snoopy Cache Coherent Memory System



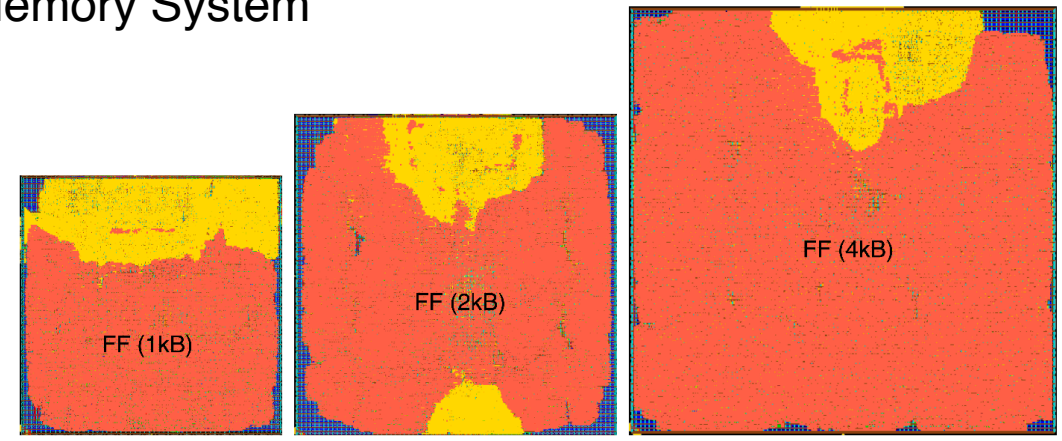
MLP Xcel

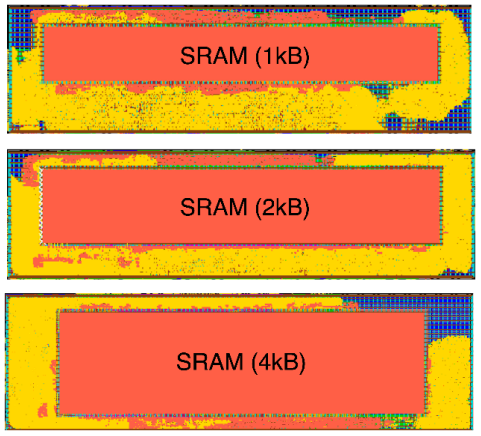


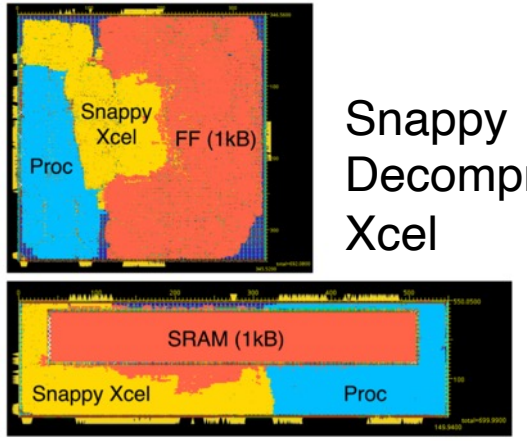
MLP Xcel



Graphics Rendering Xcel



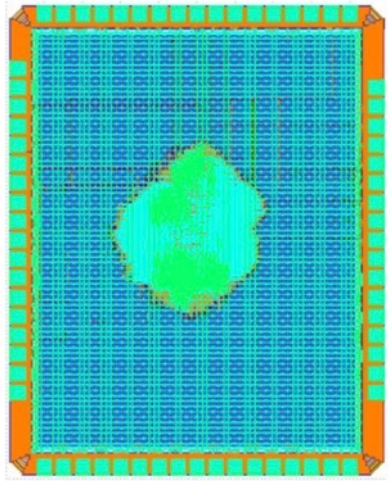


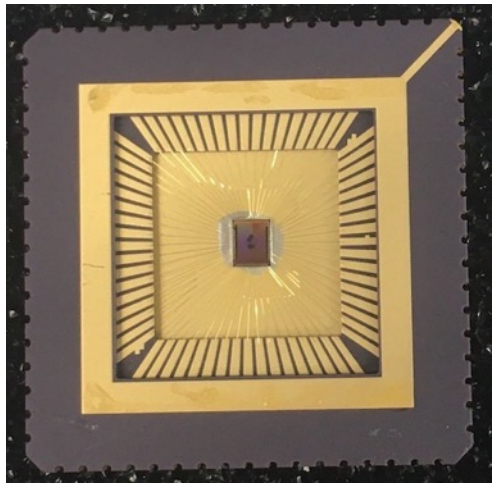


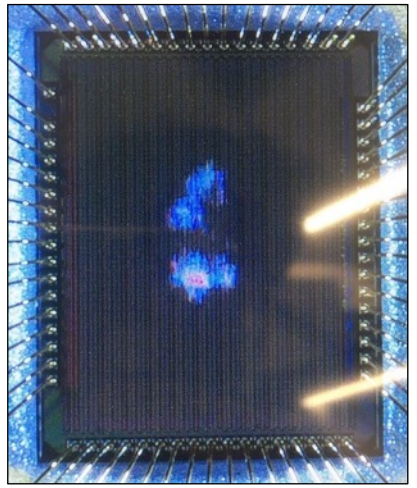
Snappy Decompression Xcel

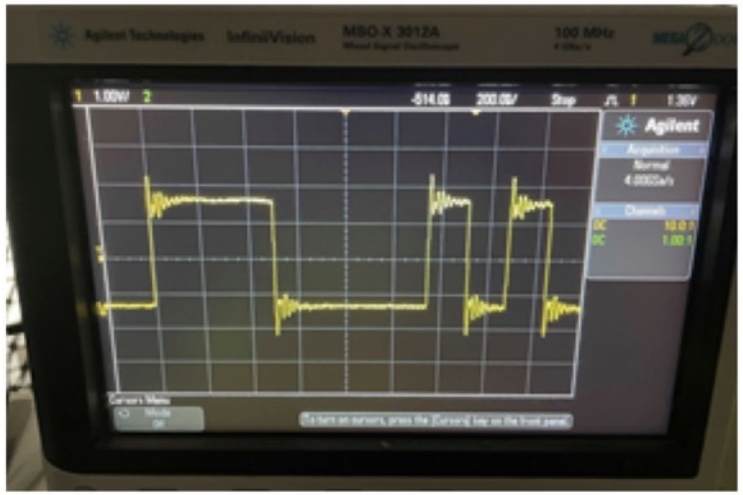
ECE 6745 Alumni Chip 1 & 2 (2020/2021)

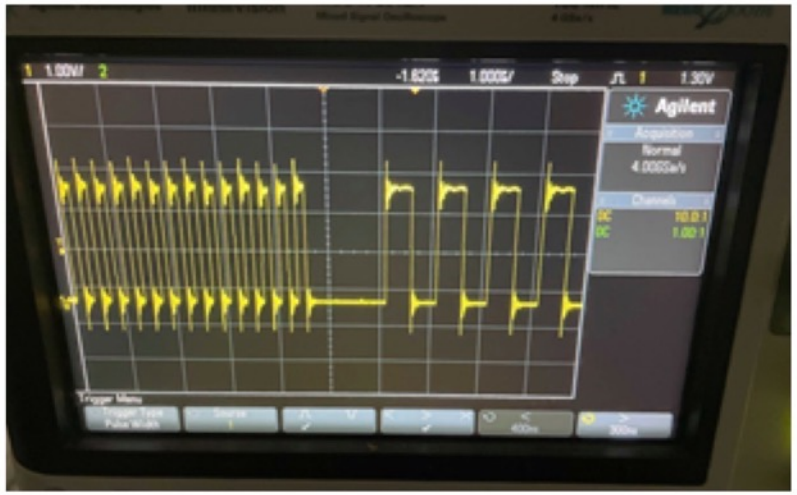
- Four undergraduates → MEng
- 2x2.5mm in TSMC 180nm
- SPI interface, floating-point ALU
- Synthesizable digital clock gen
- Chip 1 had hold time violation
- Chip 2 fully functional





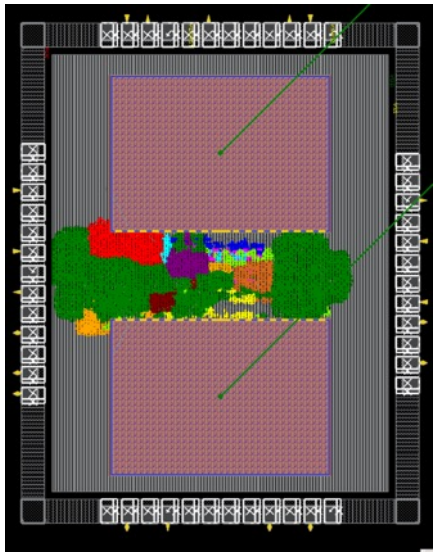


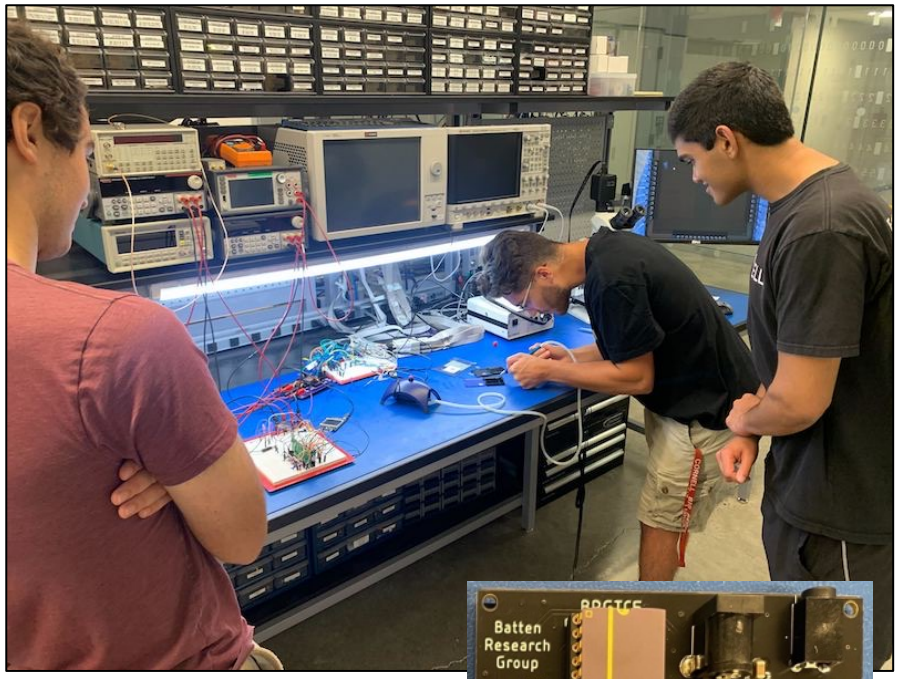


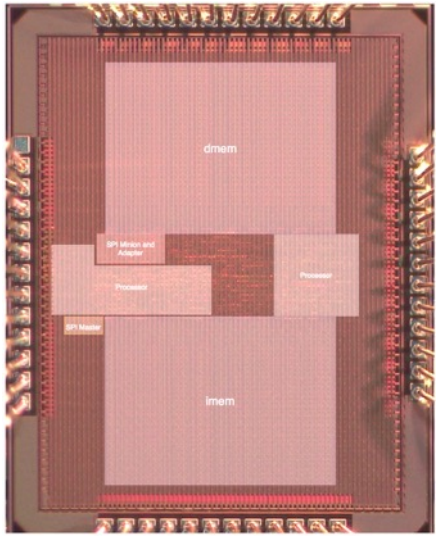


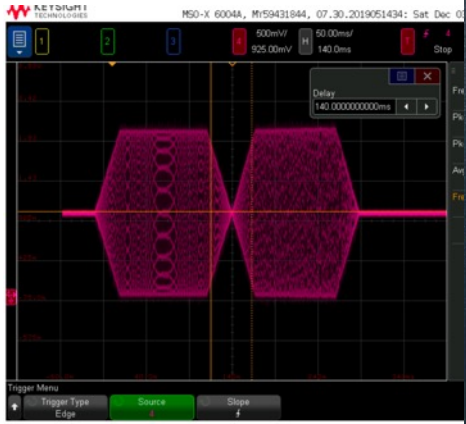
ECE 6745 Alumni Chip 3 (2021/2022)

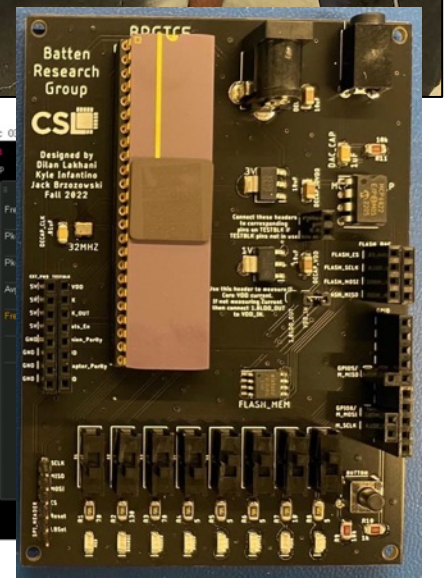
- Three undergraduates → MEng
- 2x2.5mm in TSMC 180nm
- RISC-V RV32IM micro-controller
- 16KB instruction SRAM
- 16KB data SRAM
- Low power sleep mode
- SPI interface for configuration and for loading programs
- SPI master used to control DAC for audio synthesis
- Custom evaluation board





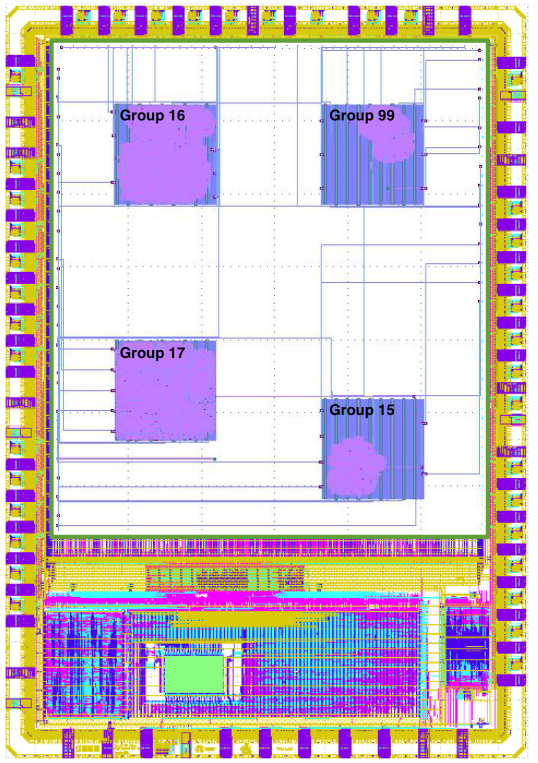


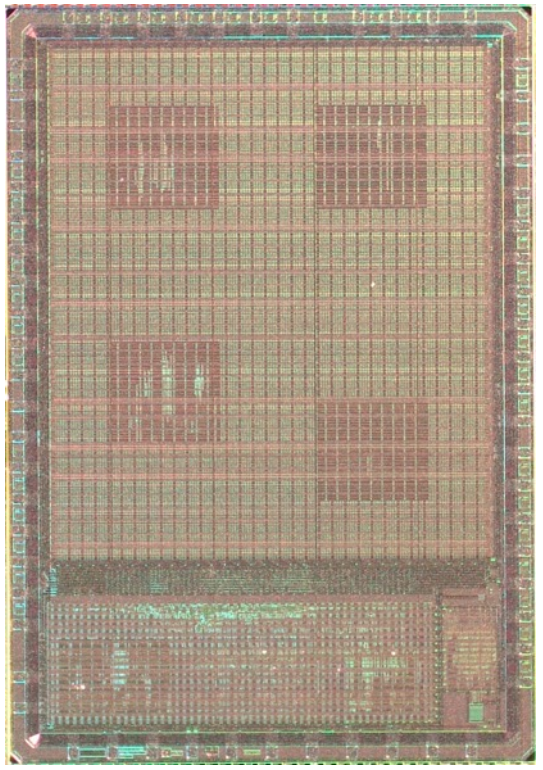


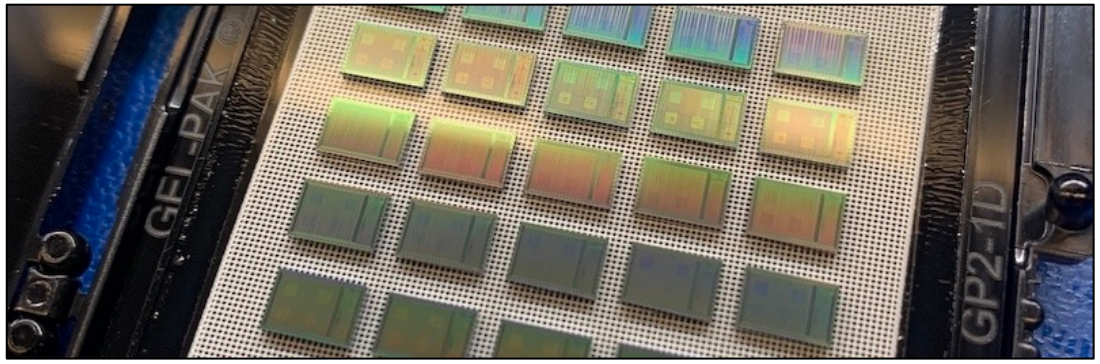


ECE 6745 Tape-Out Option (Spring 2022)

- First teaching tapeout in 20+ years
  - SkyWater 130nm through efabless
  - Taped out using completely open-source EDA tools (Icarus Verilog, Yosys, OpenROAD)
- 15 students in four groups
  - CRC32 checksum unit implemented using C++ high-level synthesis tools
  - Latency insensitive synthesizable memory implemented in PyMTL3
  - 2x2 systolic array multiplier implemented in SystemVerilog
  - Greatest common divisor unit implemented in SystemVerilog
  - Each unit included dedicated SPI interface

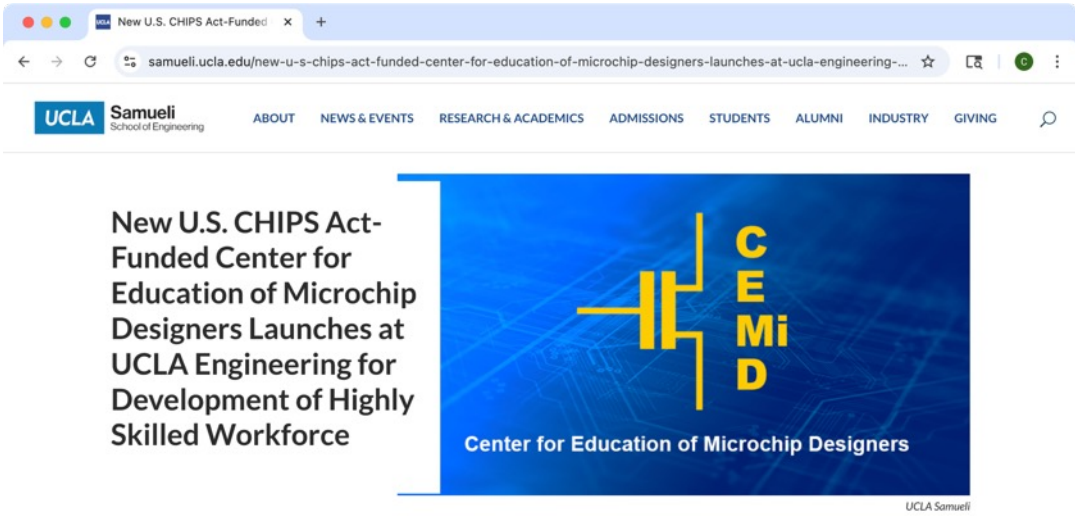


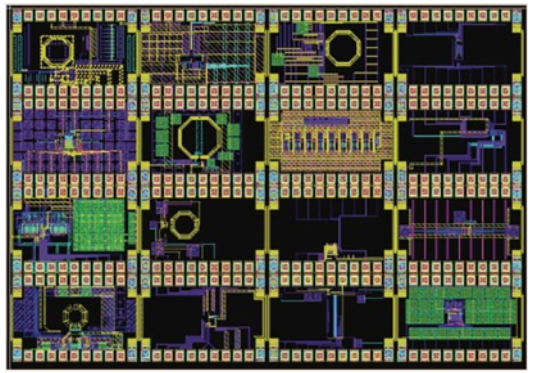


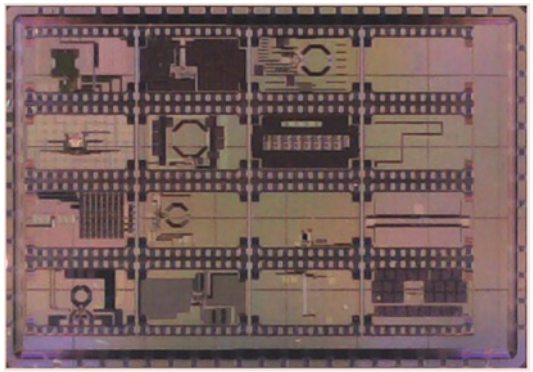


ECE 6745 Tape-Out Redesign (Spring 2026)

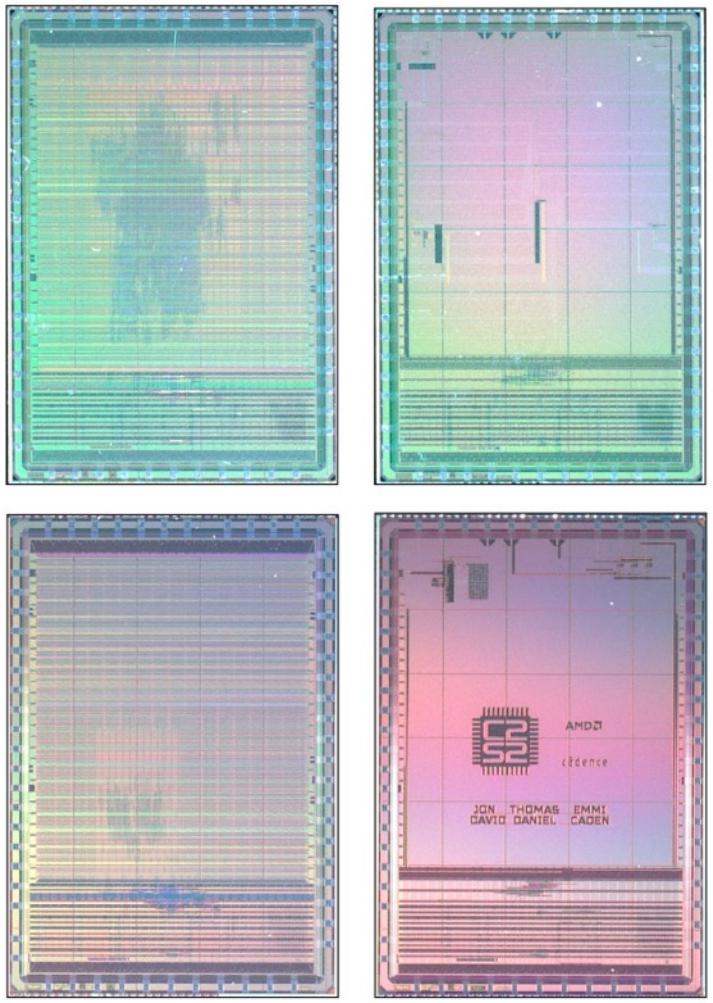
- Leverage several recent trends to combine the best of tape-out and tape-in courses
  - Several recent undergraduate tapeouts at Cornell
  - Recent reclassification of TSMC 180nm as EAR99
  - Center for Education of Microchip Designers at UCLA will provide funding and shared expertise
- Tape-Out Project
  - Groups of 2-3 students tape-out 1x1mm digital ASIC on TSMC 180nm
  - Commercial tools, standard-cells
  - Students test their chips in the fall
- Tape-In Project
  - Groups of 2-3 students tape-in much larger and more complex digital ASIC using TSMC 180nm
  - Commercial tools, standard-cells, SRAM compiler







Experiential Learning for Semiconductor Chip Design through Student-Led Project Teams



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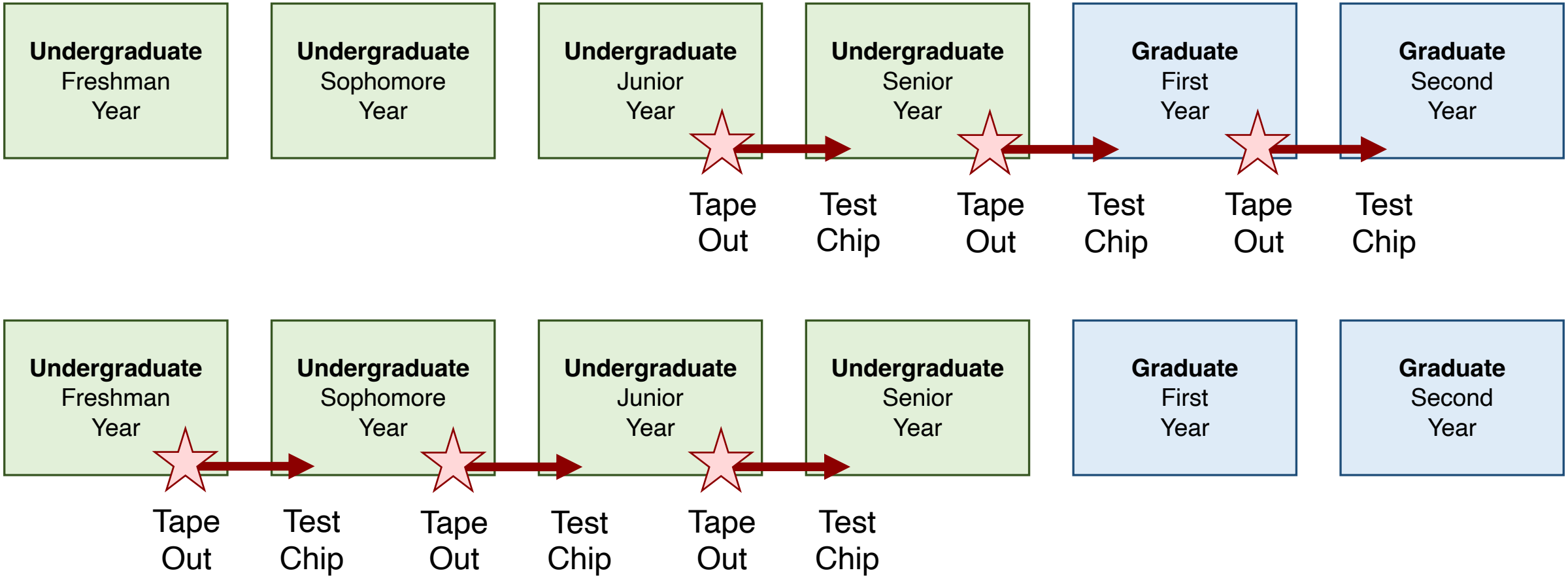
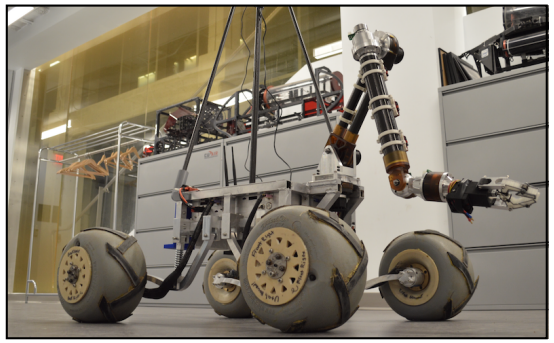


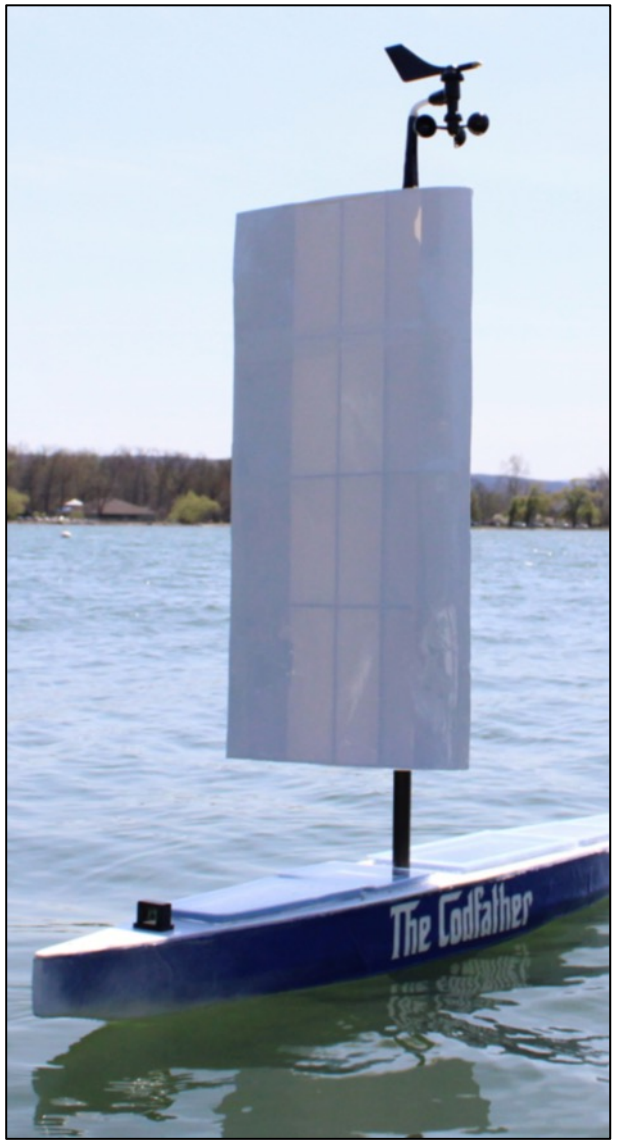
How can we get students experiencing the joy of chip design first-hand far earlier in their time as undergraduate students?

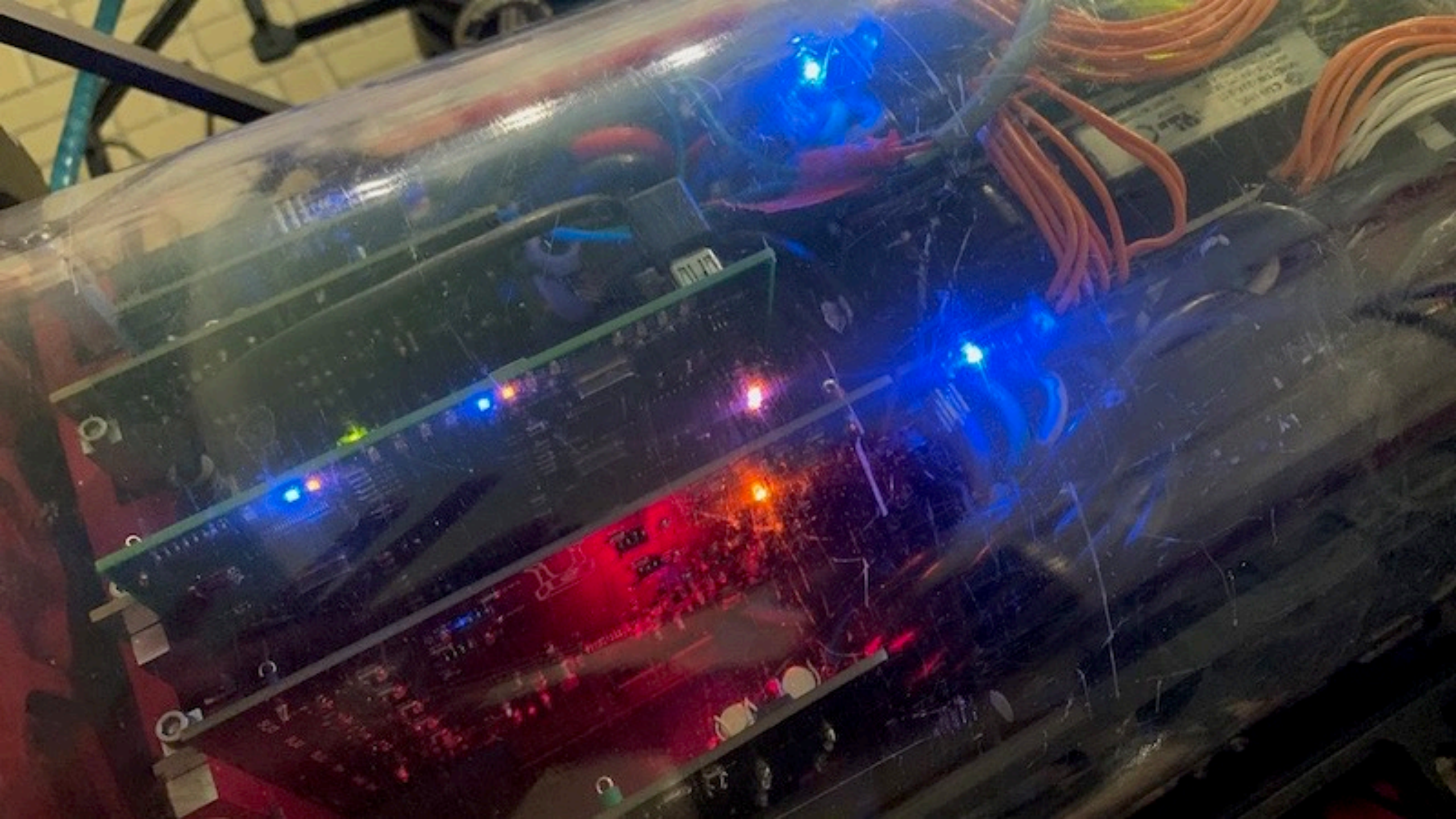
Is chip design really too hard for these younger students?

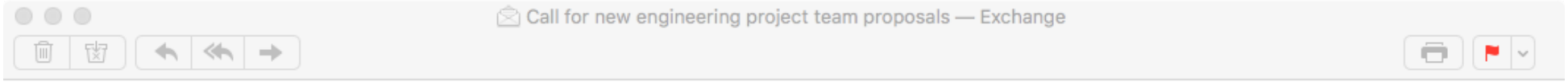
Cornell Student-Led Project Teams



1400 students on 30 teams
14 engineering majors







Associate Dean for Undergraduate Programs
Call for new engineering project team proposals
To: ENGRFACULTY-L, ENGRFACULTYINCSANDBEE-L, ENGRACADEMICS-L, Cc: Lauren Stulgis,
Reply-To: Associate Dean for Undergraduate Programs

Archive - Exchange February 22, 2022 at 12:08 PM
Details

Colleagues,

Through a generous donor gift creating the **Shen Fund for Social Impact** we have the opportunity to fund multiple new engineering project teams. This program is designed to bring together new student teams under a faculty member's mentorship to address significant social challenges through novel and/or advanced engineering solutions. Falling under the Project Team Umbrella, the program will fund up to three new teams per year, with each supported for a three-year period at $30K/yr. The teams will also be provided space and support to design and implement these projects.

Proposals may be submitted by either faculty looking to guide a group of students, or by students who will engage with a faculty member to form the teams.

Attached to this e-mail are three documents:

- **Shen Fund FAQ Sp22.pdf:** More fully describes the nature of the projects and the goals of the program (also copied to the e-mail below).
- **Shen Fund Proposal Template Sp22.docx:** Short project proposal form.
- **Shen Funded Projects Summary_Sp22.pdf:** A summary document of a currently funded teams.

The ideal project will likely develop through discussions with Lauren Stulgis (as director of the project teams) and me. Feel free to reach out to us with rough ideas and concepts and we can help to try to develop a viable proposal.

Proposals will be considered as they arrive, with discussions to strengthen each within the program constraints. The initial application is a simple document identifying the primary goals, technical challenges and plans, timeline and budget, and currently engaged personnel.

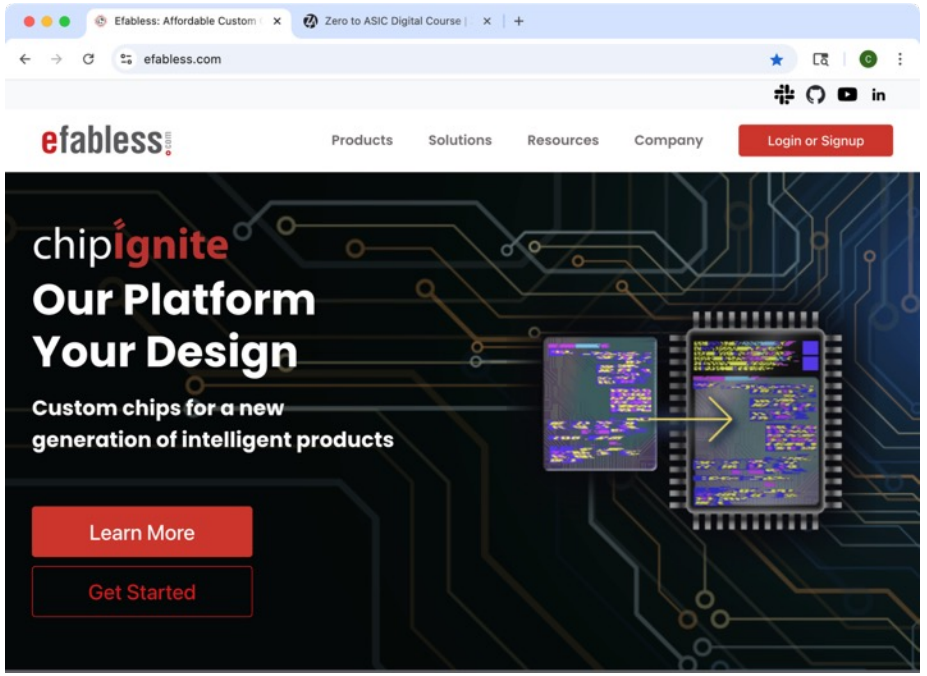
Proposals must be uploaded directly to Box by email to: Proposa.zeuyhp9wqg5p8teo@u.box.com. The first round of decisions will be made based on submissions received by **11:59pm on Sunday, March 13, 2022.**

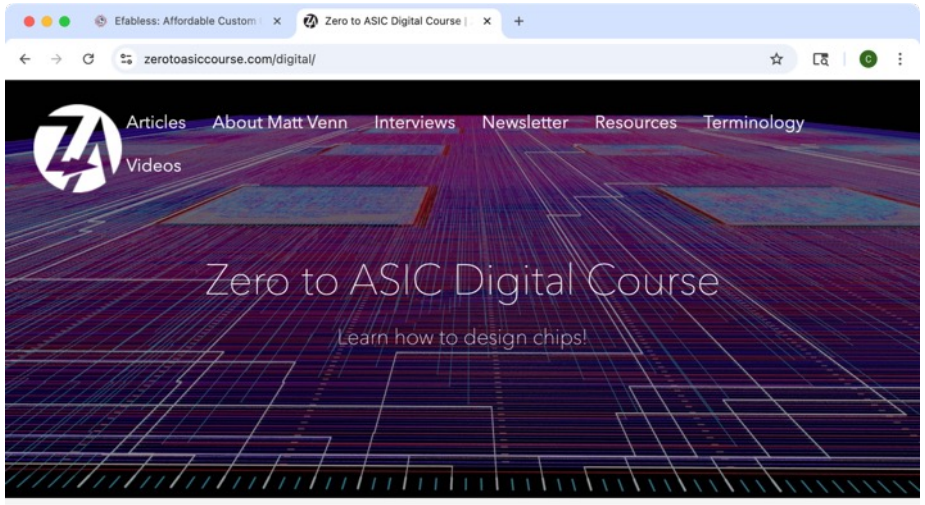
Again, please feel free to contact me or Lauren Stulgis with any questions or to discuss potential projects.

Prof. Alan Zehnder
Associate Dean for Undergraduate Programs
177 Rhodes Hall
Phone: (607) 255-9181
email: eng_ugdean@cornell.edu

Open-Source Chip Design Path-Finding (2022)

Aidan McNay
Cornell ECE, BS'24





chipIgnite Shuttle

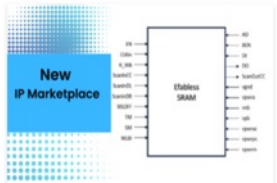
Submit your design by April 21 for the next fab run!

Learn More

Keyword Spotting

Transform your ML algorithm into analog-rich SoC

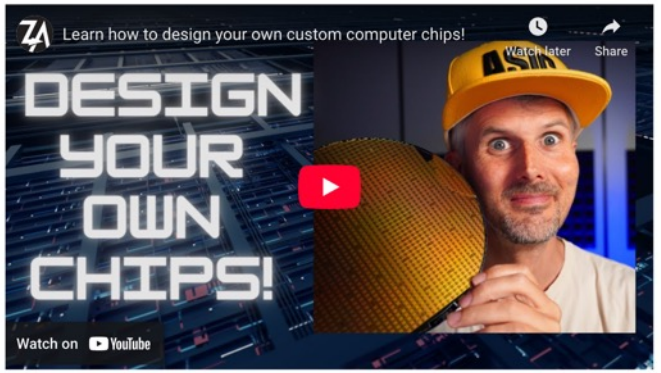
Learn More



New Efabless Marketplace

Free & Commercial IP available now with other tech resources

Learn More



Digital ticket options

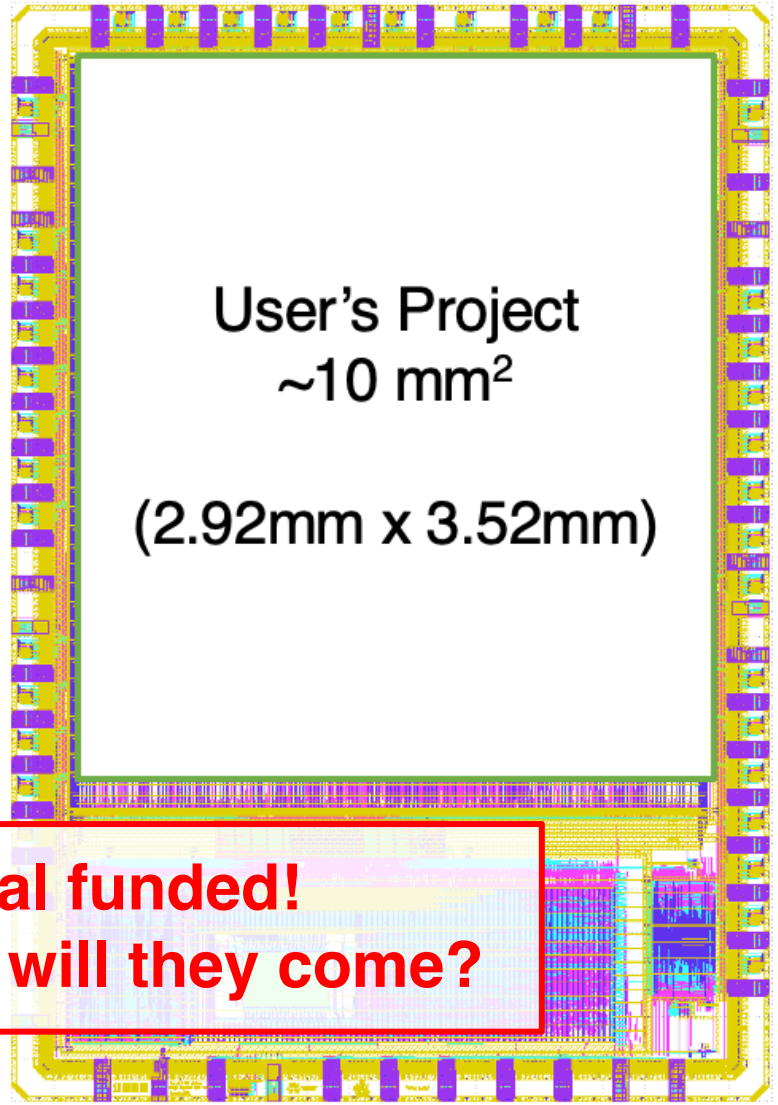
	Silicon	Boron	Arsenic
	Buy for $650	Buy for $950	POA
Access to 6 hours recorded video	✓	✓	✓

Related

- Newsletter
- Resources
- Zero to ASIC Analog Course
- Review of 2024 and aims for 2025
- Tiny Tapeout 9
- My analog microelectronics journey
- Review of 2023 and aims for 2024
- Tiny Tapeout 2 Silicon Is Alive!
- Tiny Tapeout 4
- Review of 2022 and aims for 2023
- Cloud Tools for ASIC Development

Cornell Custom Silicon Systems Project Team

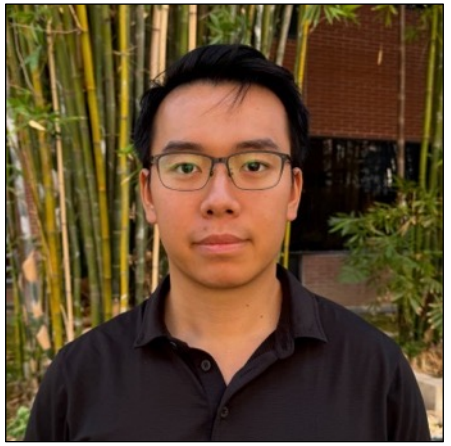
- Submitted proposal for student-led project team to tape-out multiple custom chips in SkyWater 130nm to implement a proof-of-concept system for a campus partner
  - Custom system-on-chip
  - Custom evaluation board
  - Custom software stack
- Team is made possible by leveraging emerging open-source chip desing ecosystem
  - Open RISC-V instruction set
  - Open-source VexRISCV micro-controller
  - Open-source OpenROAD chip flow
  - Open PDK for SkyWater 130nm
  - Efabless ChipIgnite program



Proposal funded!
If you build it will they come?

Bootstrapping the C2S2 Leadership Team

- Recruited Hunter Adams as a co-faculty advisor
- 60+ students attended online information session during summer 2022
- 40 students applied to be on the leadership team
- 7 students selected to lead team in its first year



Jon Ho
Cornell ECE, BS'23

Project Team Lead	Aidan McNay	Junior
Digital Subteam Lead	William Salcedo	Senior
Analog Subteam Lead	Jon Ho	Junior
Software Subteam Lead	Tanya Zhou	Junior
System Arch Subteam Lead Project Mgmt Subteam Lead	Chidera Wokonko	Senior
	Tomas Choi	Sophomore
	Vicky Le	Sophomore

"I have a deep interest in exploring the possibility of taping-out an analog/mixed-signals IC for C2S2. The ideas presented by Prof. Adams are exciting but appear to require analog front-ends. I would love to take on the challenge of learning how to tape-out an analog chip with the Skywater PDK and help kickstart an analog subteam, which would be an opportunity for me to develop as a leader; I believe that in doing so, C2S2 can also serve an even greater number of undergraduates."

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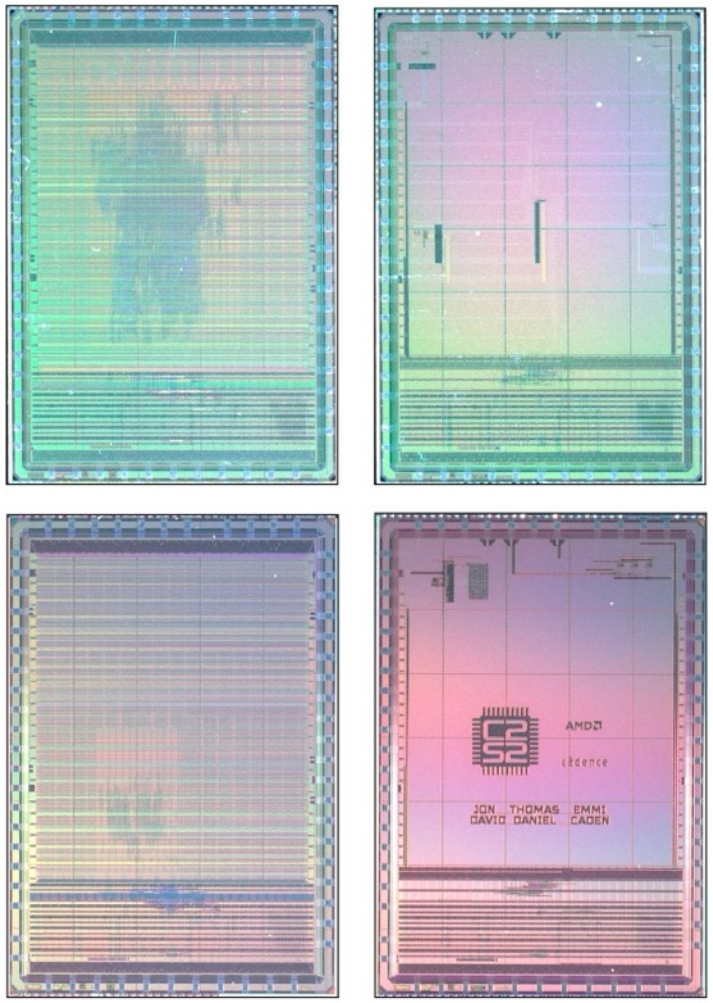

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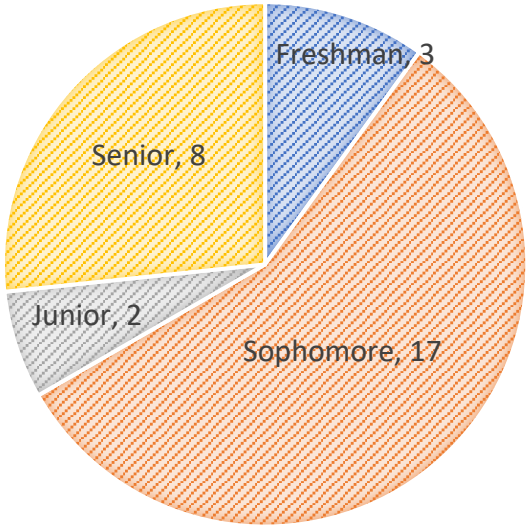
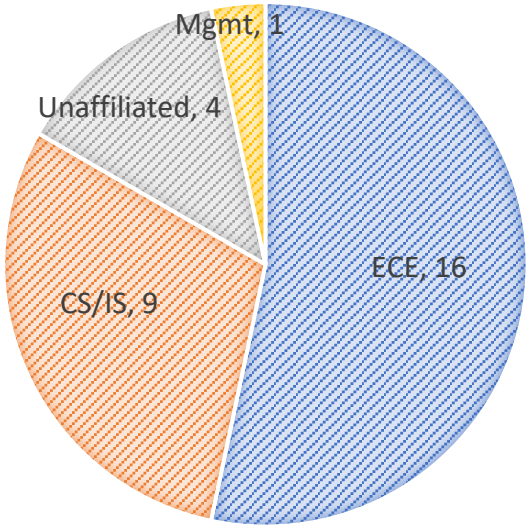
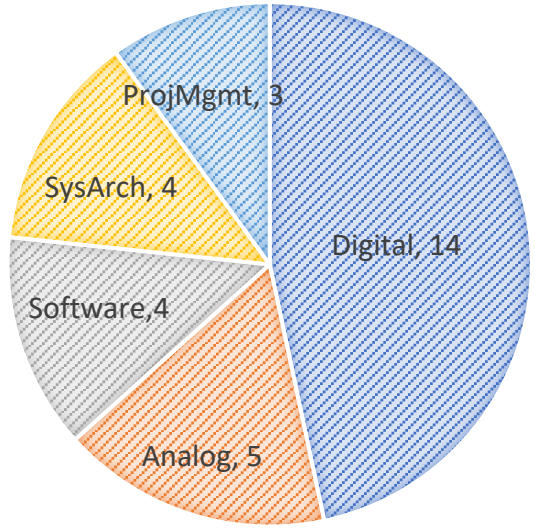
C2S2 Year 1 Team

- Recruited a total of 30 members spanning all levels and four majors
- Year 1 focus
  - Ramping up infrastructure
  - Taping out two chips

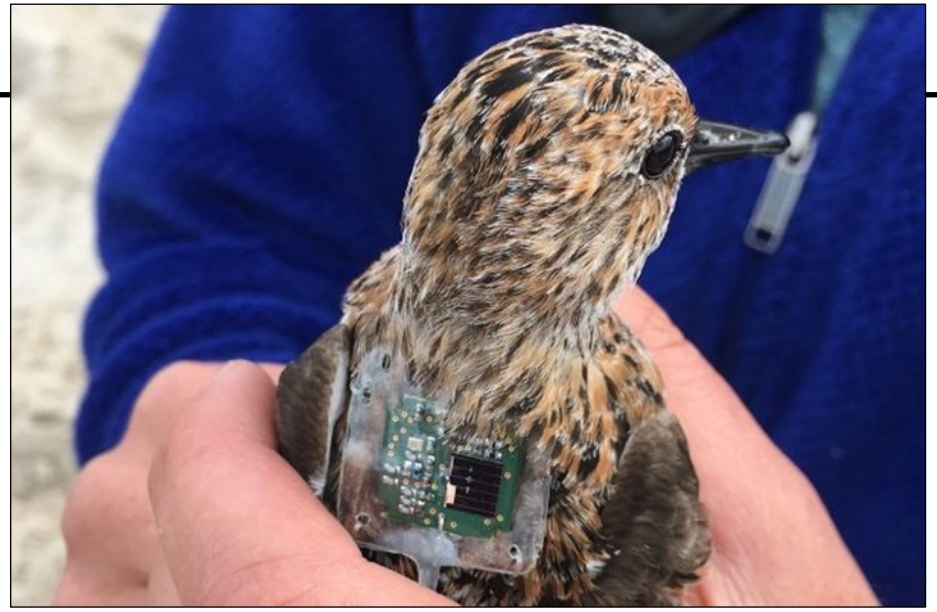


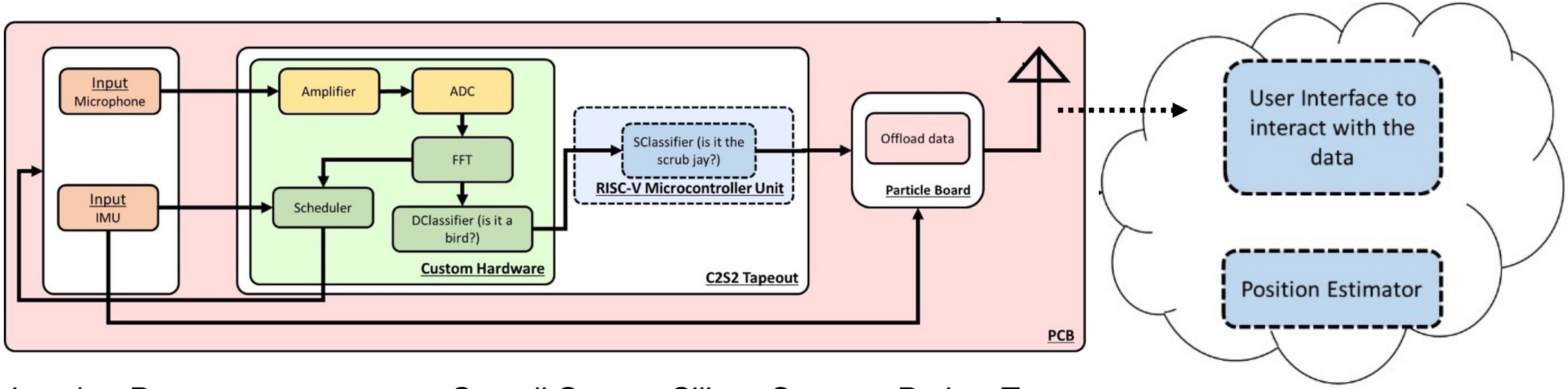




Finding a Campus Partner

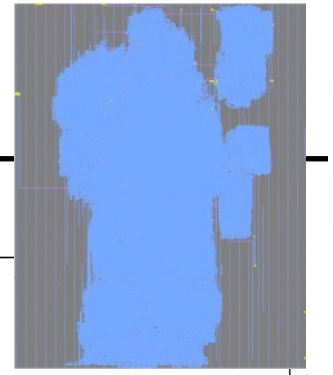
- Reached out to 30+ groups to find a campus partner to provide a problem specification that can be addressed through custom system-on-chip
- Team settled on working with Christopher Tarango, PhD student in the Lab of Ornithology
- Exploring a proof-of-concept ultra-low-power bird call recording system for scrub jays

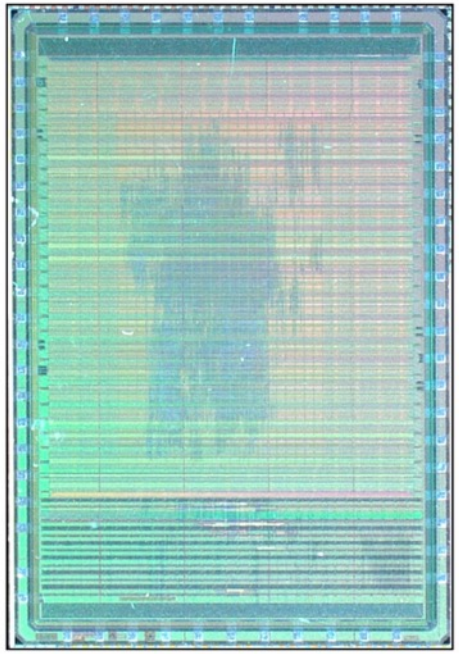


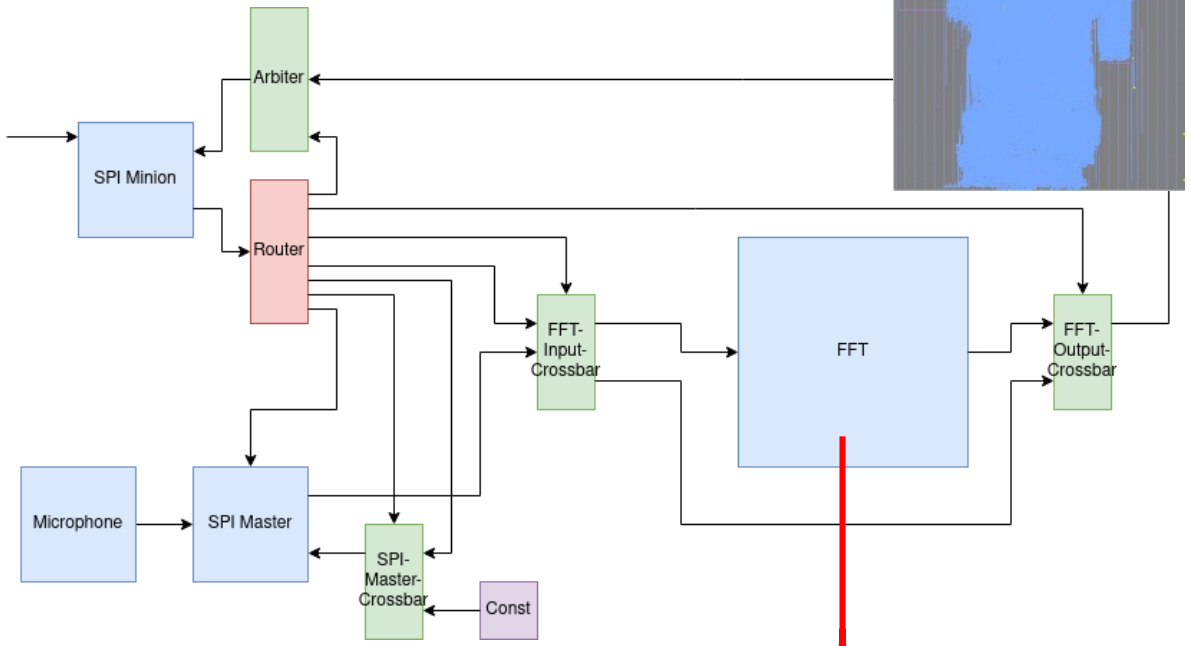


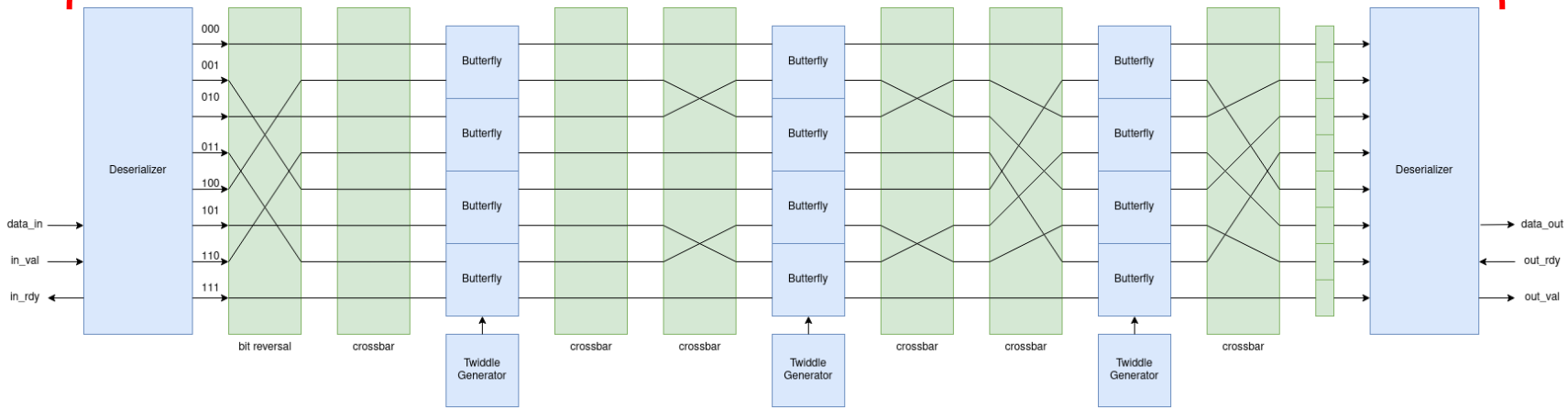
C2S2 Year 1 Digital Tape-Out

- FFT hardware unit for analyzing audio data
- SPI interface for testing
- SPI interface for microphone
- Python-based PyMTL testing framework
- All digital design completed using only open-source EDA tools



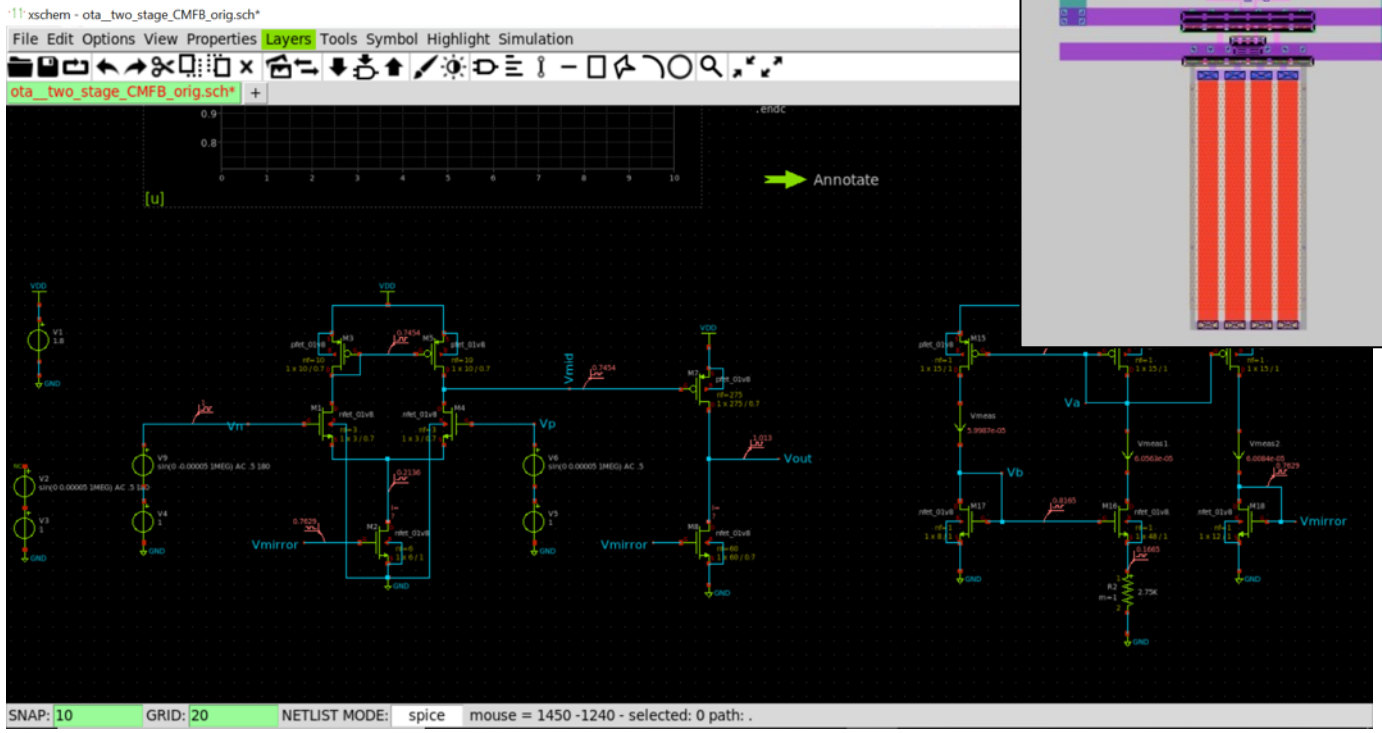




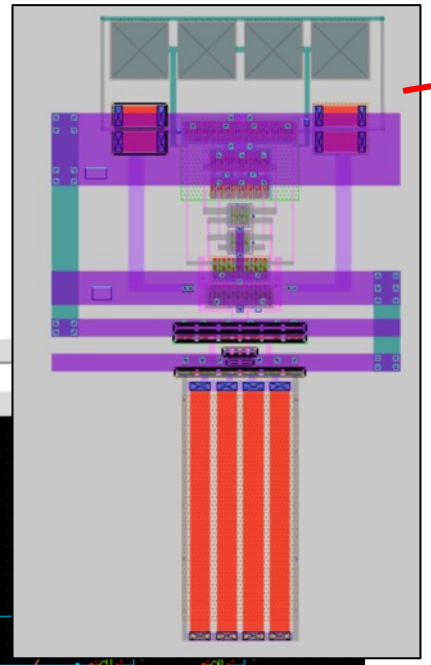


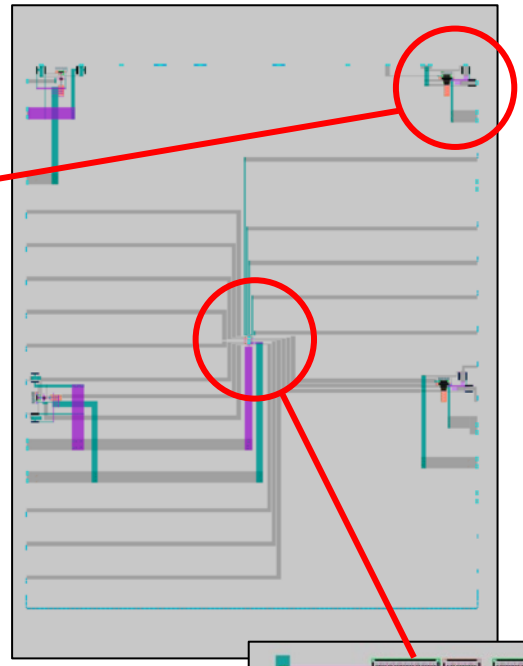
C2S2 Year 1 Analog Tape-Out

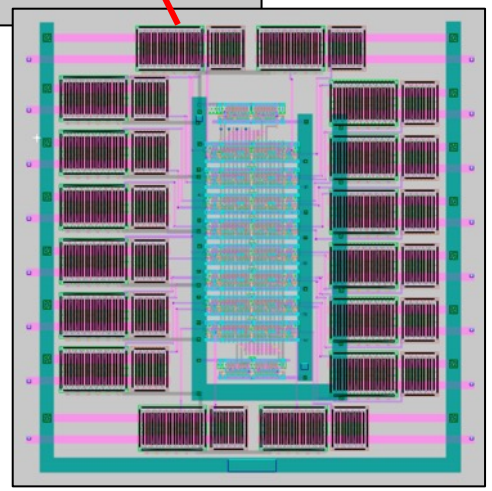
- Two different versions of an op-amp along with an analog mux
- All analog design completed using only open-source EDA tools



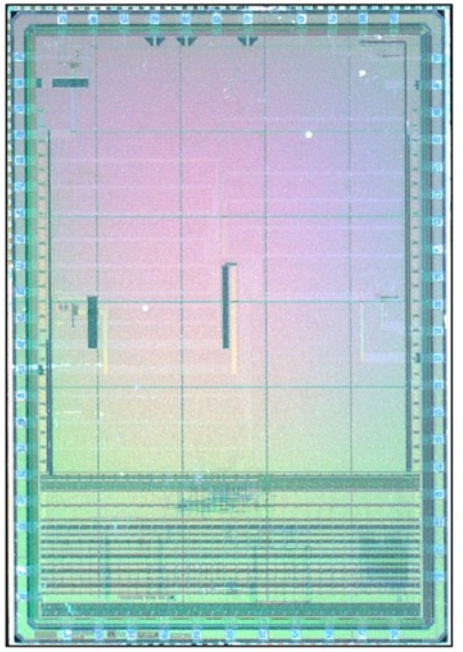
Op-Amp



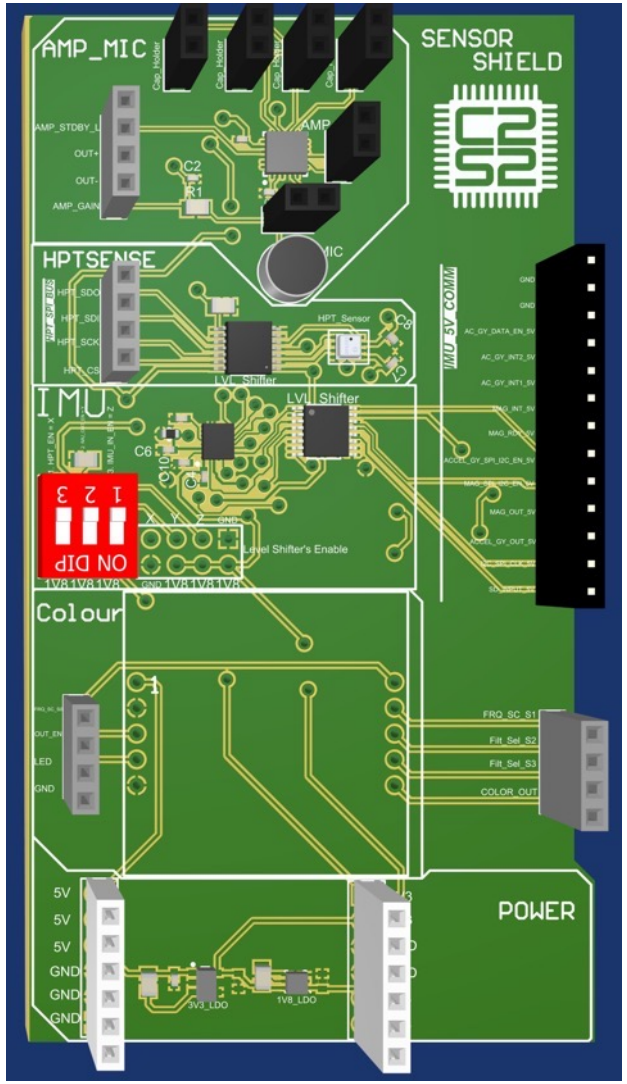


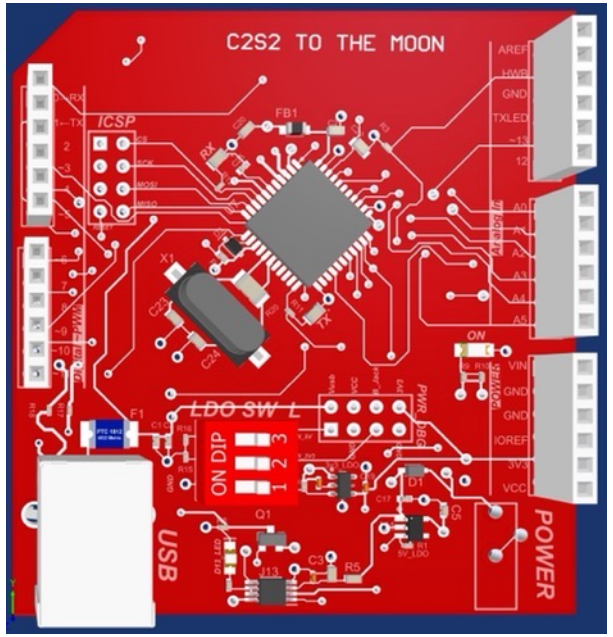


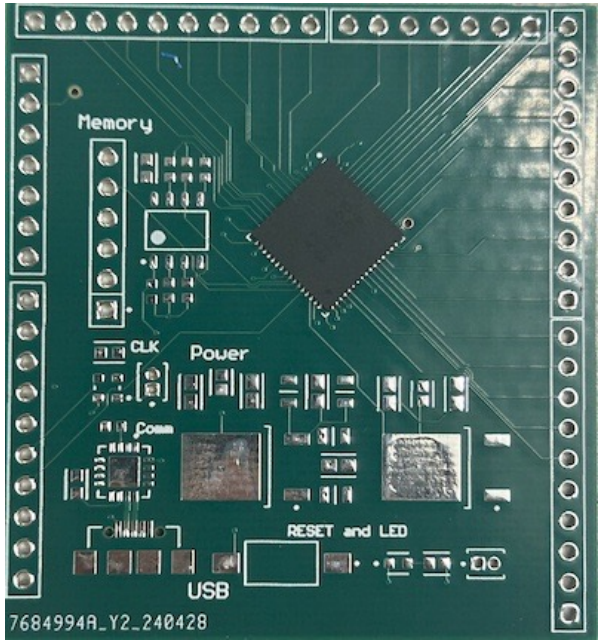
Analog Mux

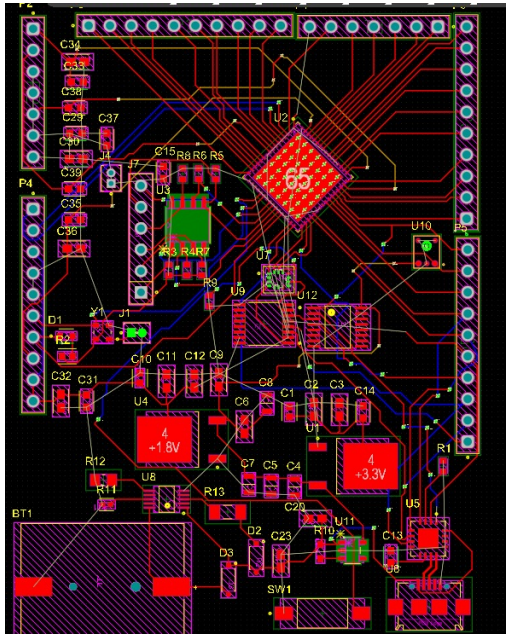


C2S2 Software and System Architecture







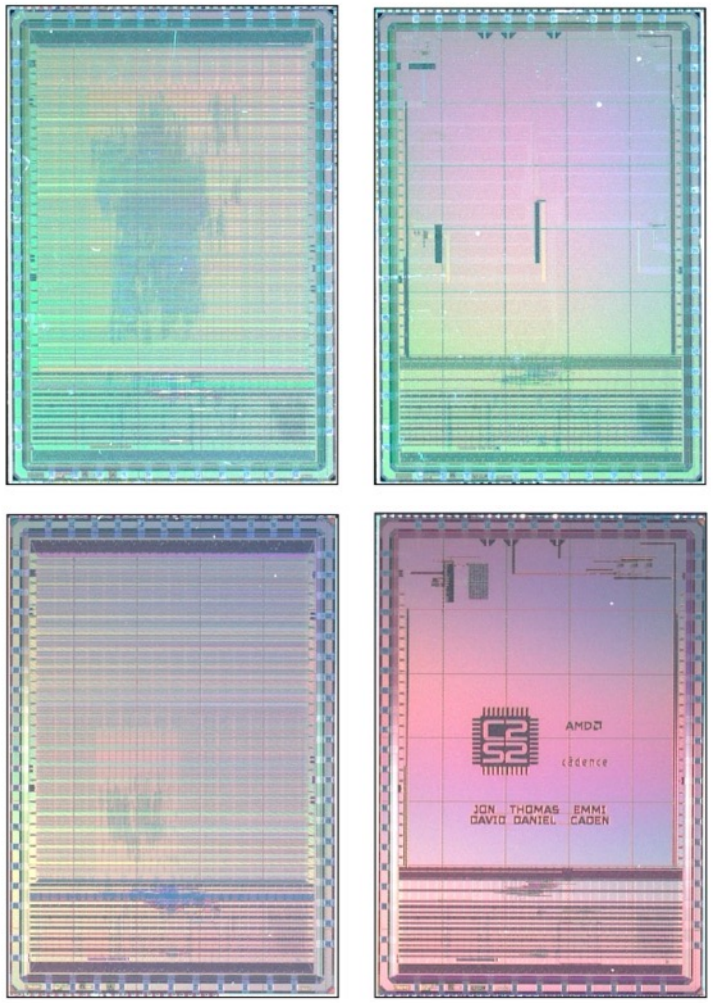


- Developing various custom boards to gain experience towards building proof-of-concept system
- Developing embedded software to run on RISC-V core and/or on-board microcontroller

C2S2 Community

- Coding sprints and hack-a-thons
- Social events like bowling and movie nights
- Outreach events with local high schools
- Field trip to the Albany NanoTech Complex

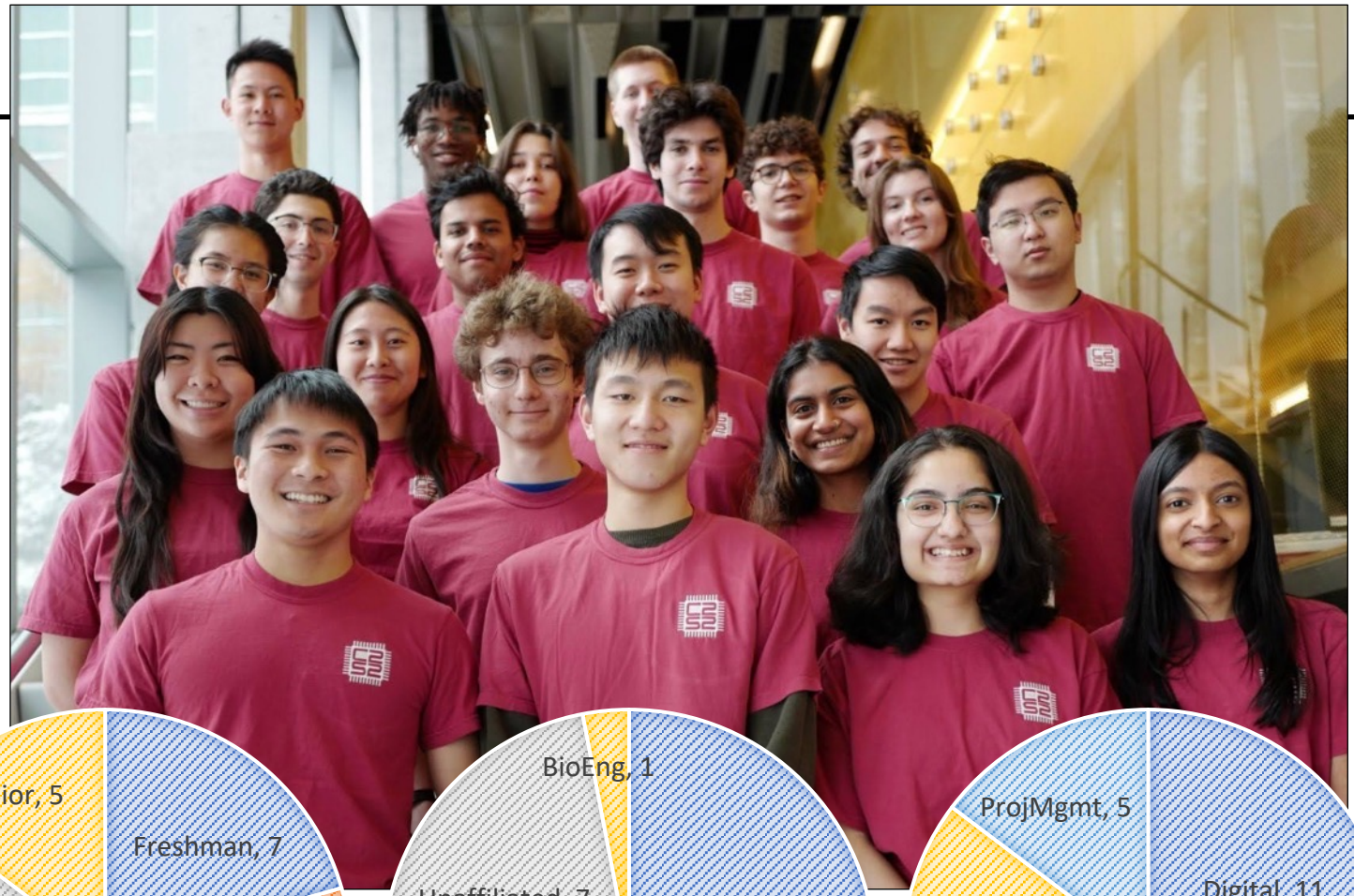
Experiential Learning for Semiconductor Chip Design through Student-Led Project Teams

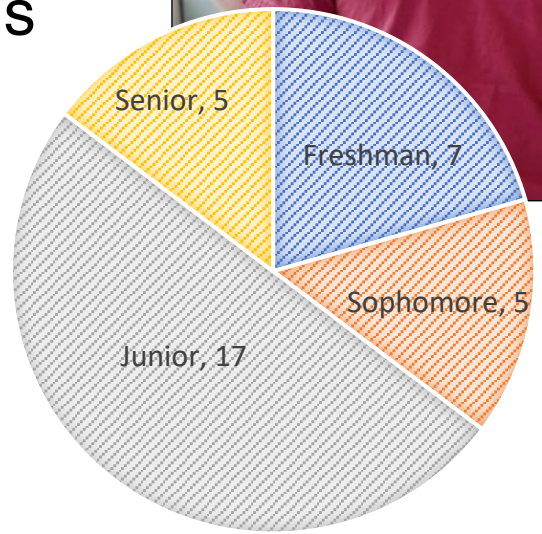


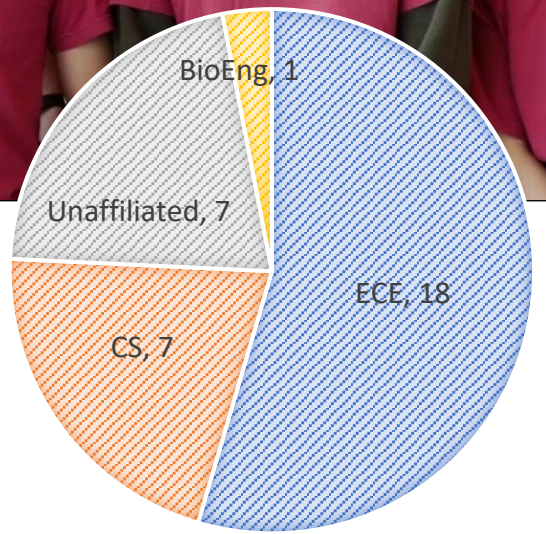
- Cornell Tape-Out Courses
- C2S2 Founding
- C2S2 Year 1: Campus Partner & Two Chips
- C2S2 Year 2: Two More SkyWater 130nm Chips
- C2S2 Year 3: Pivot to TSMC 180nm
- C2S2 Lessons Learned

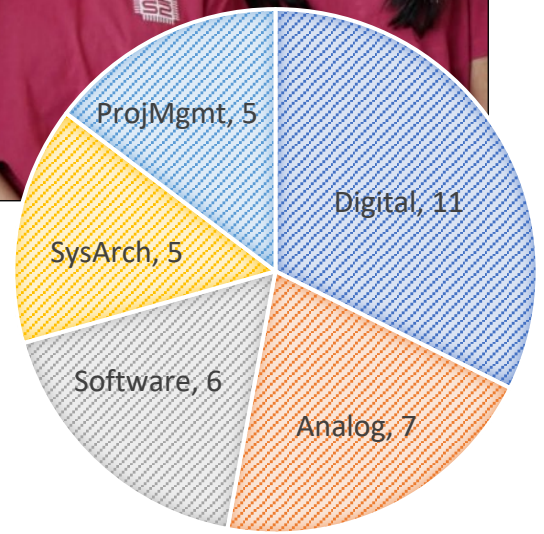
C2S2 Year 2 Team

- 34 members spanning all levels and four majors
  - 17 returning members
  - 17 new members
- Year 2 focus
  - Testing year 1 chips
  - Crystallizing specifications from campus partner
  - Exploring sponsorships
  - Taping out new digital and analog chips

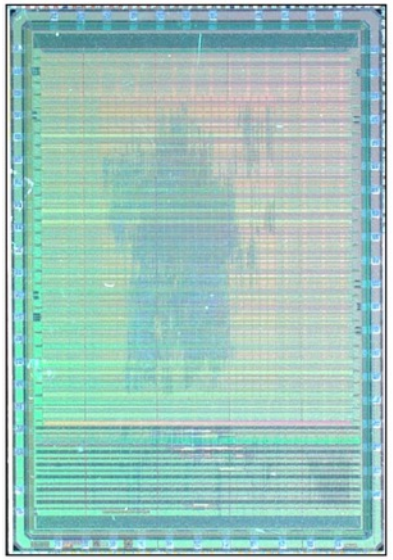


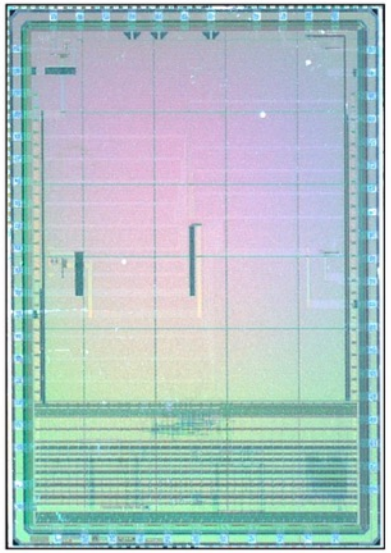






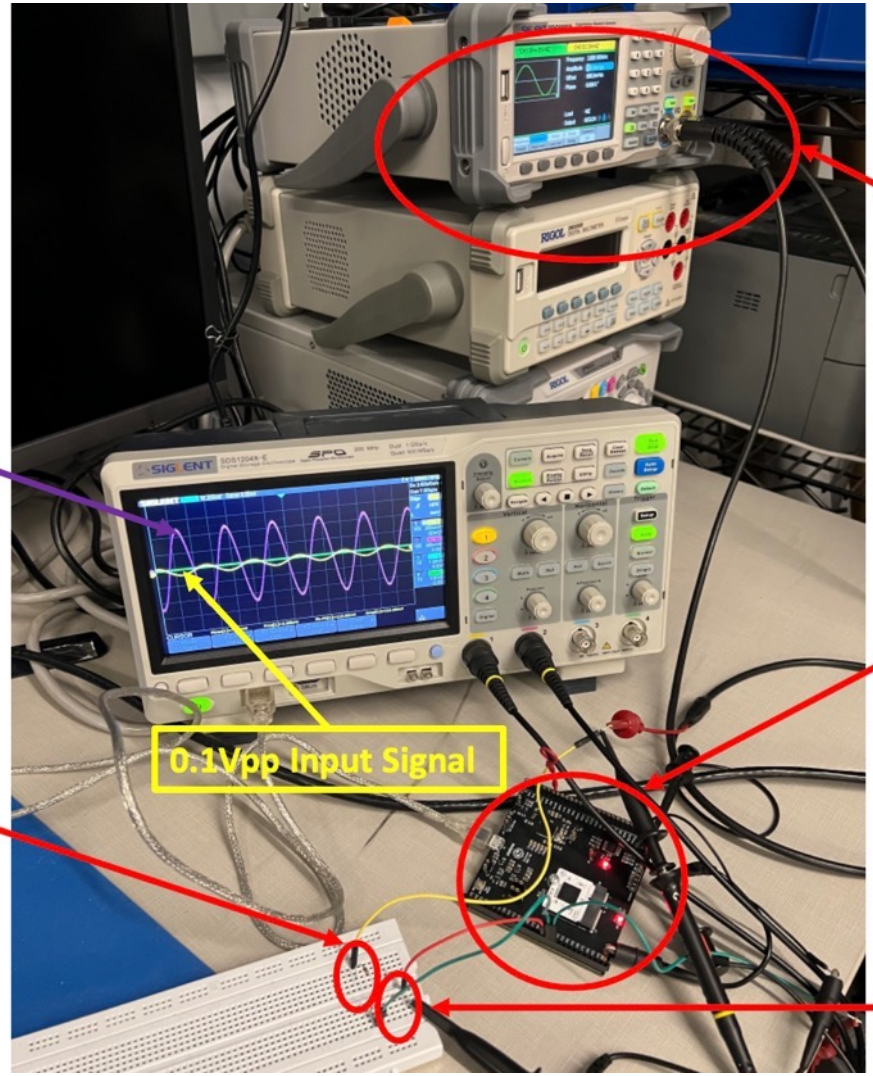
Testing Year 1 Chips





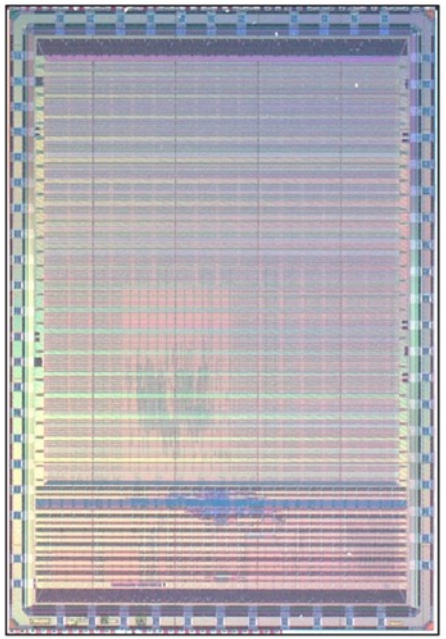
Five-month turn around time

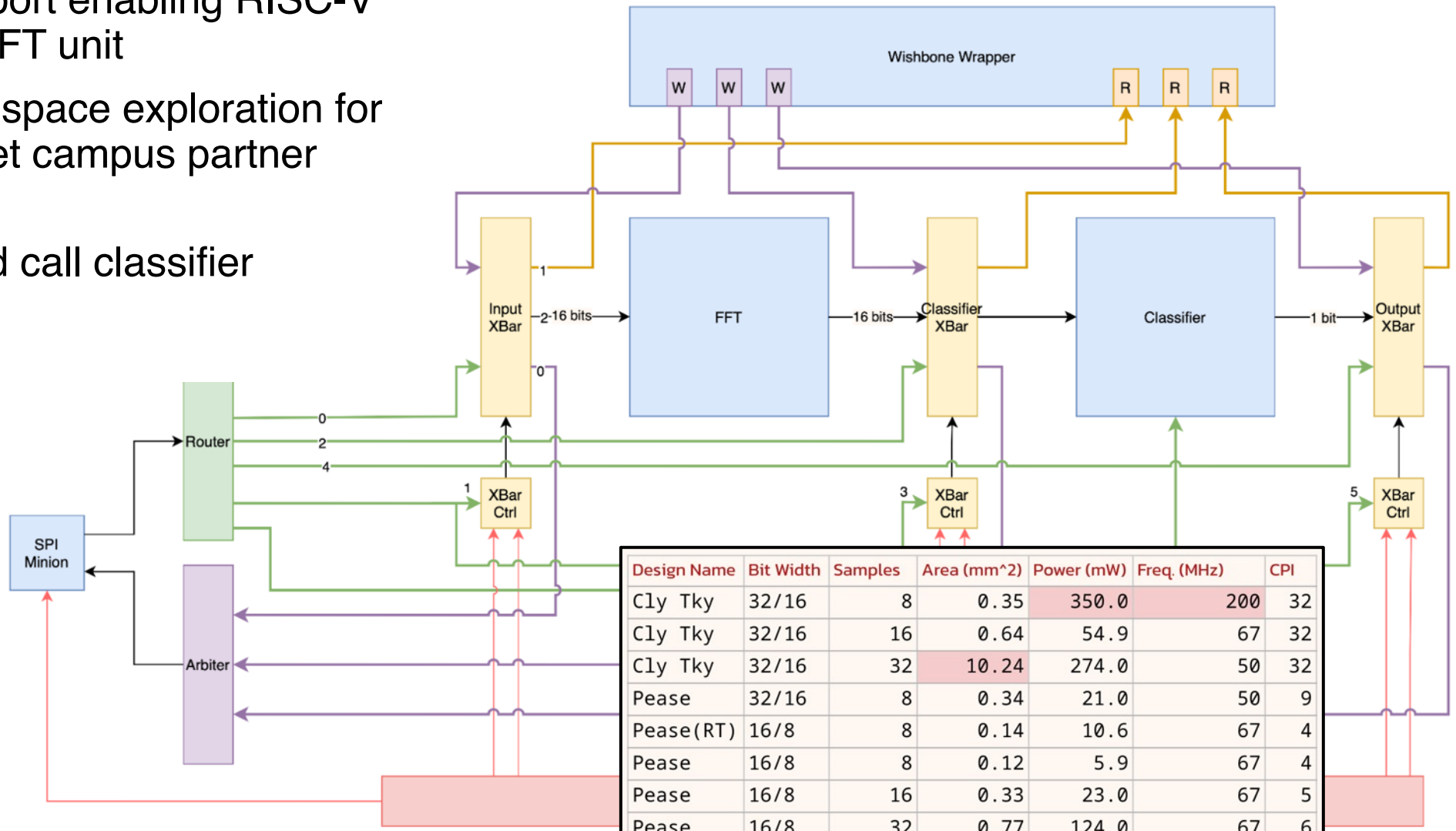
Both chips fully functional



C2S2 Year 2 Digital Tape-Out

- Added wishbone support enabling RISC-V core to interact with FFT unit
- More rigorous design space exploration for FFT unit to better meet campus partner specifications
- Added lightweight bird call classifier

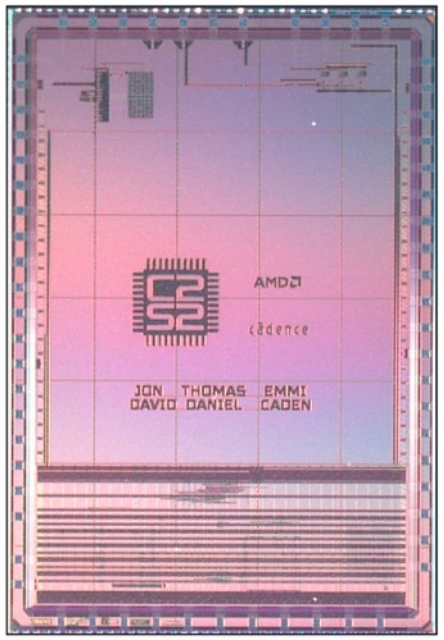




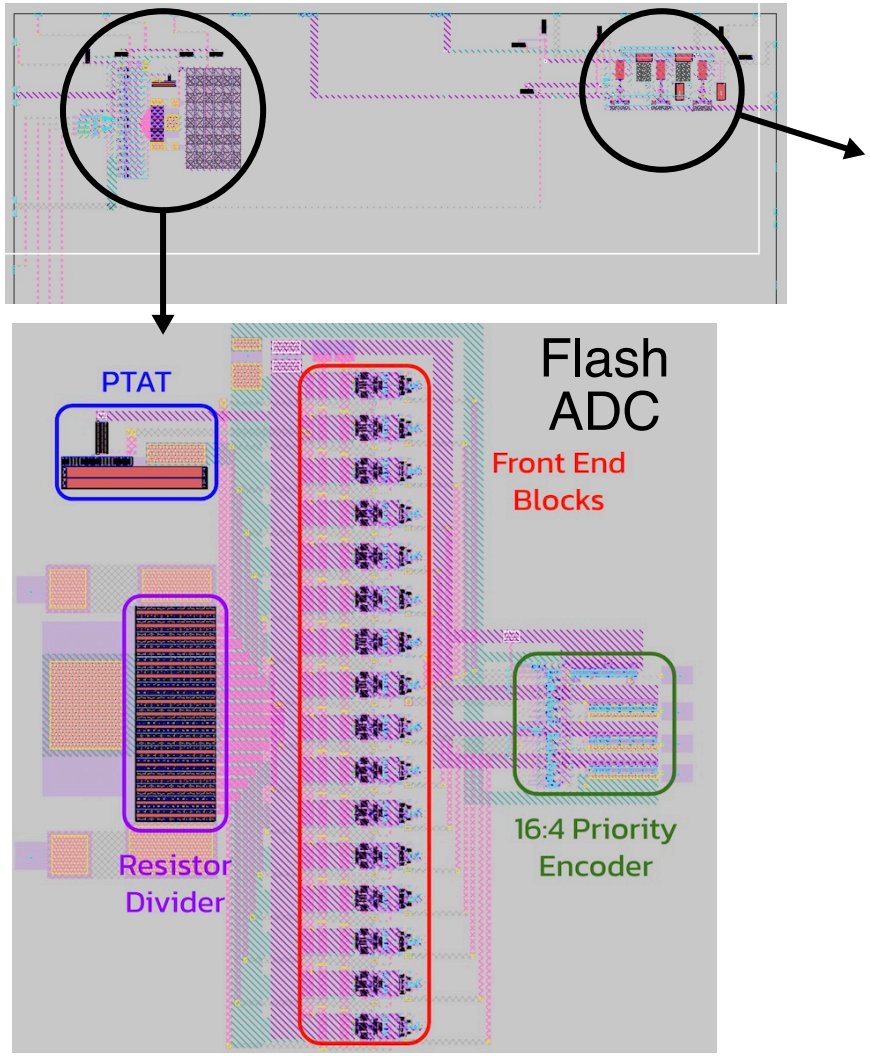
Design Name	Bit Width	Samples	Area (mm^2)	Power (mW)	Freq. (MHz)	CPI
Cly Tky	32/16	8	0.35	350.0	200	32
Cly Tky	32/16	16	0.64	54.9	67	32
Cly Tky	32/16	32	10.24	274.0	50	32
Pease	32/16	8	0.34	21.0	50	9
Pease(RT)	16/8	8	0.14	10.6	67	4
Pease	16/8	8	0.12	5.9	67	4
Pease	16/8	16	0.33	23.0	67	5
Pease	16/8	32	0.77	124.0	67	6

C2S2 Year 2 Analog Tape-Out

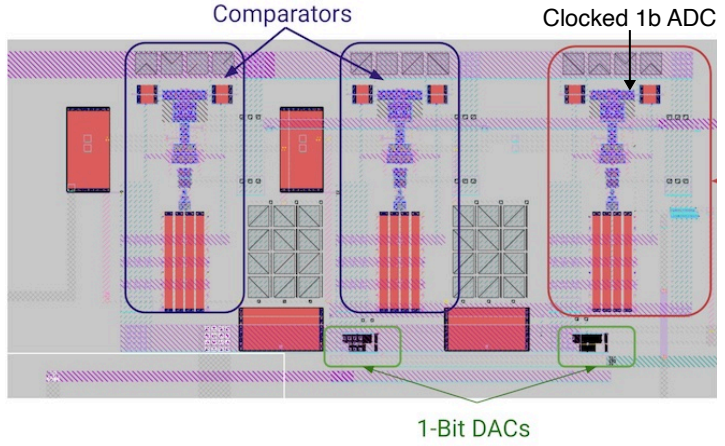
- Exploring ADCs for eventual integration with digital components for complete SoC
- Reused op-amp from year 1 tapeout as building block
- Implemented flash ADC and delta-sigma modulator

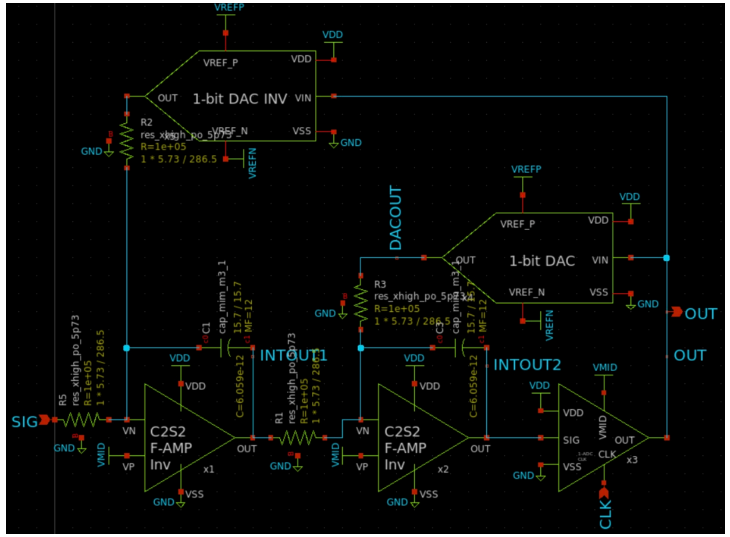


Learned how to add chip art!



Delta-Sigma Modulator





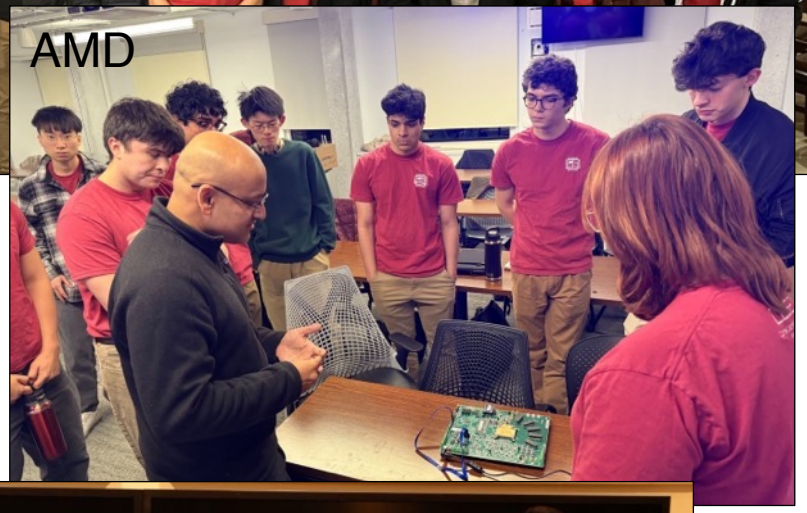
C2S2 External Sponsors

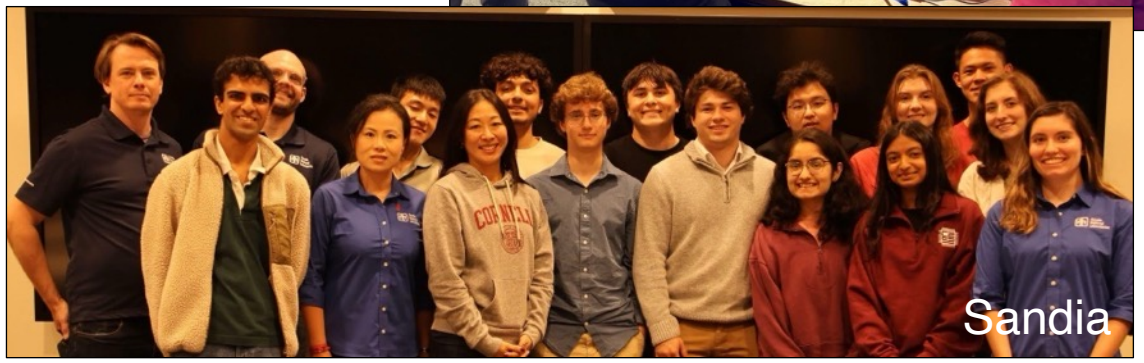
AMD

cadence®

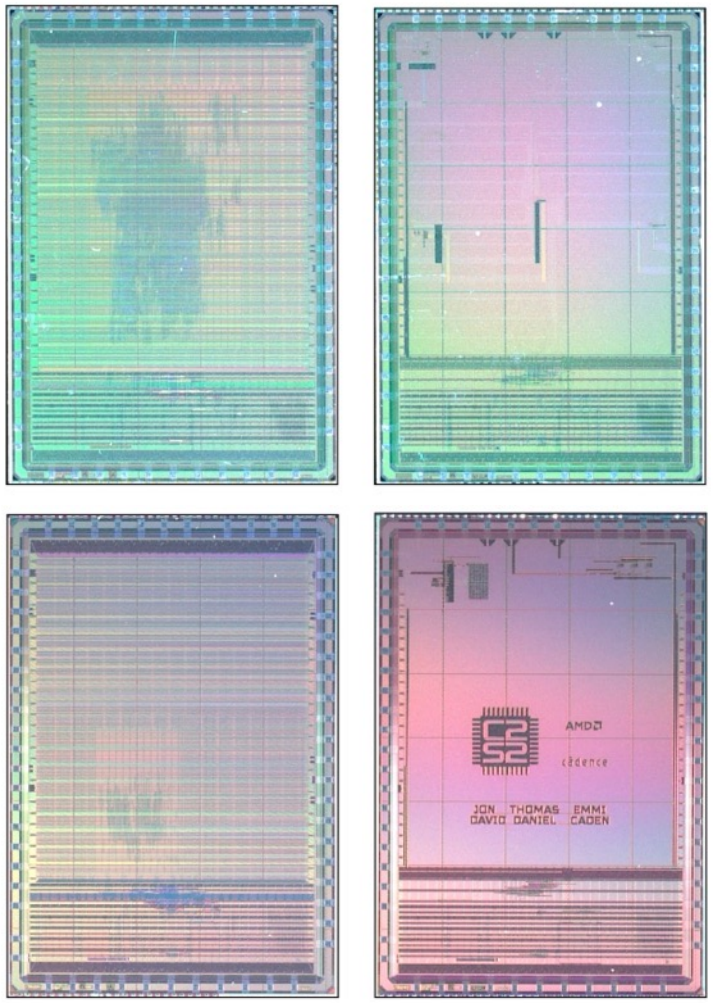
Sandia National Laboratories

NORDTECH
Northeast Regional Defense Technology Hub





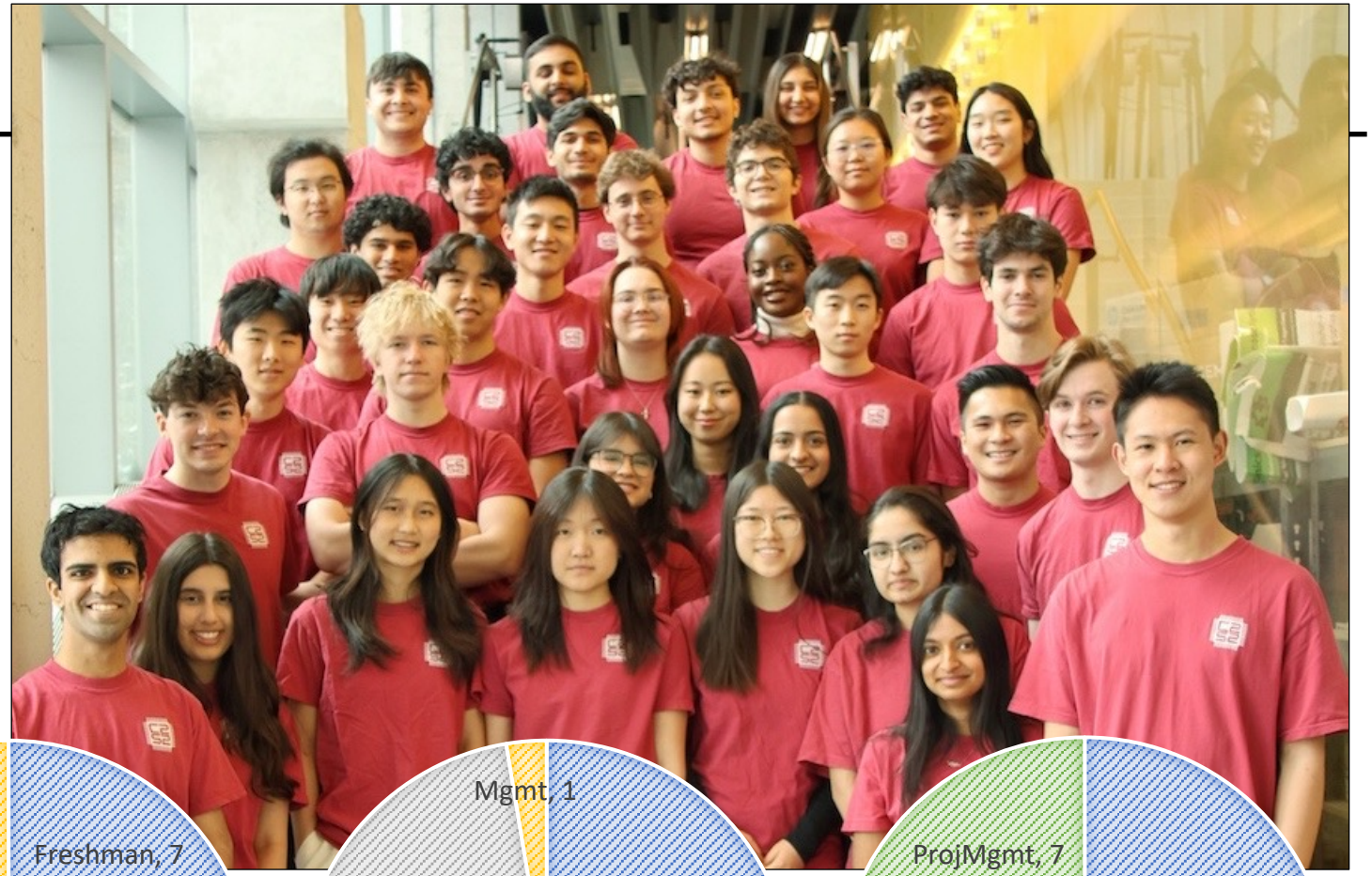
Experiential Learning for Semiconductor Chip Design through Student-Led Project Teams

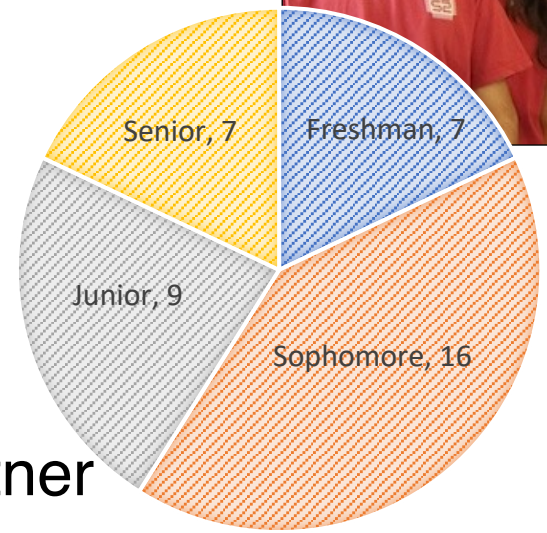


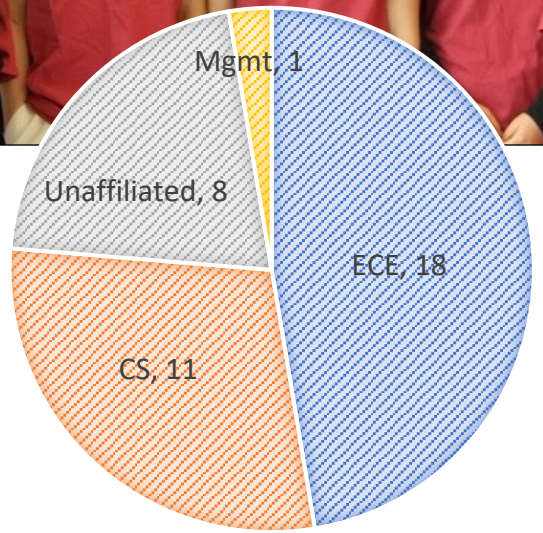
- Cornell Tape-Out Courses
- C2S2 Founding
- C2S2 Year 1: Campus Partner & Two Chips
- C2S2 Year 2: Two More SkyWater 130nm Chips
- C2S2 Year 3: Pivot to TSMC 180nm
- C2S2 Lessons Learned

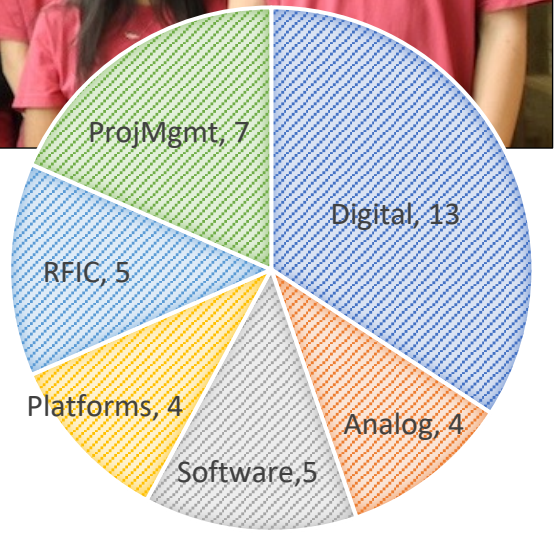
C2S2 Year 3 Team

- 38 members spanning all levels and four majors
  - 7 returning members
  - 31 new members
- Recruited Mohamed Ibrahim as third faculty co-advisor
- Year 3 focus
  - Abigail Varghese as new team lead
  - New RFIC subteam
  - Tapeout mixed-signal chip for bird tag demo
  - Find new campus partner

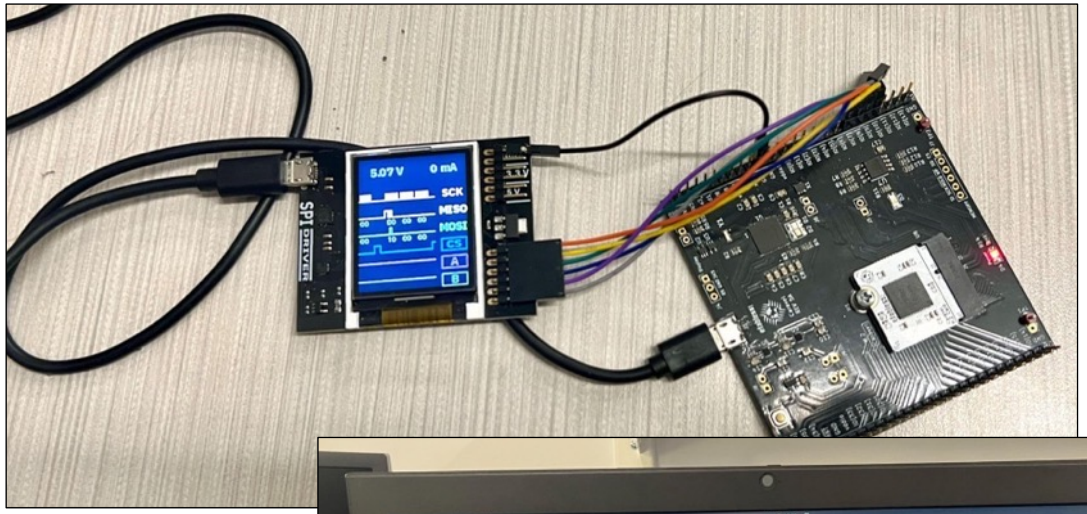


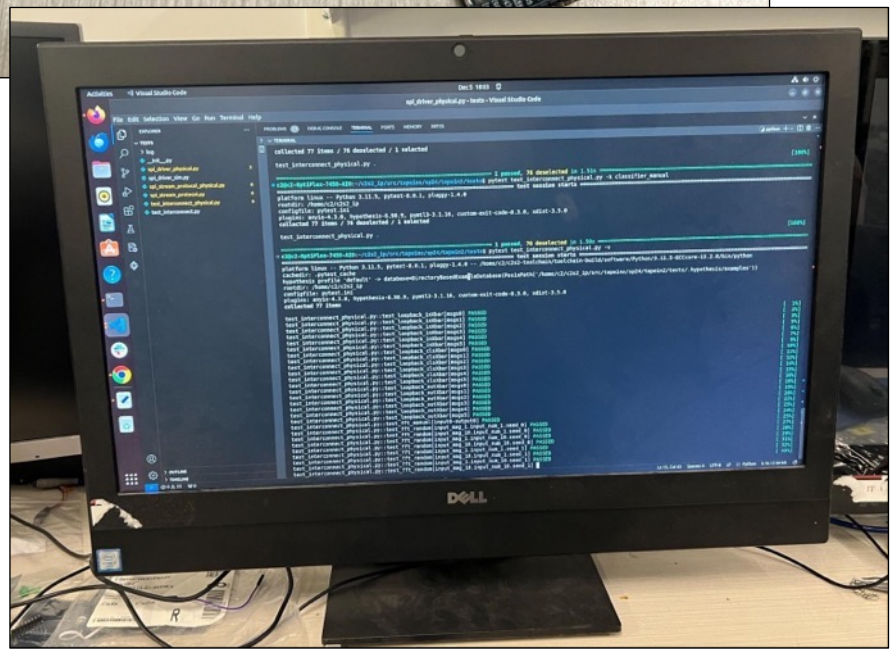




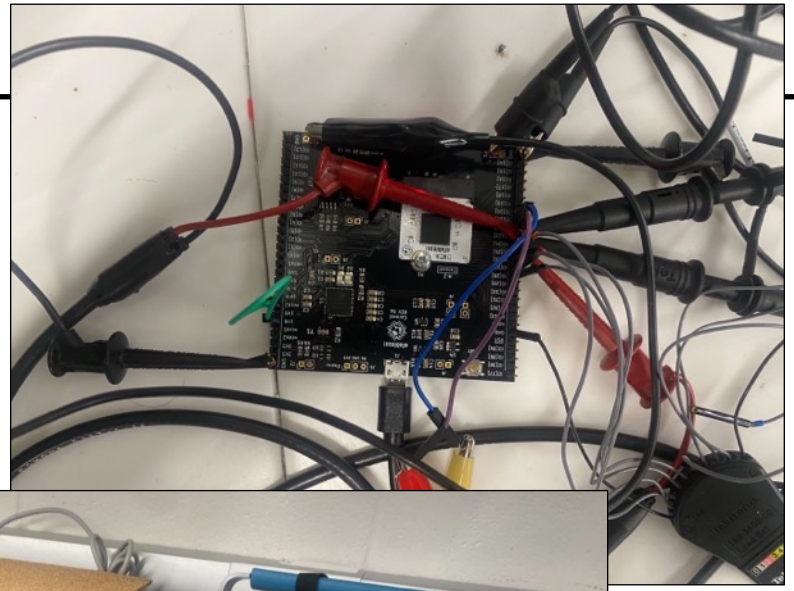


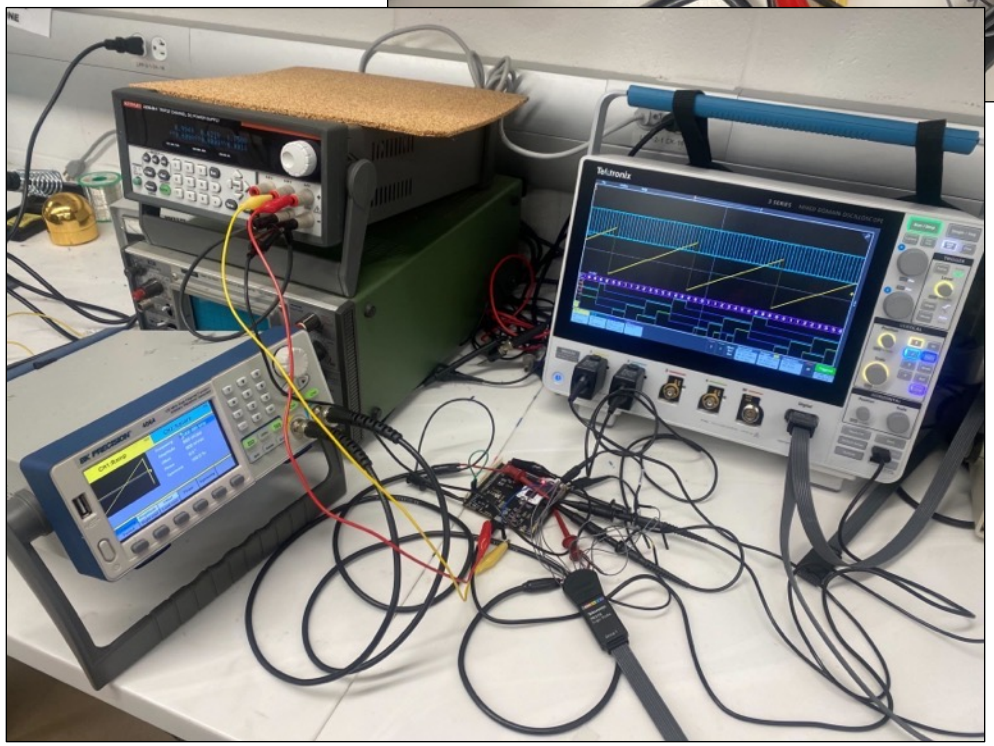
Testing Year 2 Chips





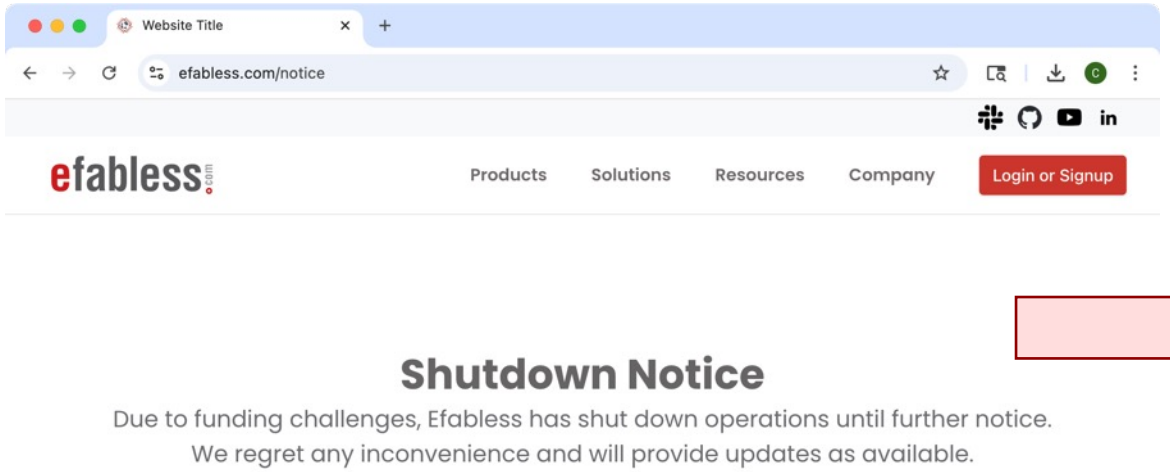
Both chips match pre-silicon testing results*

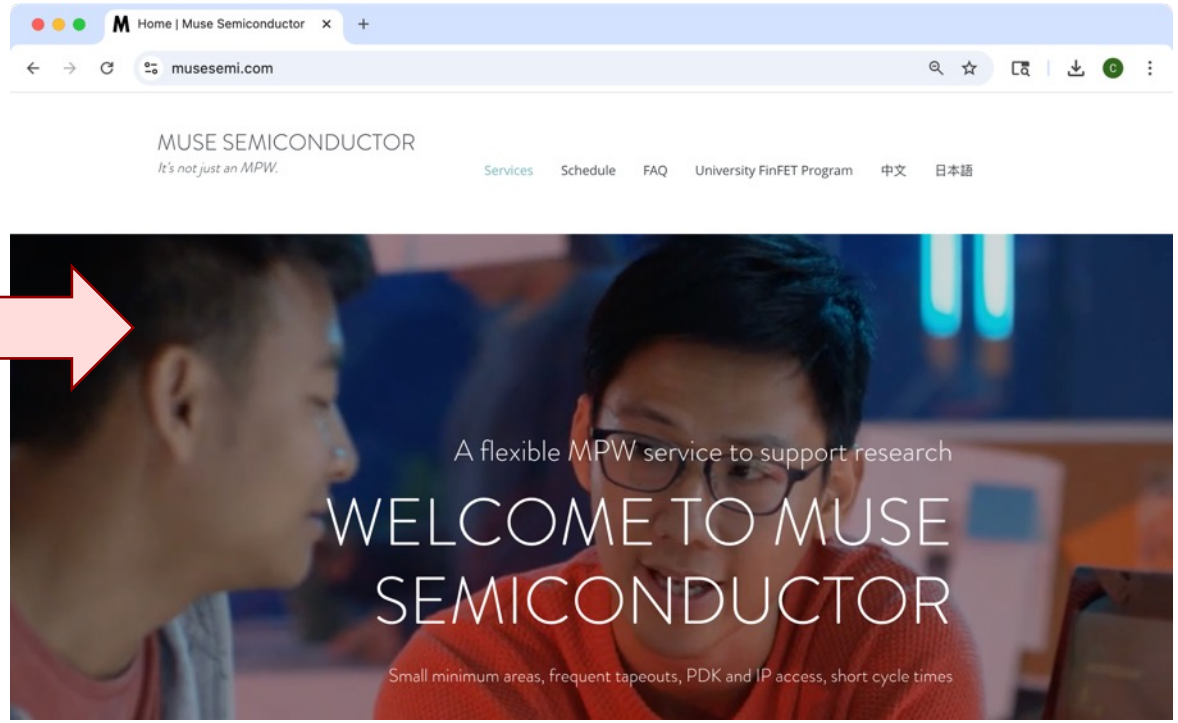




* Discovered functional issue due to bug in how SV to Verilog conversion tool handles signed logic

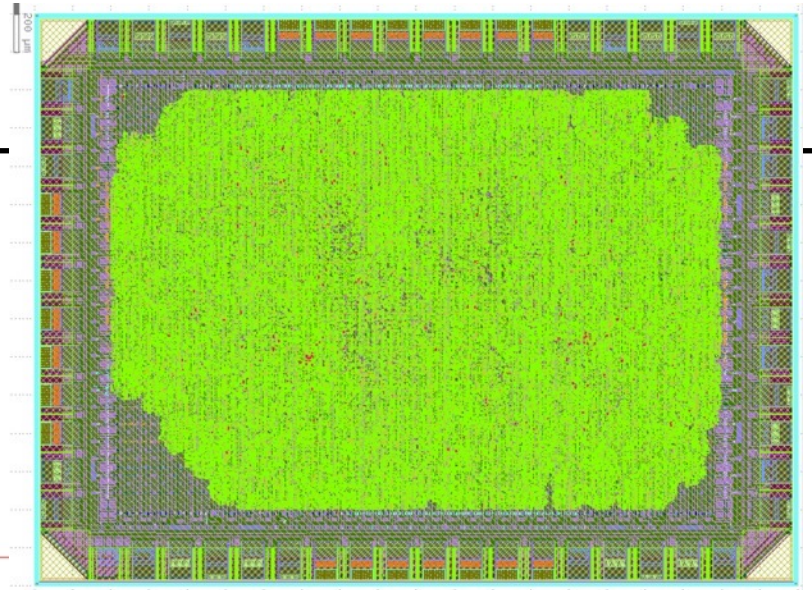
C2S2 Pivot to TSMC 180nm



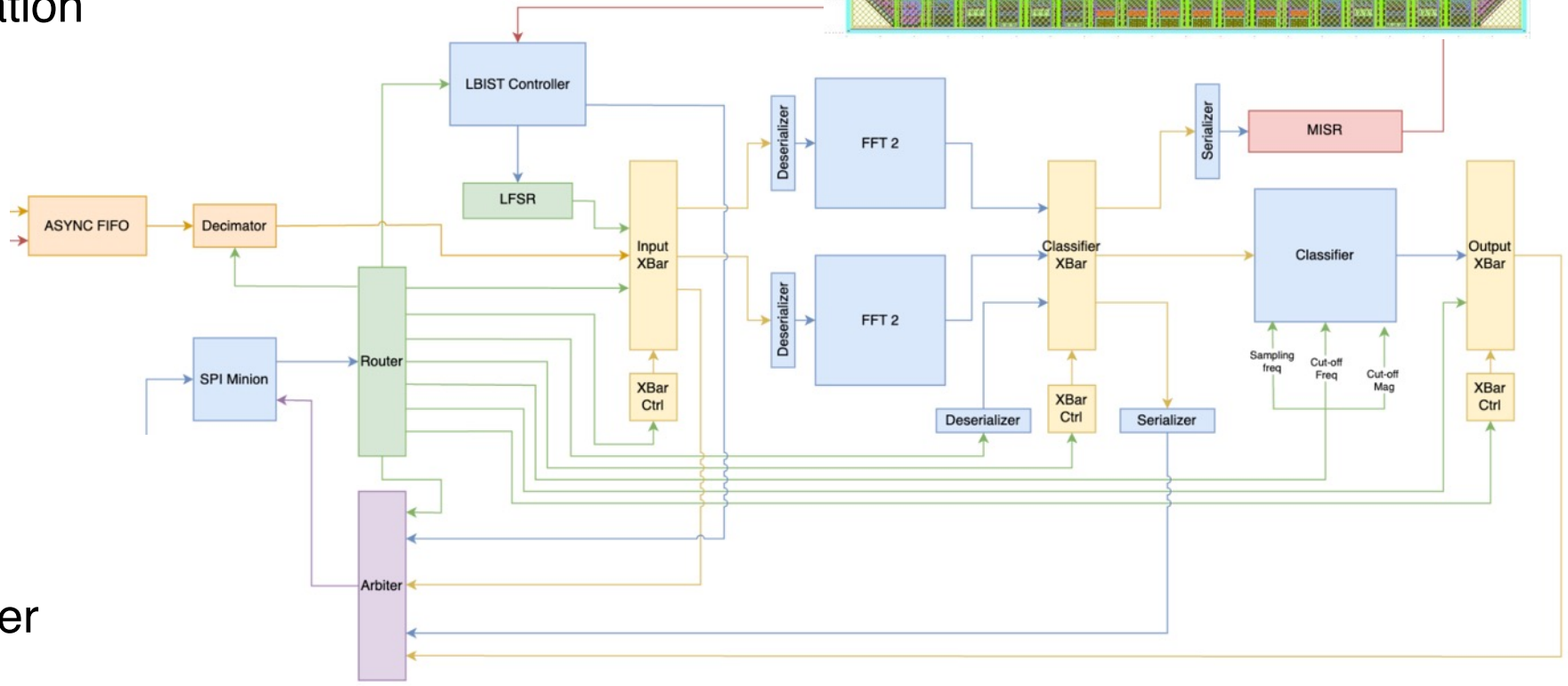


- Team was excited for the challenge!
  - Sign NDAs, manage confidential information
  - Bring up a commercial toolflow
  - Develop their own pad ring, power network
  - Manage their own packaging
  - Develop their own test boards
  - Find alternative to on-chip RISC-V core

C2S2 Year 3 Digital Tape-Out

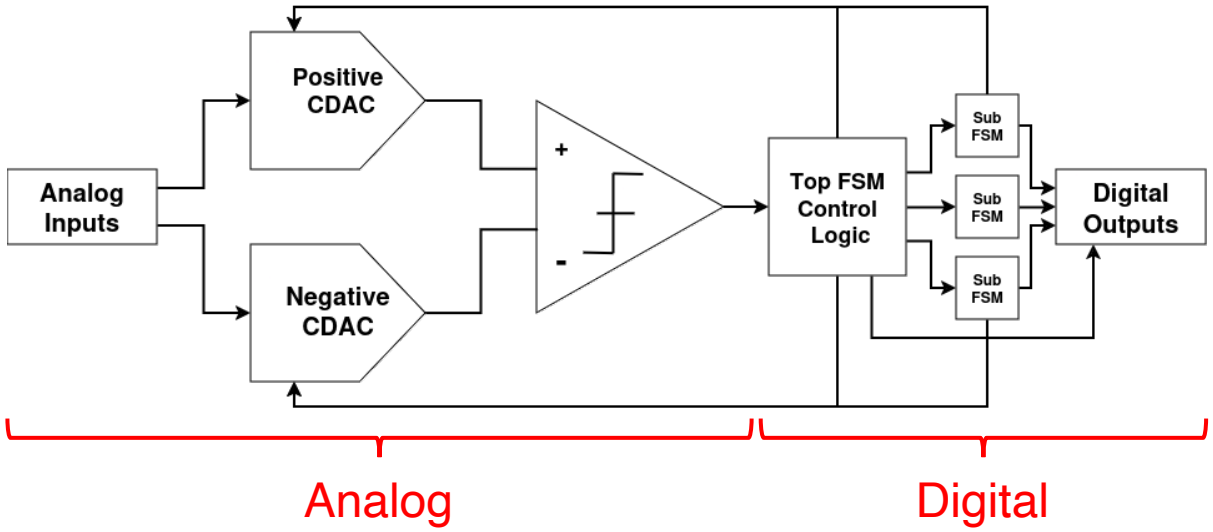


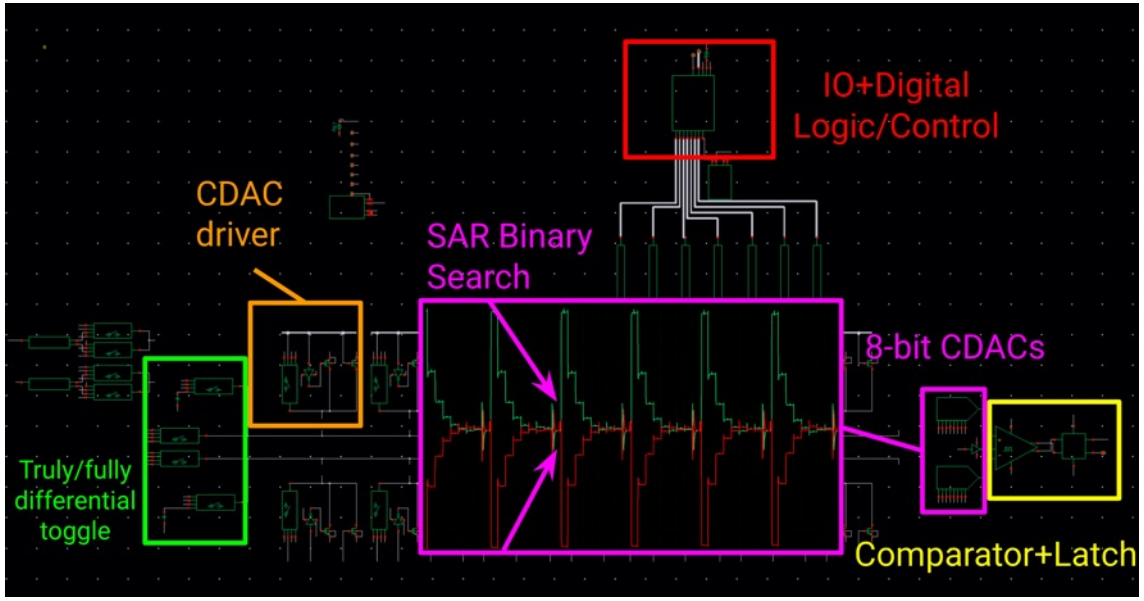
- Migrated to using commercial tools (Synopsys, Cadence, Mentor)
- Adopted many new improvements to digital design methodology
  - CocoTB for digital verification
  - Formal verification
  - FPGA emulation
  - Logical built-in self test
- New design
  - Asynchronous interface
  - Decimator to better meet target specifications
  - Multiple FFT units
  - Improved bird call classifier



C2S2 Year 3 Analog Tape-Out

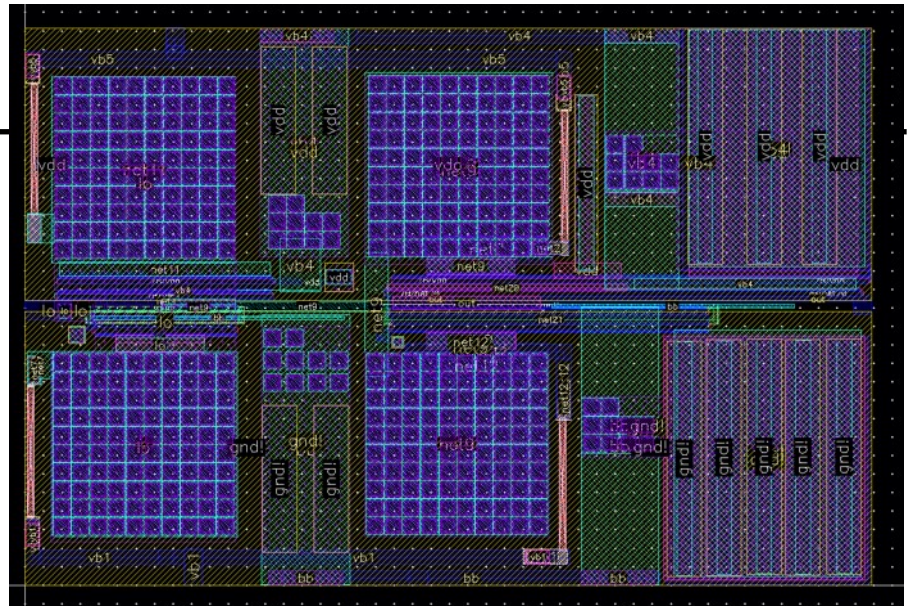
- Already migrating to commercial tools (Cadence, Mentor) early in the year for planned SkyWater 130nm tapeout
- Originally planning to tape-out SAR ADC integrated with digital FFT unit and classifier into a complete system-on-chip on SkyWater 130nm tape-out
- Currently planning to tape-out portion of SAR ADC including some analog circuits and digital control logic on dedicated TSMC 180nm tape-out

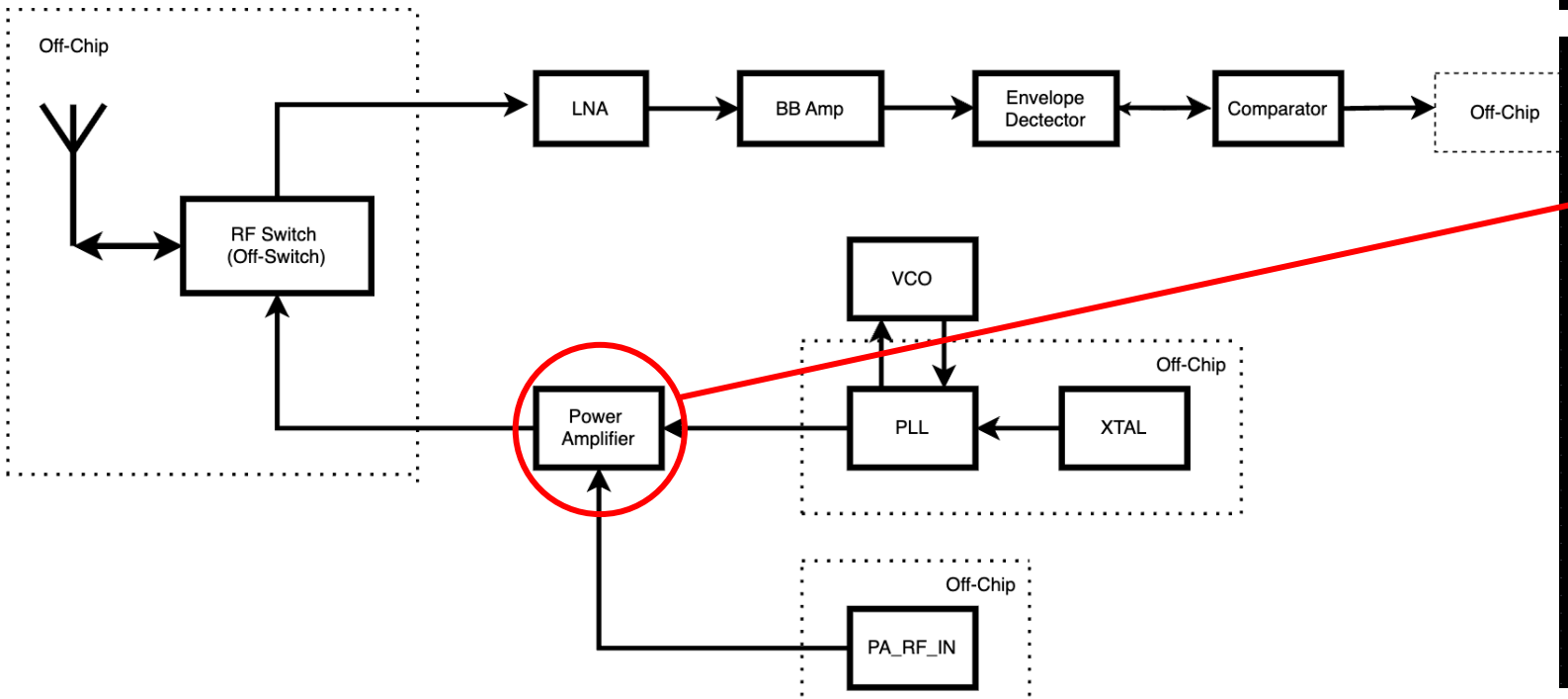


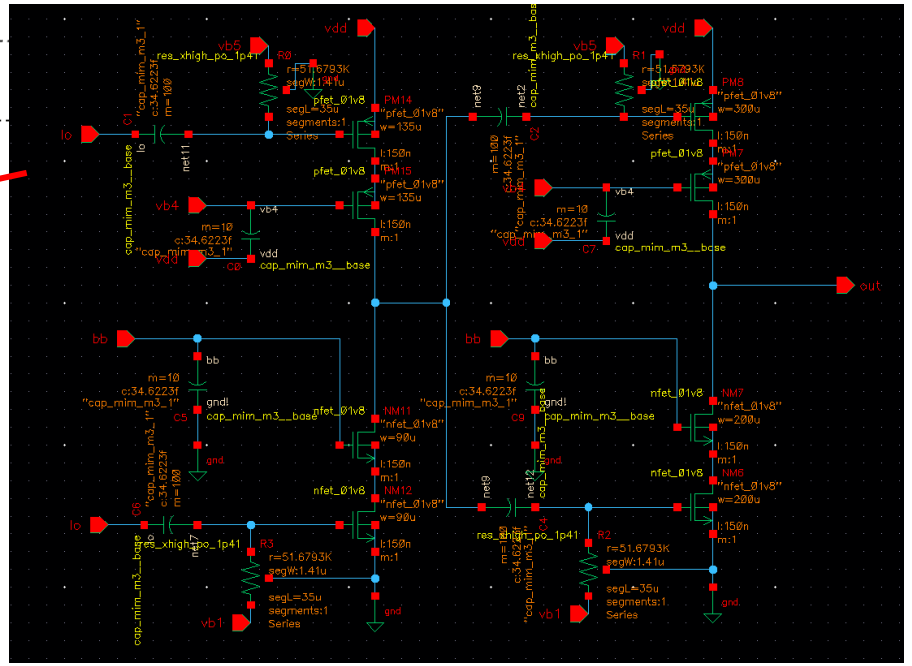


C2S2 Year 3 RFIC Tape-Out

- Original goal was to design simple half-duplex on/off keying 915MHz transceiver
- Could potentially be used in the future for wireless communication with bird tag
- Currently reducing scope given pivot to TSMC

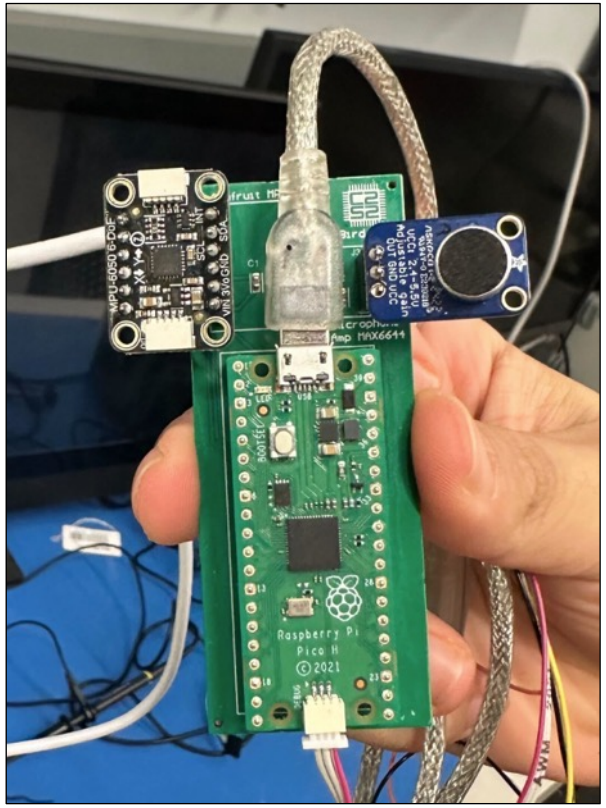


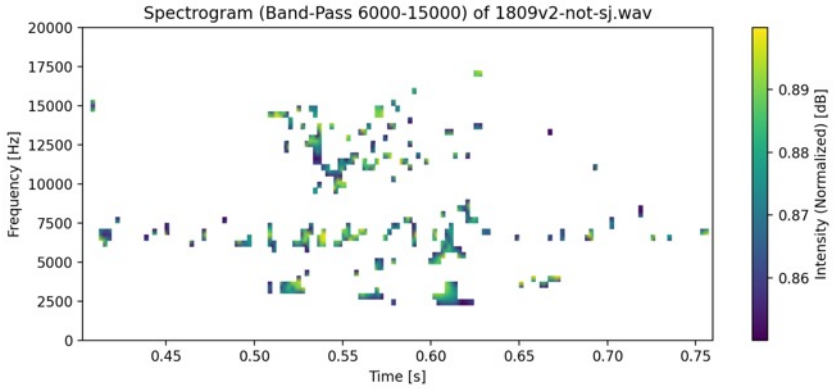


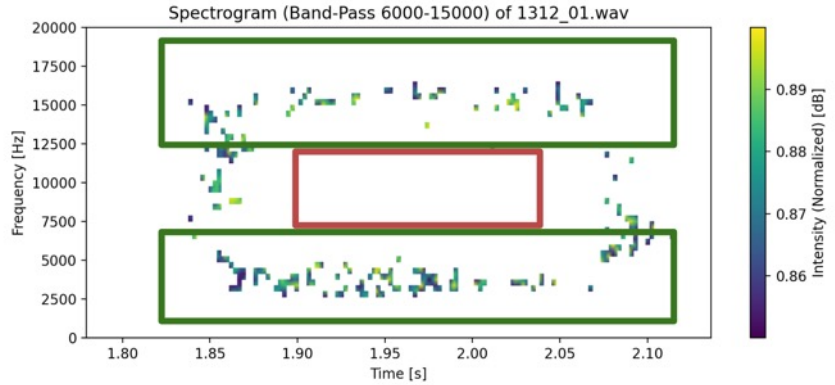


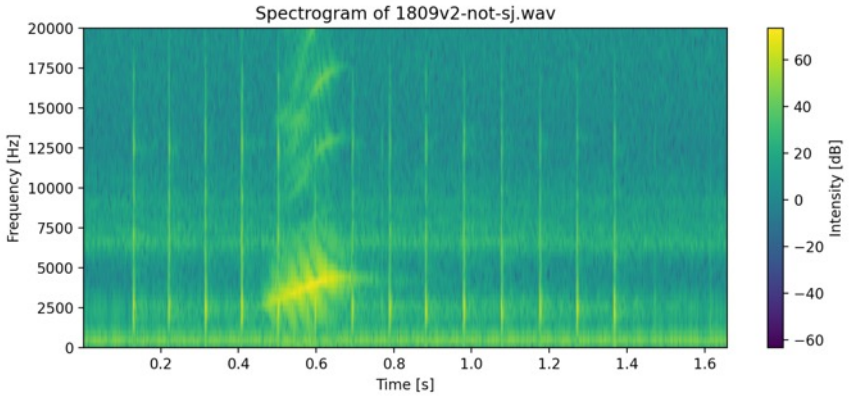
C2S2 Year 3 Software

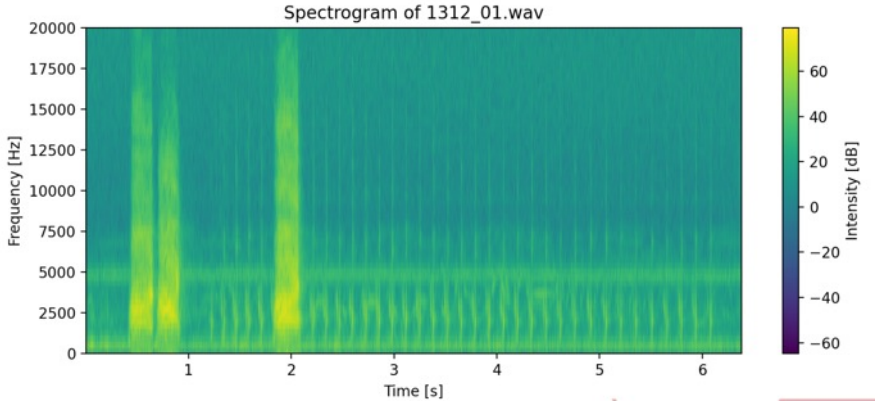
- Already migrating to Raspberry Pi Pico as target micro-controller early in the year
- Developed bird call classifier for scrub jays based on data from campus partner
- Custom hardware can act as lightweight detector and wakeup micro-controller



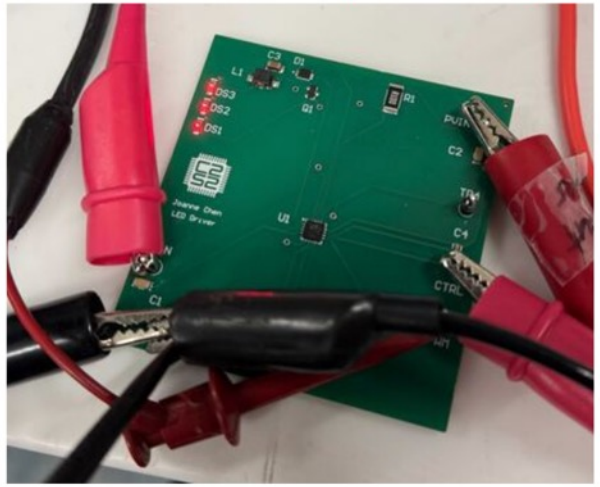


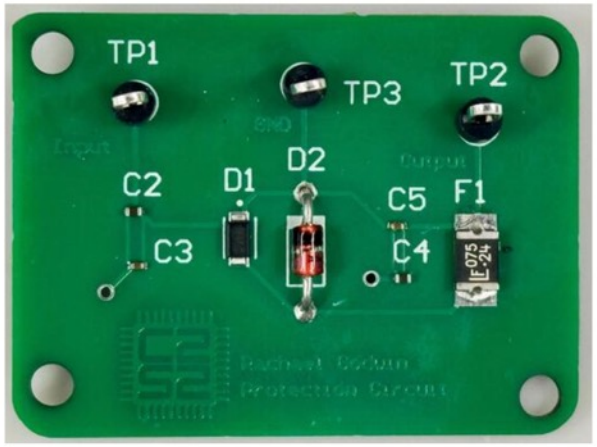


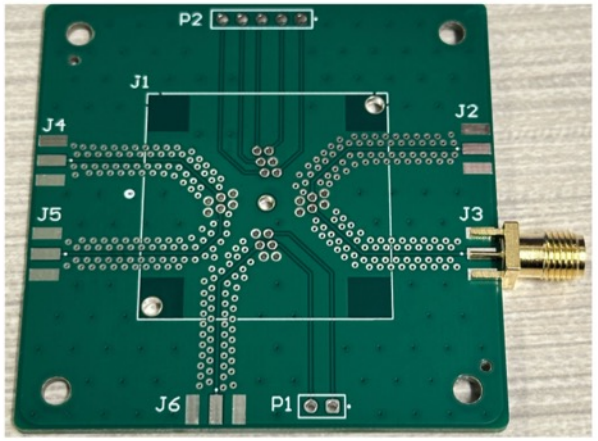


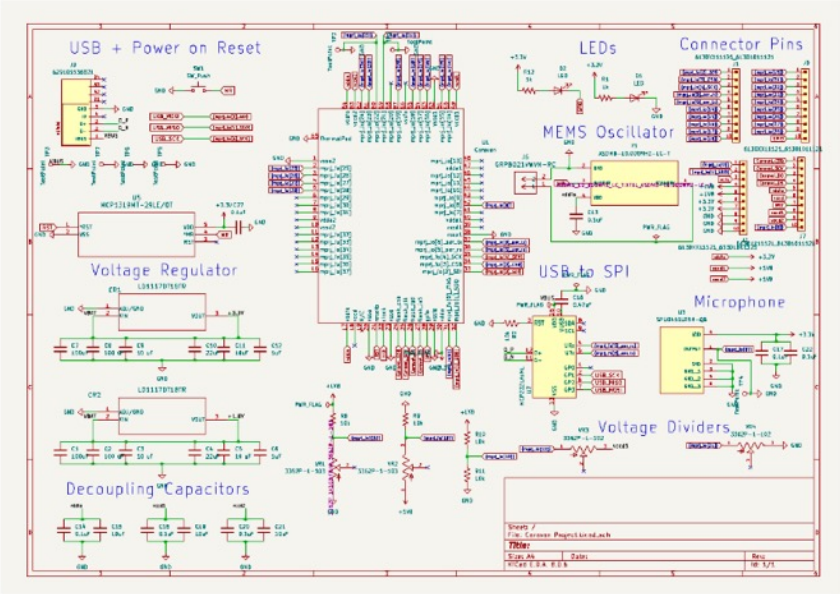


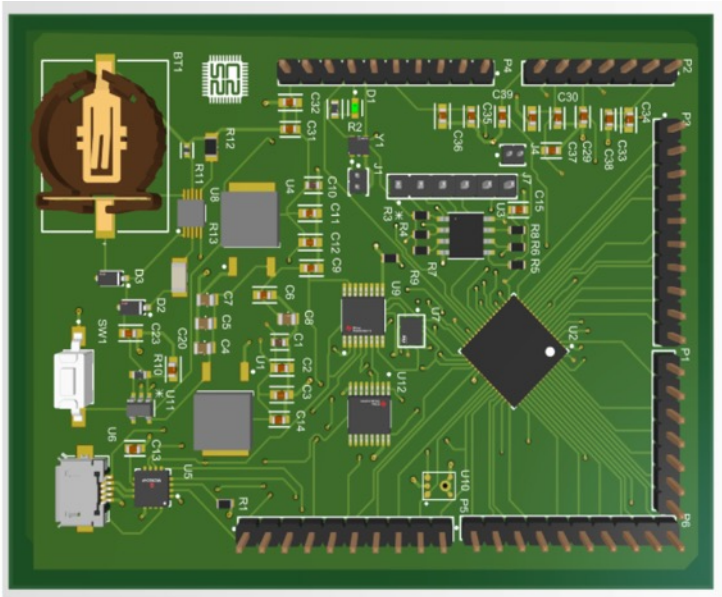
C2S2 Year 3 Platforms

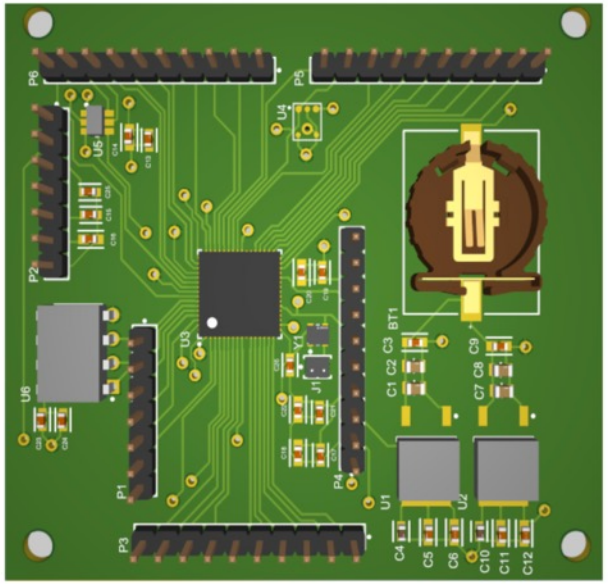




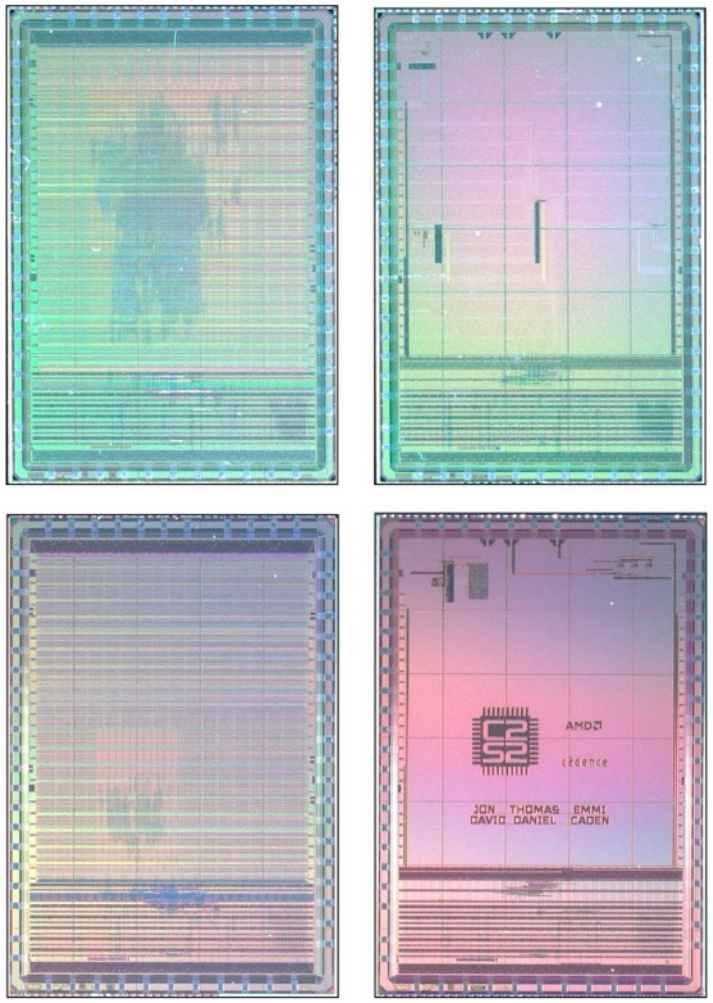








Experiential Learning for Semiconductor Chip Design through Student-Led Project Teams



- Cornell Tape-Out Courses
- C2S2 Founding
- C2S2 Year 1: Campus Partner & Two Chips
- C2S2 Year 2: Two More SkyWater 130nm Chips
- C2S2 Year 3: Pivot to TSMC 180nm
- C2S2 Lessons Learned

C2S2 Lessons Learned After Three Years

1. **Bootstrap the Initial Leadership Team –** First year leaders will shape the success of the entire project; need to include students with some experience as well as students brand new to chip design; *key is enthusiasm!*
2. **Provide Seed Funding –** Taping out chips is expensive; providing a few years of seed funding gives the team time to find external sponsors while still gaining experience taping out chips; *sponsors will come!*
3. **Encourage a Diverse Team –** Let students recruit members but work hard to encourage recruiting students at all levels and from different majors
4. **Carefully Manage Leadership Succession –** Start planning next year's leadership team as soon as possible; encourage current leaders to provide opportunities for mentoring and training

C2S2 Lessons Learned After Three Years

5. **Leverage Open-Source Chip Design Community –** Directly starting with TSMC would have been very challenging; open-source chip design lowers the barrier to entry; *post-efabless there are now four new paths for open-source chip design* (i.e., Cadence MPW & ChipFoundry on SkyWater 130nm, Synopsys MPW & WaferSpace on GF 180nm)

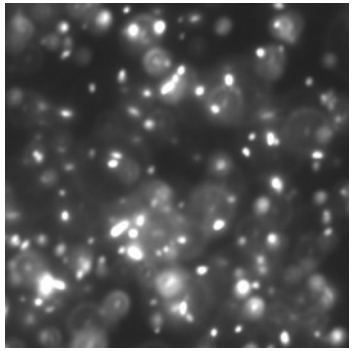
6. **Leverage Existing Project Team Ecosystem –** Cornell provides great administrative support and experimental laboratory space for project teams; training program for first-year members; team can leverage standard recruiting timeline and processes

7. **Create a Culture of Creativity, Flexibility, & Openness –** Encourage students to take ownership of the team; *listen to their ideas and help them achieve their goals* (e.g., moving from PyMTL to CocoTB, student-developed analog and RFIC subteams, next year new digital verification and physical design subteams)

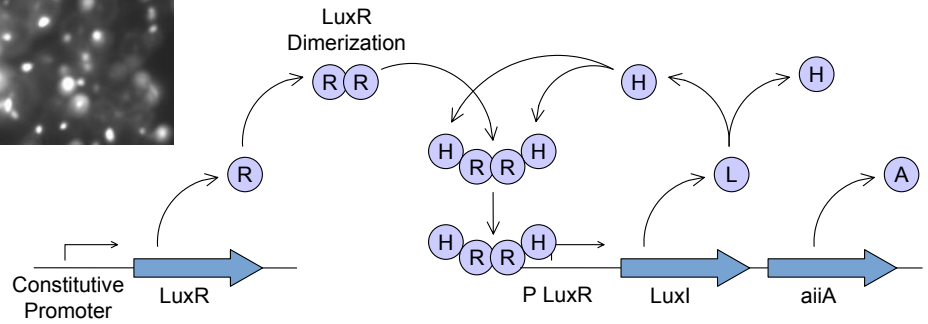
iGEM as an Ambitious Model?

iGEM 2004: 31 Participants on 5 Teams *(including me!)*

iGEM 2025: 7000+ Participants on 400+ Teams



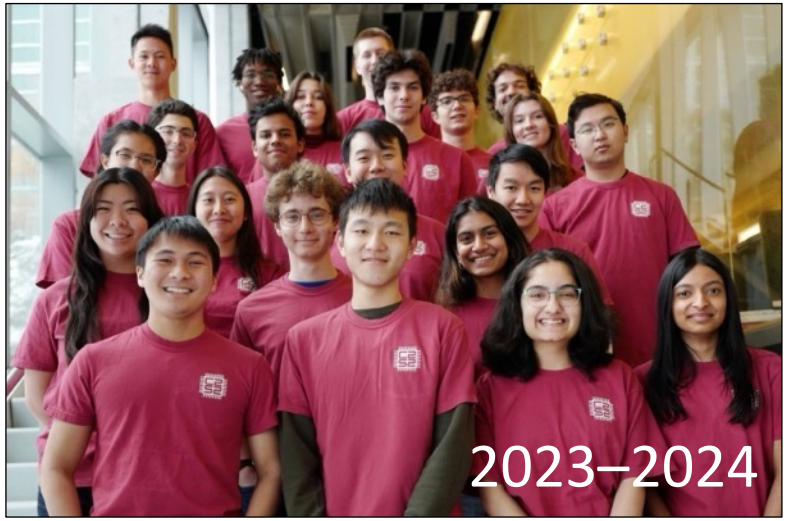
Annual event showcasing projects by multidisciplinary teams solving challenging problems using synthetic biology



Tremendous impact in generating excitement around biotechnology and synthetic biology

- Standardized DNA "parts"
- Open assembly techniques
- Accessible to all kinds of students
- Building community instead of competition

Can we achieve the same impact through a **national chip design competition?**



Siddhant Ahuja, **Chimdi Anude**, Lena Araujo, **David Bertuch**, **Anjelica Bian**, Austin Brown, Shihao Cao, **Elias Castro**, Javier Chambilla, Nicholas Channg, Sana Chawla, Jiming Chen, Joanne Chen, **Tomas Choi**, Kene Chukwuma-Orakwe, Angela Cui, Tanya Datta, **Taylor Do**, **Thomas Figura**, Mika Finkman, **Jack Frank**, Ethan Gabizon, **Demetrios Gavalas**, **Rachael Godwin**, **Ananya Goenka**, Matt Hales, Sarah Hawes, **Jon Ho**, Vinay Ivaturi, Ena Jovanovic, **Daniel Kaminski**, Tean Lai, **Edmund Lam**, Emily Lan, **Vicky Le**, Madeleine Lee, Chris Lonergan, Barry Lyu, **Johnny Martinez**, Michael McGruder**, Aidan McNay**, Ivan Mokeyev, Arnav Muthiayen, Judith Osei-Tete, Jay Patel, **Alga Peng**, Natalia Pope, Andrew Pung, **Sherri Qazi**, Anishka Raina, Nathan Rakhlin, Arjun Saini, **Will Salcedo**, Jasmine Samadi, Kate Sanders, **Akanksha Sarkar**, Christopher Schiff, **Joyce Shen**, Jun Sim, Setor Simpri, Anika Sukthankar, Steven Sun, Adele Thompson, Annalise Thompson, **Vayun Tiwari**, **Simeon Turner**, **Akshati Vaishnav**, **Abigail Varghese**, **Joseph Wan**, **Jason Wang**, Jeffrey Wilcox, **Chidera Wokonko**, Emmi Wyttenbach, Shang Xiang, **Caden Xu**, **Alyssa Xu**, Paige Yun, Xiangyi Zhao, **Tanya Zhou**