All New Course Content!

ECE 6745 Complex Digital ASIC Design
Spring 2026

Prof. Christopher Batten

Lecture: Tuesdays & Thursdays @ 1:25–2:40pm

Required Lab Section: Fridays @ 1:25–4:25pm

Prerequisites: ECE 4750 or ECE 5740

This course has been completely redesigned to include a real tape-out experience through a commercial semiconductor foundry. This will be the first tape-out course offered at Cornell in 20 years. The course is structured around three projects focused on digital chip design each of which is 4–5 weeks long and completed in groups of 2–3 students. The course is supported through the College of Engineering, the Center for Education of Microchip Designers, and the Taiwan Semiconductor Manufacturing Company and will also included engagement with current digital design and verification engineers at Apple. *ECE 4750/5740 is a firm prerequisite in order to take this course!*

- **Project 1: TinyFlow Tape-out –** Students will build their own TinyFlow, a very simple standard-cell-based flow in Python. They will develop four standard cells in TSMC 180nm and the corresponding standard cell logical, timing, and physical views. They will then implement simple algorithms for technology mapping, static timing analysis, placement, and routing. Even though their TinyFlow will only support a very small combinational subset of Verilog, this project still gives students a unique hands-on opportunity to appreciate every step required in more sophisticated commercial tools. Each group will create a tiny block using their tiny flow and these blocks will be aggregated into a single unified tape-out on the TSMC 180nm technology node.
- **Project 2: Accelerator Tape-out –** Students will leverage what they learned in the first project to transition to using a commercial standard-cell library and commercial electronic design automation tools for simulation, synthesis, place-and-route, static-timing analysis, power analysis, design rule checking (DRC), and layout-vs-schematic checking (LVS). Students will develop a simple accelerator in Verilog RTL and evaluate the potential benefit of using this accelerator in the context of a RISC-V processor. Students will then combine just their accelerator with an SPI interface and use the commercial library and tools to turn this accelerator+SPI into complete chip layout in TSMC 180nm. Students will need to navigate many practical issues associated with a real tape-out including packaging, chip I/O, clock tree synthesis, fixing setup and hold time violations, sign-off timing analysis, DRC and LVS, seal ring insertion, etc. Students will upload their designs for fabrication at TSMC and then test their chips in the lab through a separate 1-credit chip testing class offered in Fall 2026.
- **Project 3: System-on-Chip Tape-in –** Owing to the small silicon area, the tape-out in the second project will have to be relatively simple. In the final project, students will be able to explore a more complex system-on-chip using everything they have learned in the first two projects. Students will have access to commercial SRAM memory compilers and since this final project will not be taped out, they can use much more area than is feasible in the second project. Students are free to explore any design they wish including advanced processor, memory, and/or network microarchitecture as well as various accelerators.