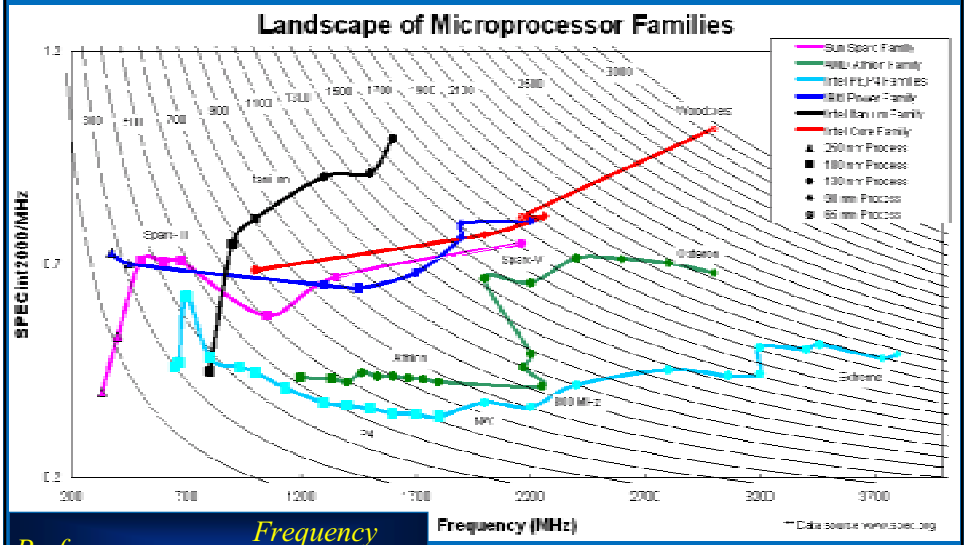
Lost in the Bermuda Triangle: Complexity vs. Energy vs. Performance

John Paul Shen
Intel Microarchitecture Research Lab

June 18, 2006
WCED Panel

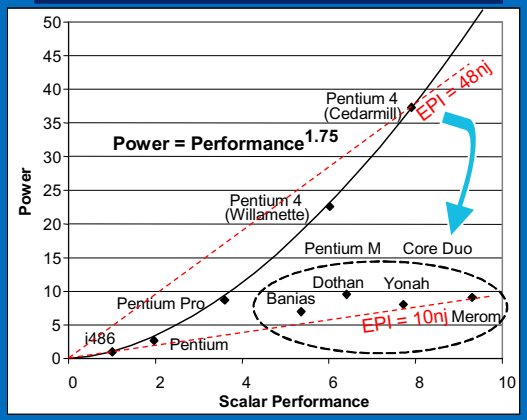
Microprocessor Performance Evolution



$$Performance = \frac{Frequency}{PathLength \times CPI}$$

Power/Performance (EPI) Evolution

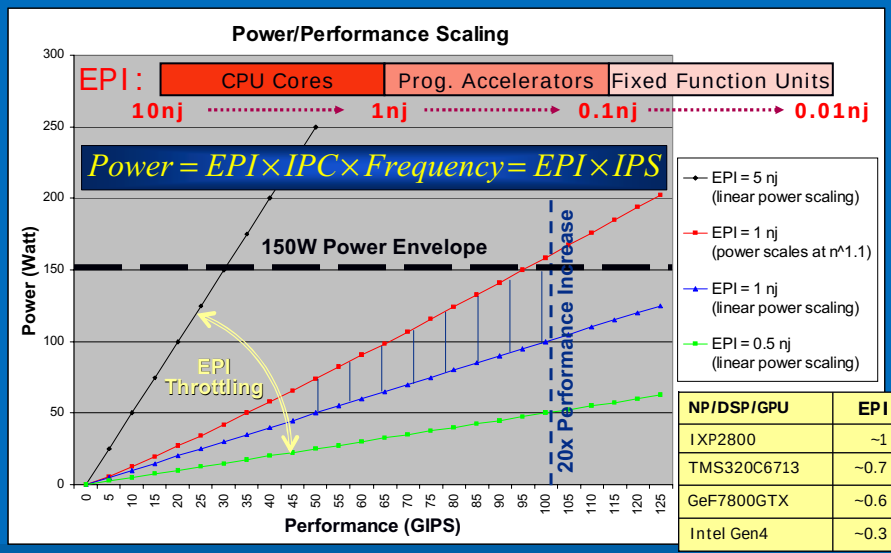
$$Power = EPI \times IPC \times Frequency$$



Intel Microprocessors	EPI (nj) 65nm at 1.33v
i486	10
Pentium	14
Pentium Pro	24
Pentium 4 (WMT)	38
Pentium 4 (CDM)	48
Pentium M (Banias)	13
Pentium M (Dothan)	15
Core Duo (Yonah)	11
Core Duo (Merom)	10

Power: single core power (relative to i486 baseline)
Performance: SPECint performance (relative to i486 baseline)
EPI: average energy spent per instruction (in nano-joules)

EPI Optimization for CMP Architectures



NP/DSP/GPU	EPI
IXP2800	~1 nj
TMS320C6713	~0.7 nj
GeF7800GTX	~0.6 nj
Intel Gen4	~0.3 nj

Research Challenges

- 10x Reduction of Core EPI:
  - Avoid $O(n^2)$ and $O(n^3)$ structures
  - Leverage heterogeneous cores/accelerators
- Linear Power Scaling of Uncore:
  - Provide on-demand interconnects
  - Eliminate legacy interfaces
- 2x Reduction of Design Cycle:
  - Adopt modular design style
  - Reuse building blocks