WARP 2015
6th Workshop on Architectural Research Prototyping

Co-Located with the 42nd International Symposium on Computer Architecture
Sunday, June 14th, 2015 • Portland, Oregon
http://www.csl.cornell.edu/warp2015

Workshop Organizers

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Program Committee

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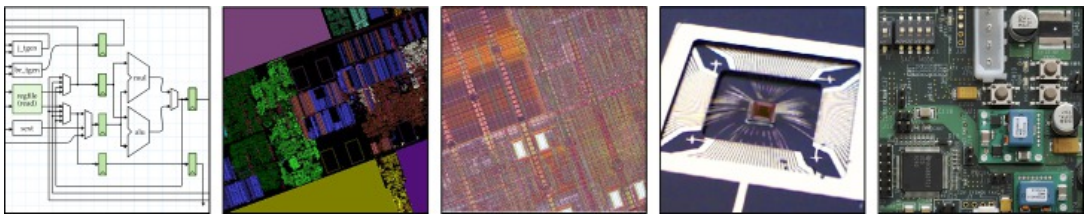

Building prototype systems can be one of the best ways to validate assumptions, gain intuition about practical design issues, and provide platforms for future software research. While the research ideas behind these prototypes can be published in top-tier conferences, there are not many venues suitable for focusing on the actual prototype itself. At the same time, building an FPGA, ASIC, or full-custom computer architecture prototype is a non-trivial endeavor and requires a significant financial and time commitment. This workshop is intended as a forum for the builders in our community to share their practical on-the-ground experiences, to provide a status update on their progress, and to convey insights for those considering prototyping their ideas.

This half-day workshop will be held on Sunday, June 14th, 2015, co-located with ISCA-42 in Portland, OR. The technical program committee and workshop organizers have selected a particularly strong program from a record number of submissions. Participation is encouraged for anyone interested in learning about some of the best prototyping work going on within the computer architecture research community. Participation is also encouraged for researchers that have recently constructed or are currently constructing prototypes, for those considering embarking on a prototyping effort, or even for those who strongly disagree with the need to build prototypes.

Workshop Advance Program

- *Prototyping Heterogeneous SoC Architectures: A System-Level Design Approach*, L. Carloni (Columbia University)
- *Post Mortem on Building 28nm/45nm RISC-V Vector Microprocessors with Chisel and the Rocket Chip Generator*, Y. Lee, A. Waterman, R. Avizienis, H. Cook, C. Sun, B. Zimmer, K. Asanovic (UC Berkeley)
- *State of the Akvario Project*, A. Hindborg, N. Jensen, P. Schleuniger, S. Karlsson (Technical University of Denmark)
- *Designing a Complex 25-Core Academic Processor*, D. Wentzlaff, M. McKeown, Y. Fu, T. Nguyen, Y. Zhou, J. Balkind, A. Lavrov, M. Shahrad, S. Payne (Princeton University)
- *From PDF to GDS: Designing the RoboBee SoC*, B. Reagen, X. Zhang, D. Brooks, G.-Y. Wei (Harvard University)
- *Lessons from Five Years of Making Michigan Micro Motes*, P. Pannuto, Y. Lee, Z. Foo, G. Kim, D. Blaauw, P. Dutta (University of Michigan)
- *NVM-Charade: Open-Sourced FPGA-Based NVM Characterization Scheme*, G. Park, M. Shihab, L. Nahar, S. Kang, D. Donofrio, J. Shalf, M. Jung (UT Dallas and Lawrence Berkeley National Laboratory)
- *Experiences with Two FabScalar-Based Chips*, E. Forbes, R. Chowdhury, B. Dwiel, A. Kannepalli, V. Srinivasan, Z. Zhang, R. Widialaksono, T. Belanger, S. Lipa, E. Rotenberg, W.R. Davis, P.D. Franzon (North Carolina State University)
- *Experiences and Lessons from a 3D Integrated Prototype*, R. Dreslinski (University of Michigan)
- *A 10G NetFPGA Prototype for In-Network Aggregation*, V.T. Lee, J. Nelson, M. Oskin, L. Ceze (University of Washington)
- *Cymric: A Framework for Prototyping Near-Memory Architectures*, C. Kersey, H. Kim, S. Yalamanchili (Georgia Tech)