ECE 6745 Complex Digital ASIC Design, Spring 2025

Next Steps

School of Electrical and Computer Engineering
Cornell University

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1. Verify you can view the Canvas course site

We will be using Canvas for all announcements, distributing course materials, collecting assignments, and distributing grades. Please make sure that if you are officially enrolled in the course you can view this course in Canvas.

2. Verify you can view the Ed discussion forum

We will be using Ed for online discussion and most student/instructor communication. Students officially enrolled should already be automatically added to the Ed discussion forum for this course. Please use the link in Canvas to make sure you can view the Ed discussion forum.

3. Read the course syllabus

The course syllabus contains essential information about the course motivation, structure, procedures, and policies. It will be assumed that all students have read and understand all of the material in the course syllabus. We will not waste lecture time going through every detail of the syllabus, so it is very important to read the entire syllabus!

4. Read Chapter 1 of Weste and Harris

The course textbook is *"CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed."* by Neil Weste and David Harris. For your convenience, the first chapter is available as a PDF on the Canvas course page in the readings section.

5. Review background material as necessary

Students which are less confident of their mastery of the material covered in ECE 4750 might consider reviewing the material on the ECE 4750 public course website. Students which are new to Verilog might find it useful to review a text on this hardware-description language, such as "Verilog HDL, 2nd ed." by Samir Palnitkar. Students which have never used Python before may want to spend additional time reviewing the textbook titled "Think Python: How to Think Like a Computer Scientist" by A. B. Downey (Green Tea Press, 2012) (which is also available as a PDF on the Canvas course page in the resources section).

6. Work through lab tutorials

Various lab tutorials will be posted on the public course website to help you familiarize yourself with the Verilog hardware modeling framework, Python testing framework, and the ASIC CAD

toolflow. We are still setting things up, but stay ready for tutorials on remote access to ecelinux, Linux, git, and Verilog. These first four tutorials are similar to what is used in ECE 4750, but students may still find it useful to review them to refresh their understanding of important tools, techniques, and guidelines. Additional tutorials will be posted next week.

7. Begin selecting a partner for the lab assignments and project

The lab assignments are specifically designed to be a reasonable amount of work for a pair of two students working together. Students should begin the process of selecting a partner, since this choice can often make a significant difference in succeeding on the lab assignments.

8. Attend the discussion section next Friday in 225 Upson Hall

Students are expected to attend the weekly discussion section. There will be no discussion section this week. The first discussion section will be next week on Friday 1/31 from 3:35–4:25pm in 225 Upson Hall. The first discussion section will be the front-end portion of the ASIC toolflow.