ECE 5745 Complex Digital ASIC Design

Midterm Example Appendix

http://www.csl.cornell.edu/courses/ece5745
School of Electrical and Computer Engineering
Cornell University

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Appendix A: Logical Effort Equations

Equation or Symbol	Description
g	Gate logical effort
$h = C_{out}/C_{in}$	Gate electrical effort
$f = gh$	Gate effort
p	Gate parasitic delay
p_{inv}	Parasitic delay of minimum-sized inverter
τ	Delay unit ($3RC$)
$d = f + p$	Delay in units of τ
$d_{abs} = d\tau$	Absolute delay in seconds
$G = \prod g_i$	Path logical effort
$B = \prod b_i$	Path branching effort
$H = C_{out}/C_{in}$	Path electrical effort
$F = GBH$	Path effort
$D = \sum d_i = \sum g_i h_i + \sum p_i$	Path delay
$f_{opt} = F^{1/N}$	Optimal stage effort
$D_{opt} = N f_{opt} + P$	Optimal path delay
$C_{in,opt,i} = C_{out,i} \times g_i / f_{opt}$	Optimal input capacitance for stage i

	Number of inputs					
Gate Type	**1**	**2**	**3**	**4**	**5**	**n**
Inverter Logical Effort	1					
NAND Logical Effort		4/3	5/3	6/3	7/3	$(n+2)/3$
NOR Logical Effort		5/3	7/3	9/3	11/3	$(2n+1)/3$
XOR/XNOR Logical Effort		4	12	32		
Inverter Parasitic Delay	p_{inv}					
NAND Parasitic Delay		$2p_{inv}$	$3p_{inv}$	$4p_{inv}$	$5p_{inv}$	np_{inv}
NOR Parasitic Delay		$2p_{inv}$	$3p_{inv}$	$4p_{inv}$	$5p_{inv}$	np_{inv}
XOR/XNOR Parasitic Delay		$4p_{inv}$	$4p_{inv}$	$4p_{inv}$	$4p_{inv}$	$4p_{inv}$

Appendix B: Technology Parameters for 90 nm Process

Parameter	Value	Description
τ	7.4 ps	Delay unit ($3RC$)
p_{inv}	$1\,\tau$	Parasitic delay of cannonical minimum sized inverter
μ_n/μ_p	2	Ratio of NMOS mobility to PMOS mobility
V_{dd}	1 V	Nominal supply voltage
C	0.5 fF	Gate capacitance for NMOS in cannonical minimum sized inverter