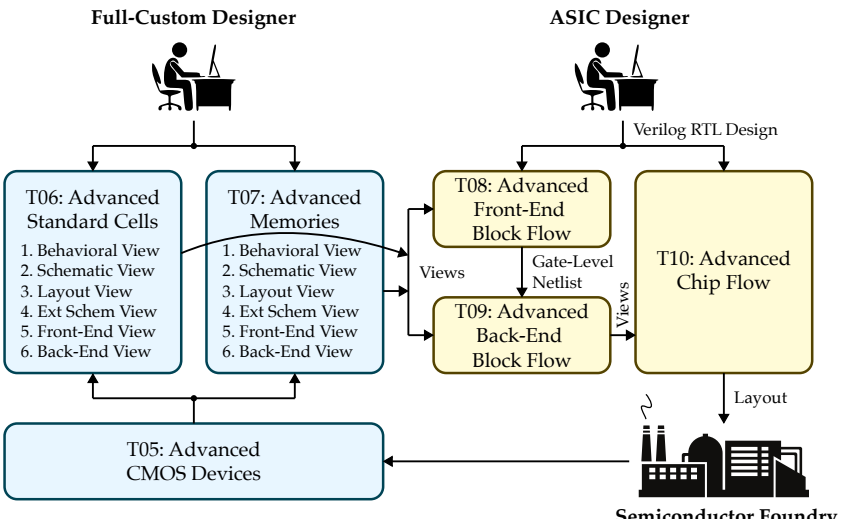
ECE 6745 Complex Digital ASIC Design

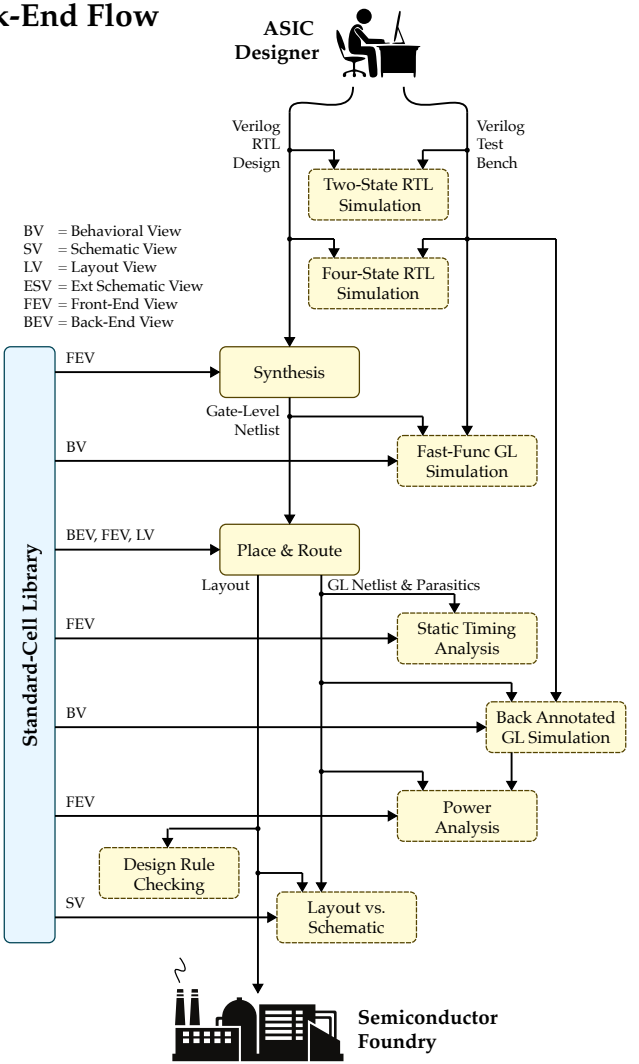
Topic 9: Advanced Back-End Flow

School of Electrical and Computer Engineering
Cornell University

revision: 2026-03-19-12-19

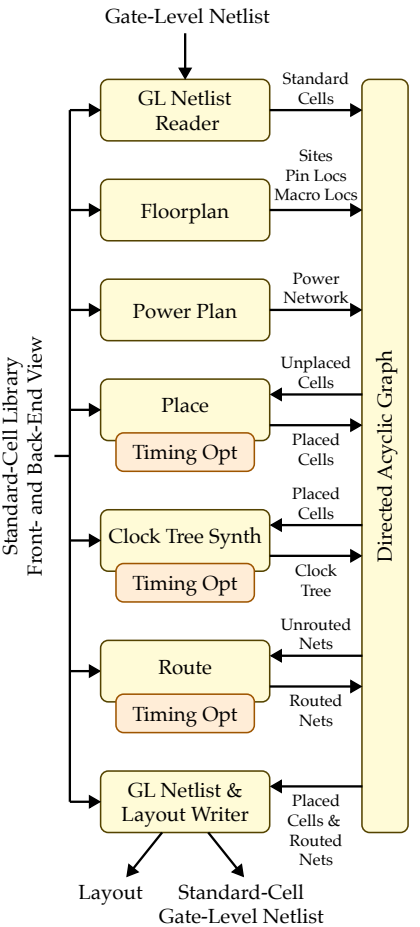


1. Back-End Flow



Place-and-Route

- Place-and-route takes as input a standard-cell gate-level netlist, places cells, routes nets, and produces the final layout
- Place-and-Route Data Structure
  - Graph of standard-cell nodes
- Place-and-Route Algorithms
  - GL Netlist Reader: Parse gate-level netlist into graph of standard-cell nodes
  - Floorplan: Creates grid of sites and position macros and pins
  - Power plan: Create power distribution network
  - Place: Places each standard cell on the grid of sites
  - Clock Tree Synthesis: Create clock tree buffers and routing
  - Route: Routes each net on the routing grid
  - Timing Optimization: Size gates and insert buffers to meet timing constraints
  - Layout & GL Netlist Writer: Outputs the final layout along with an updated standard-cell gate-level netlist



1.1. *Algorithm:* Floorplan

- Goal is to create a grid of sites, position input/output pins, and place macros
  - Each *site* is a one standard cell height tall and one routing track wide
  - Standard cells must be placed such that they align to sites
  - Must also place macros (e.g., SRAM macros)

Fixed Floorplan

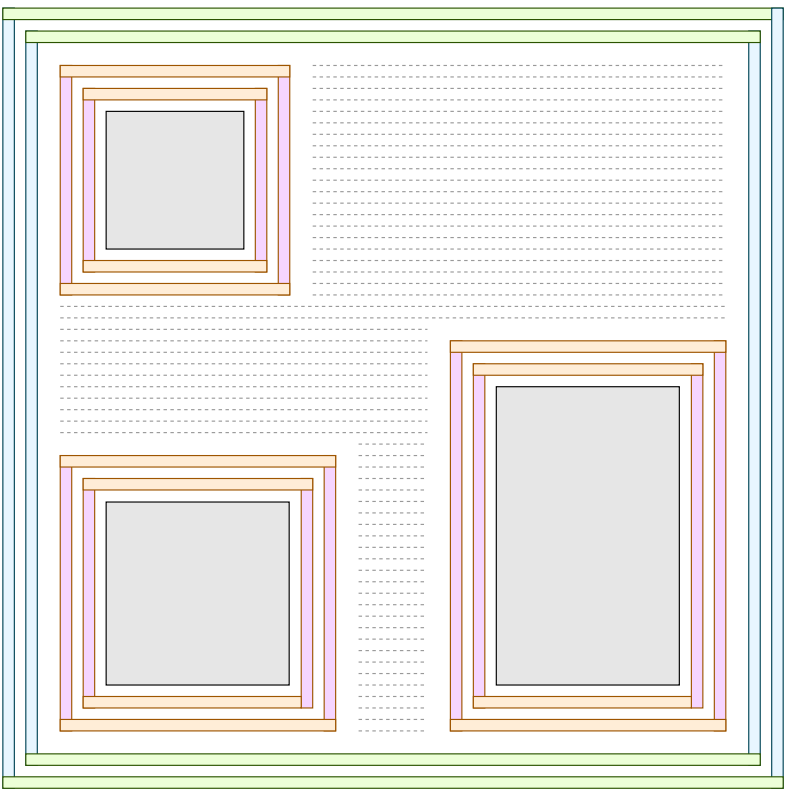
- Width, height, input/output pins, and macro placements are given

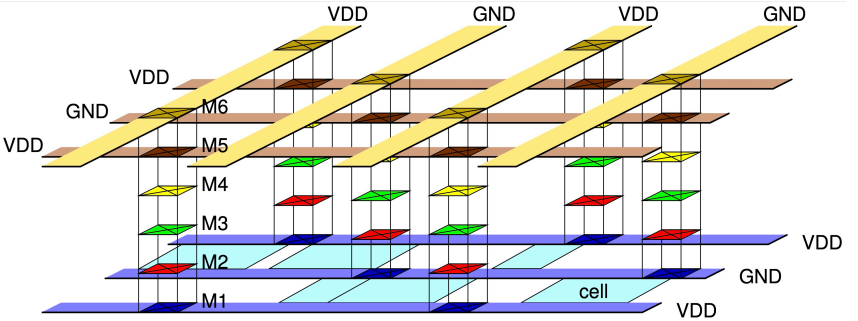
Automatic Floorplan

- Standard cell density and aspect ratio are given
- Calculate total area from gate-level netlist + macro area
- Divide by cell density to get total floorplan area
- Use aspect ratio to determine width and height
- Automatically position input and output pins along perimeter
- Automatically place macros minimizing wire length estimate

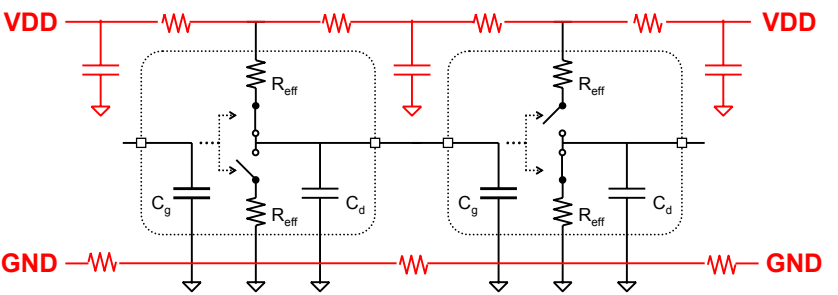
1.2. *Algorithm:* Power Plan

- Each macro has its own local power ring
- Create global power ring around the outside of the block
- Create metal 1 power straps across standard cell rows
- Create power grid on top metal layers

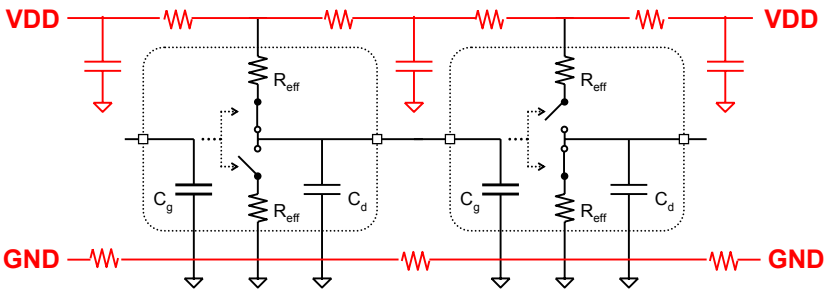




Static IR Drop



Dynamic IR Drop



Impact of Static and Dynamic IR Drop

- Lower effective voltage across logic gates
  - Propagation delays increase
  - Noise margins shrink

1.3. *Algorithm:* Place

- Global Placement: Use hierarchical and interative algorithms to roughly place standard cells on chip without worrying about exact legal palcement restrictions
- Detailed Placement: Ensure every standard cell is in a legal location and then perform local placement optimizations

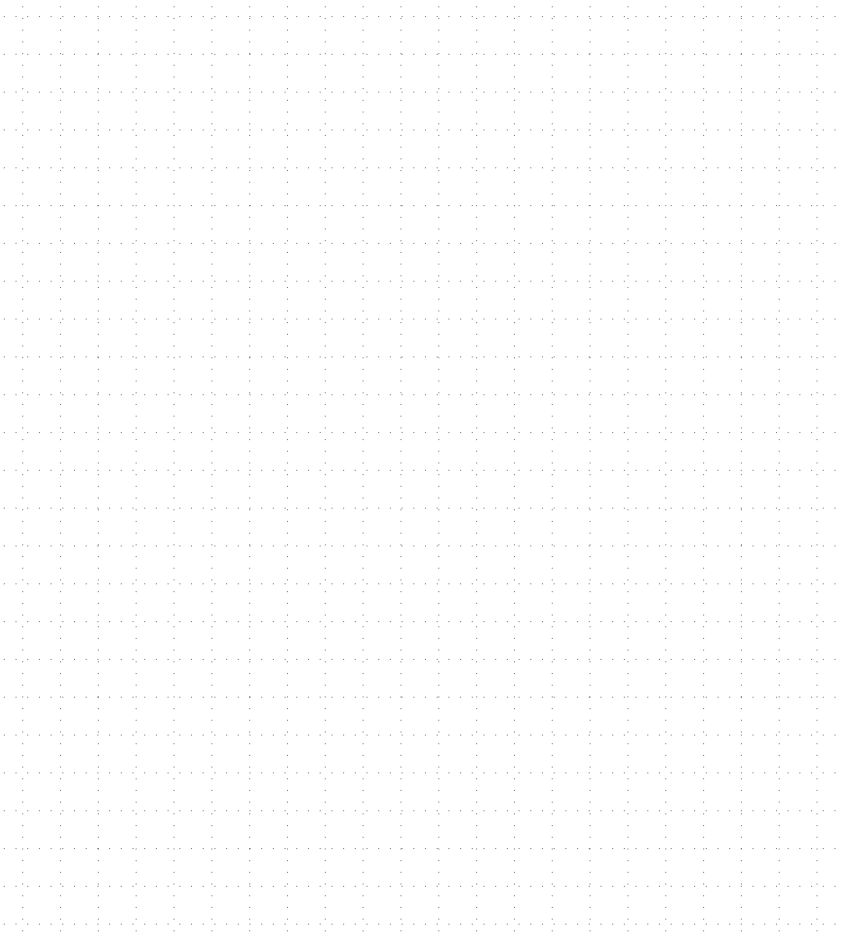
Global Placement

- Analytical approaches express a cost function and the constraints as analytical functions of the coordinates the standard cells and then use optimization techniques to reduce the overall cost
- Quadratic placement algorithm uses the sum of the squared Euclidean distances between standard cells and fixed pins

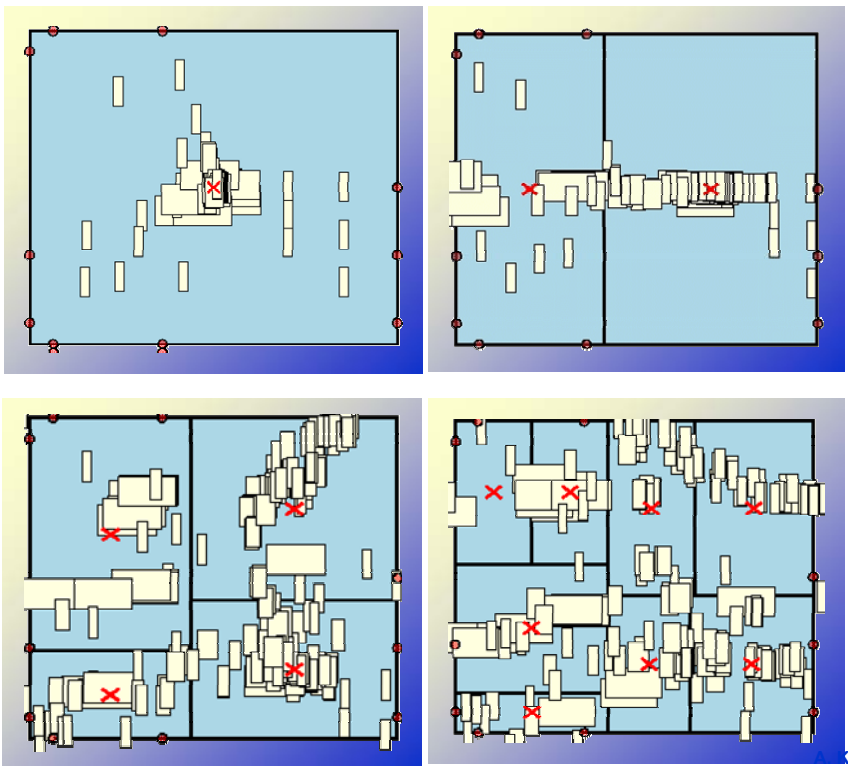
$$\text{Cost} = \sum_{(i,j)\in E} \left((x_i - x_j)^2 + (y_i - y_j)^2 \right)$$

- Consider netlist with two fixed pins and two INVX1 standard cells

- Consider netlist with three fixed pins, NAND2X1, and INVX1 standard cells



- Recursive analytical placement helps spread out cells
  - Initial analytical placement
  - Sort cells by x-coord, first half in left region, second half in right region
  - Add fixed anchor at center of left region for every cell in left region
  - Add fixed anchor at center of right region for every cell in right region
  - Redo analytical placement across all cells



Detailed Placement

- Legalization
  - Convert global placement into valid standard-cell layout
  - Snap cells to sites
  - Remove overlaps
  - Keep cells close to original positions
- Local Optimization
  - Small cell swaps or reorder cells within a row
  - Fix wirelenth or minor congestion