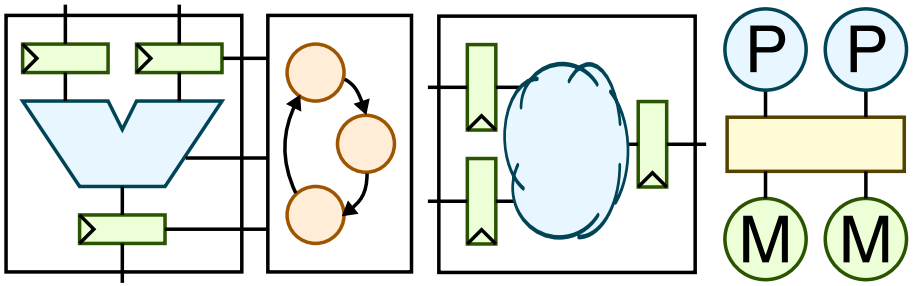
ECE 6745 Complex Digital ASIC Design Topic 7: Packaging, Power Distribution, Clocking, and I/O

Christopher Batten

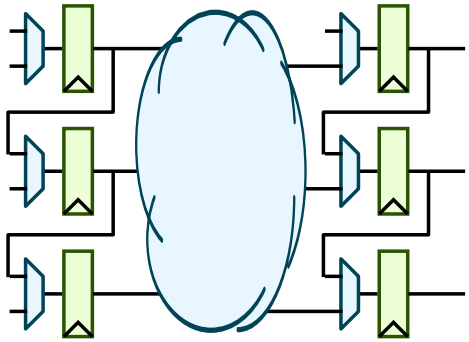
School of Electrical and Computer Engineering
Cornell University

http://www.csl.cornell.edu/courses/ece6745

Part 1: ASIC Design Overview



Topic 1
Hardware Description Languages

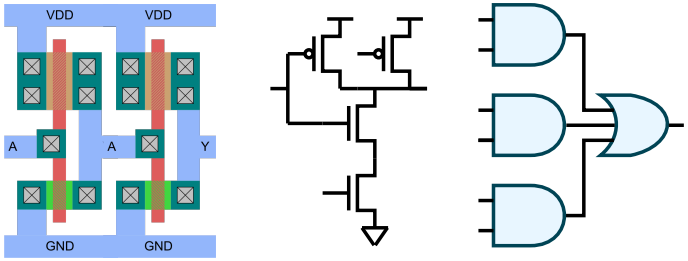


Topic 8
Testing and Verification

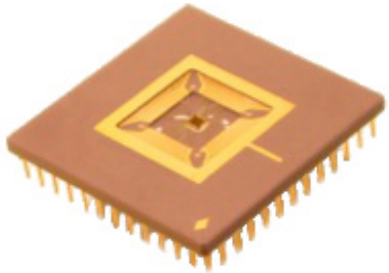
Topic 4
Full-Custom Design Methodology

Topic 6
Closing the Gap

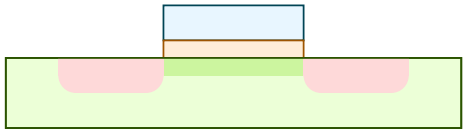
Topic 5
Automated Design Methodologies



Topic 3
CMOS Circuits



Topic 7
Clocking, Power Distribution, Packaging, and I/O



Topic 2
CMOS Devices

Agenda

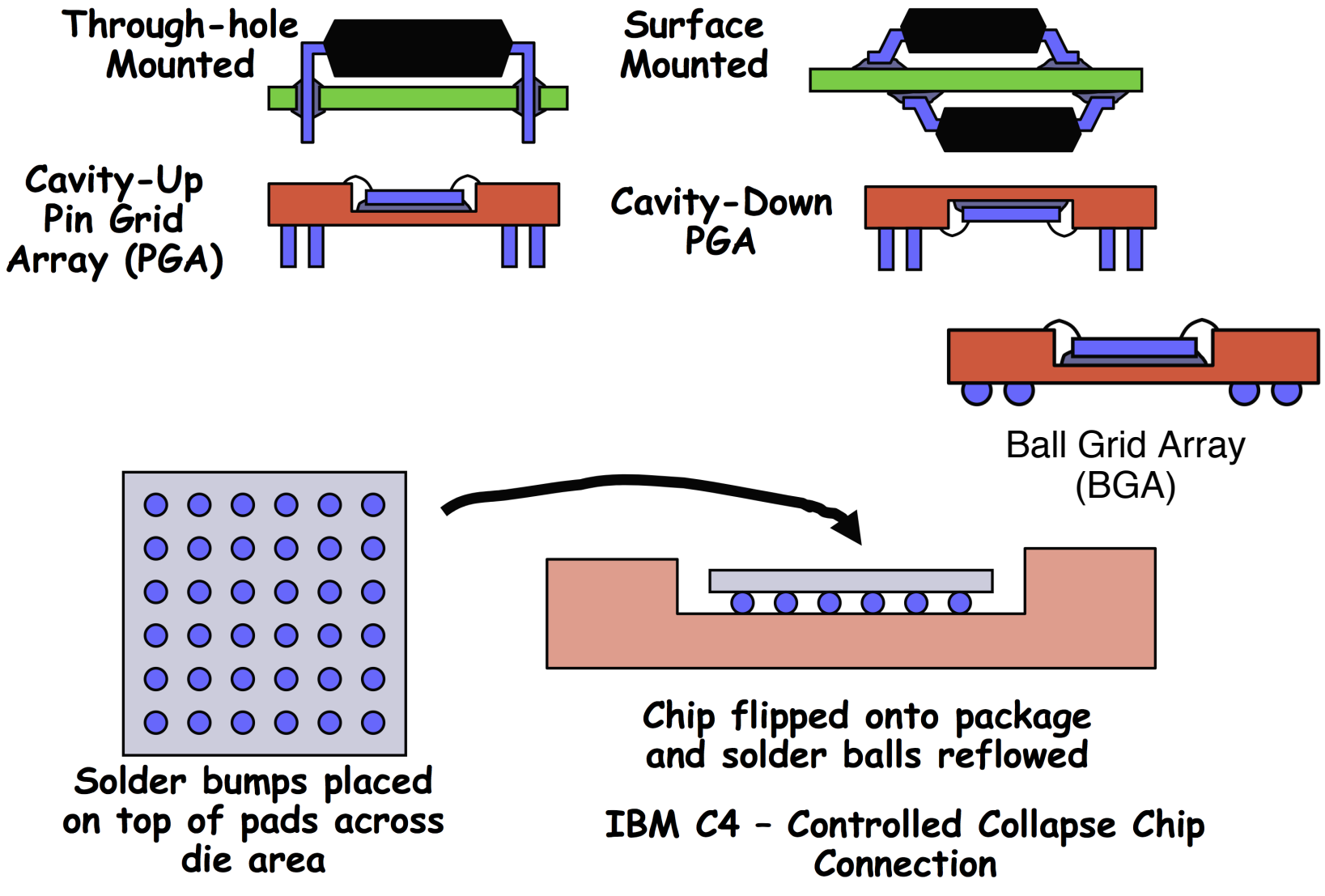
Packaging

Power Distribution

Clocking

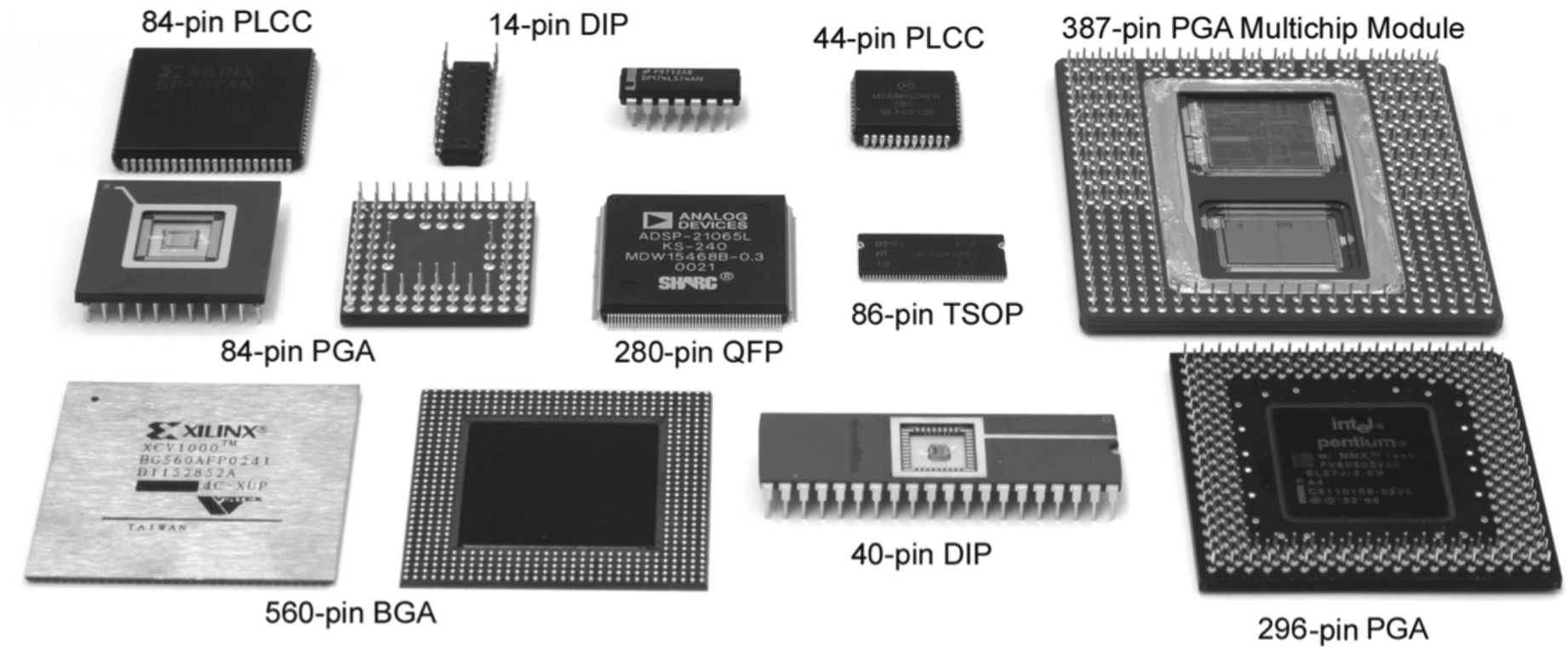
I/O

Basic Approaches to Packaging



Adapted from [Terman'02]

Basic Package Types



What makes a good package?

- Low cost
- Small size
- Good thermal performance
- Large number of pins
- Low pin parasitics
- Easy to test
- Highly reliable

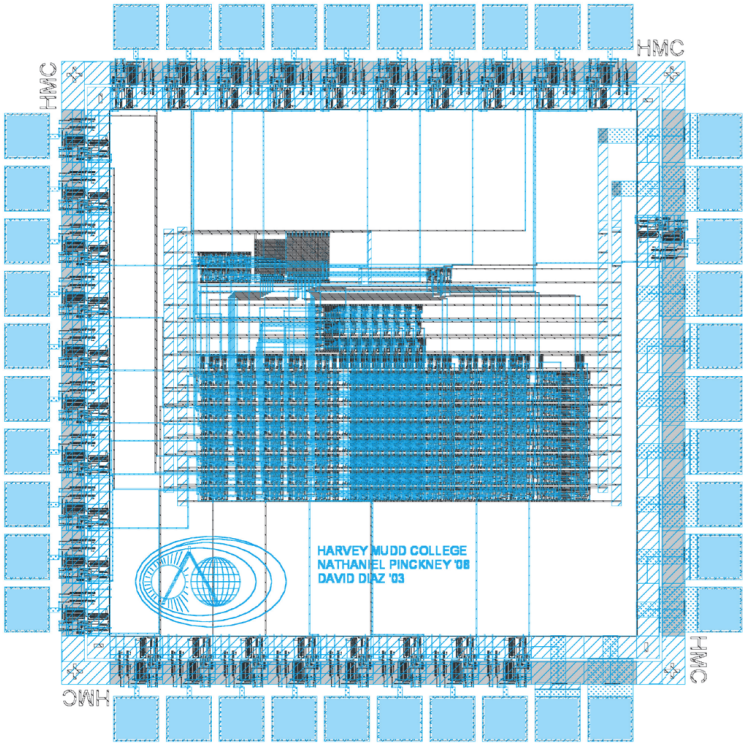
Adapted from [Weste'11]

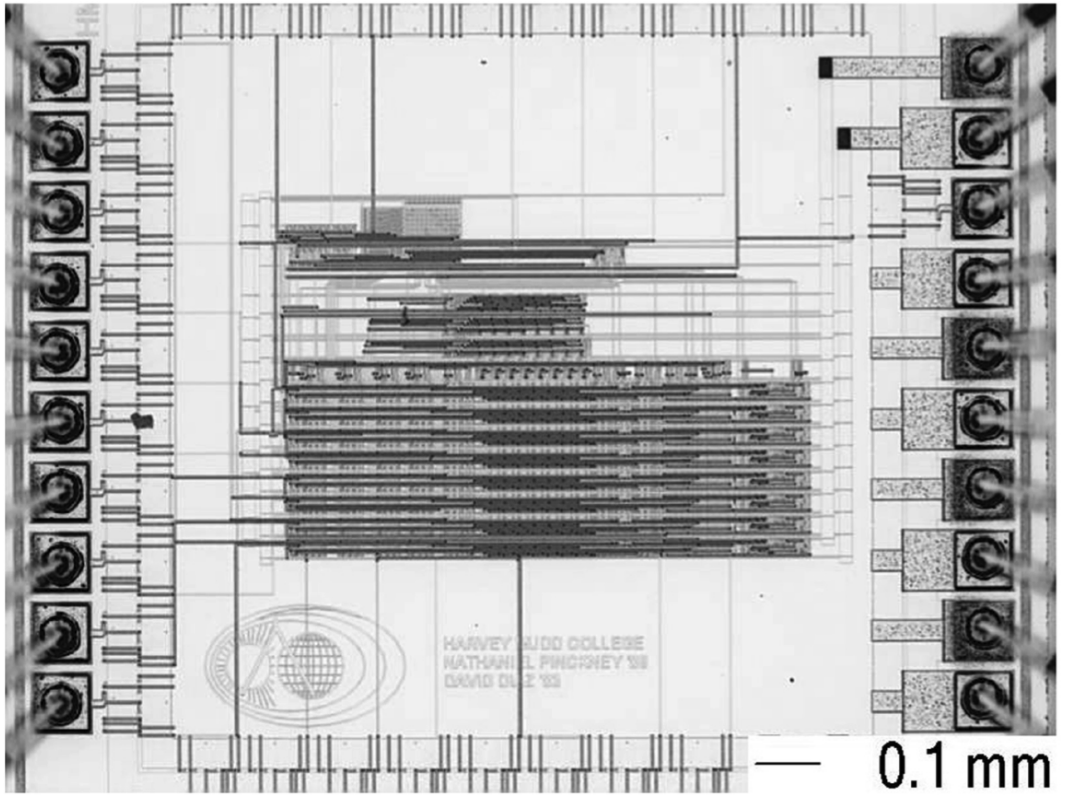
Basic Package Types

DIP	8–64	Two rows of through-hole pins. 100mil pitch. Low cost. Long wires between chip and corner pins.
PGA	65-400	Array of through-hole pins. 100mil pitch. Low thermal resistance and higher pin counts.
SOIC	8–28	Two rows of SMT pins. 50mil pitch. Low cost.
TSOP	28–86	Two rows of SMT pin. 0.5–0.8mil pitch in thin package. Used in DRAMs.
QFP	44–240	SMT pins on 4 sides. 15–50mil pitch. High density.
BGA	49–2000+	Array of SMT solder balls on underside of package on 15–50mil pitch. Very high density with low parasitics. Costly assembly.
LGA	Many	Similar to BGA but with gold pads instead of solder balls. Commonly used with sockets (processors).

Adapted from [Weste'11]

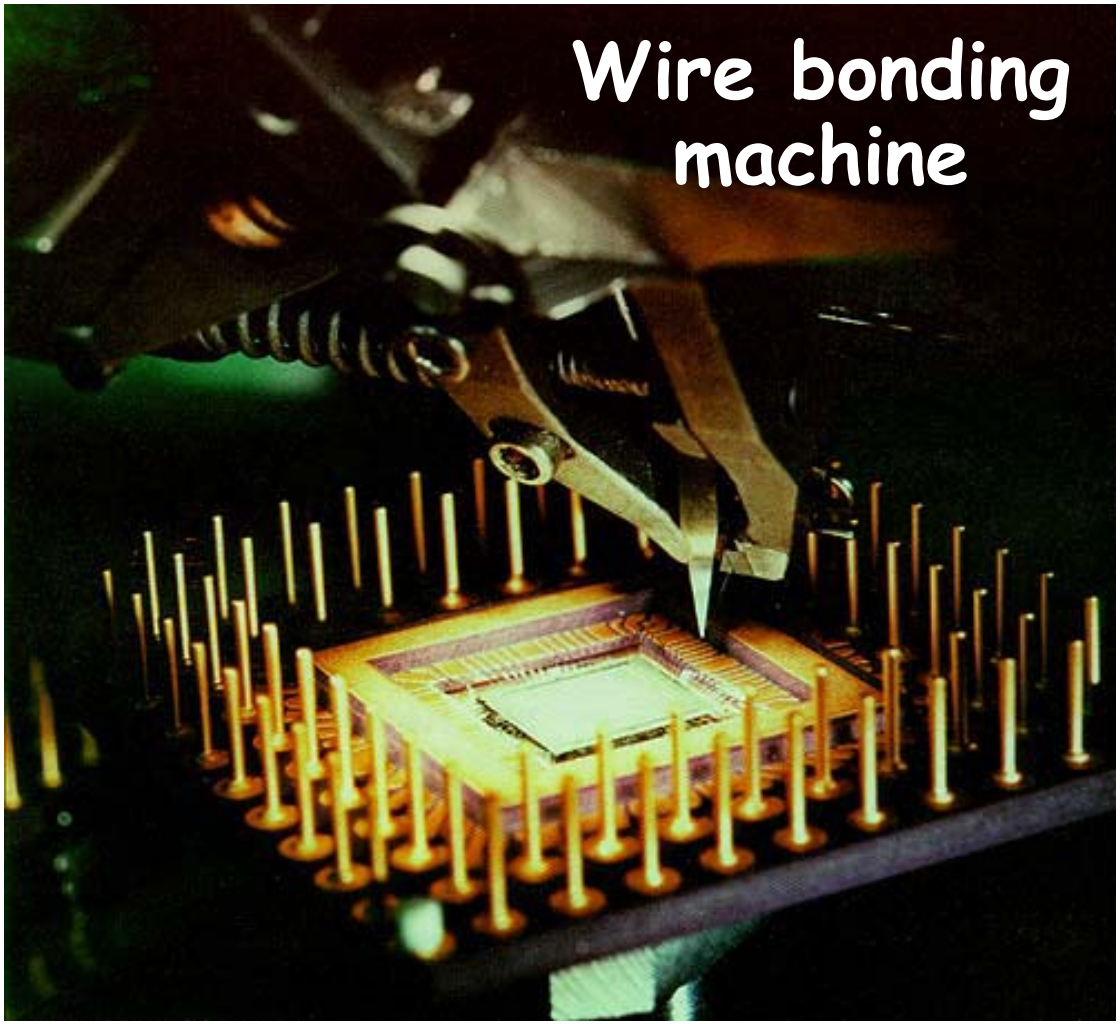
Wire-Bond Pad Ring





Adapted from [Weste'11]

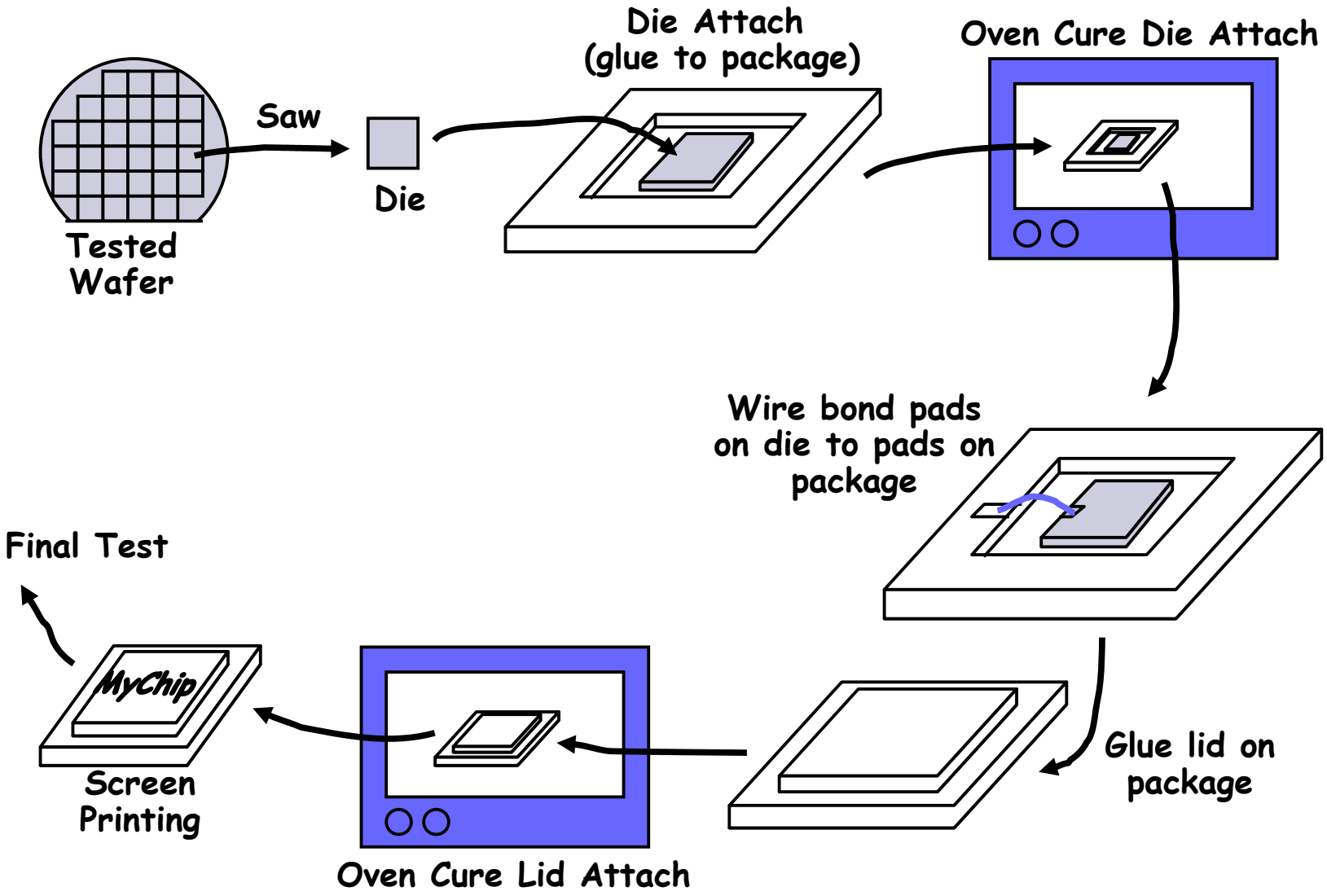
Wire Bonding Process



- Usually ultrasonic welding connects wire to package and die pad
- Bond wires can be aluminum or gold
- Different thicknesses of bond wire tradeoff parasitic inductance and resistance versus density
- Can wirebond to die pad pitches of around 100μm

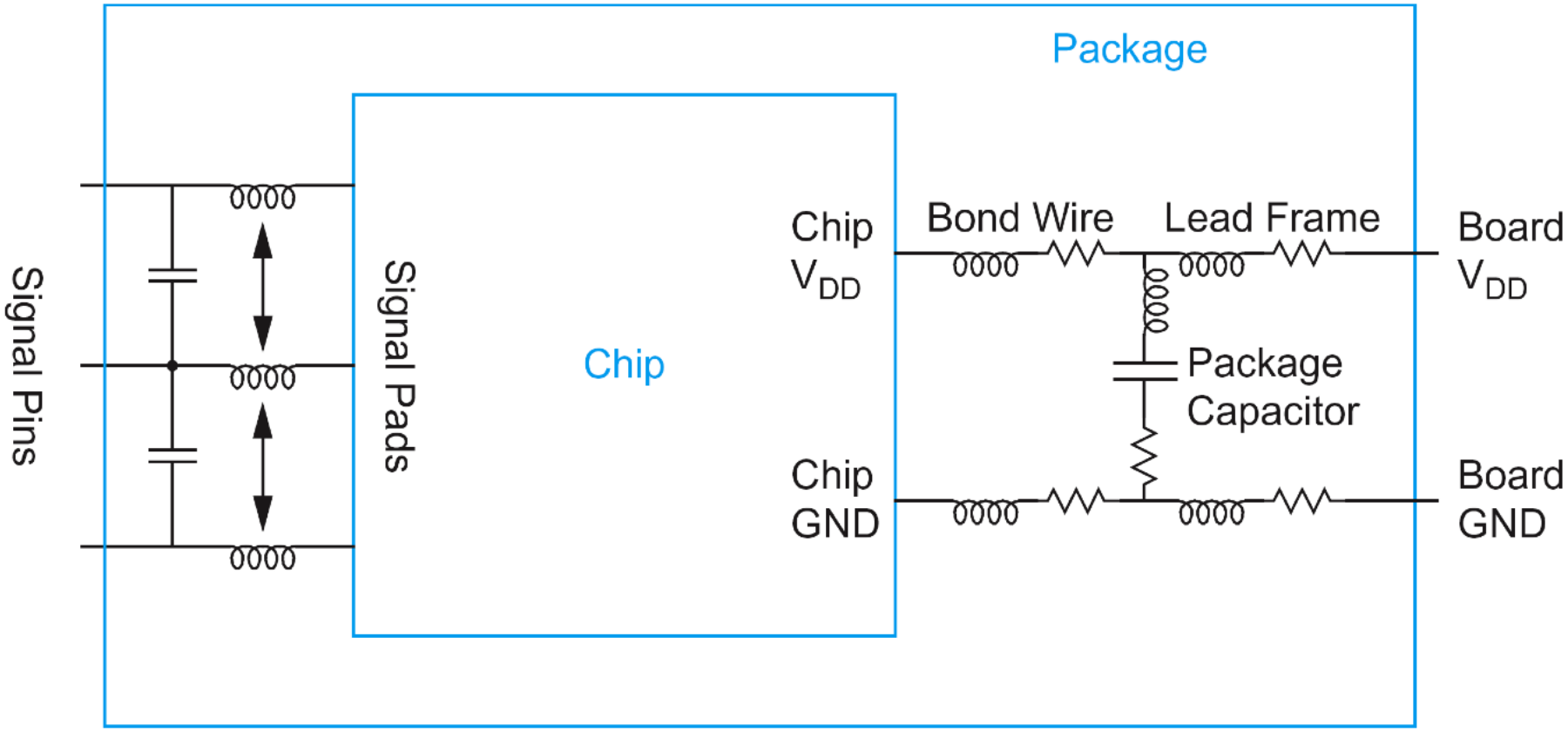
Adapted from [Terman'02]

Pin-Grid Array Assembly Process



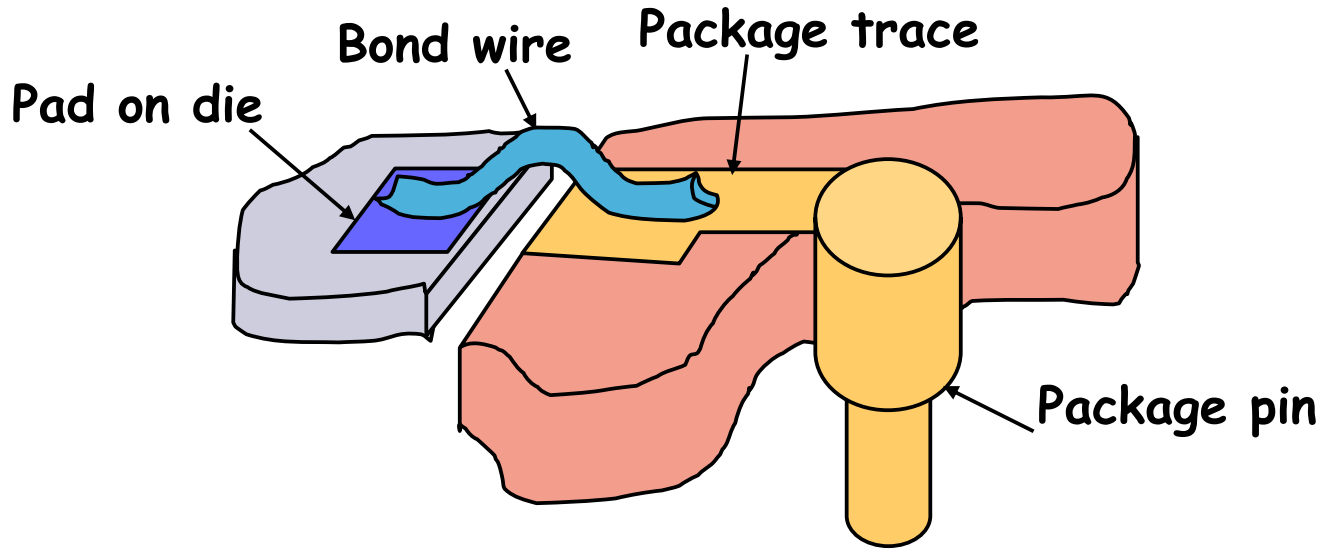
Adapted from [Terman'02]

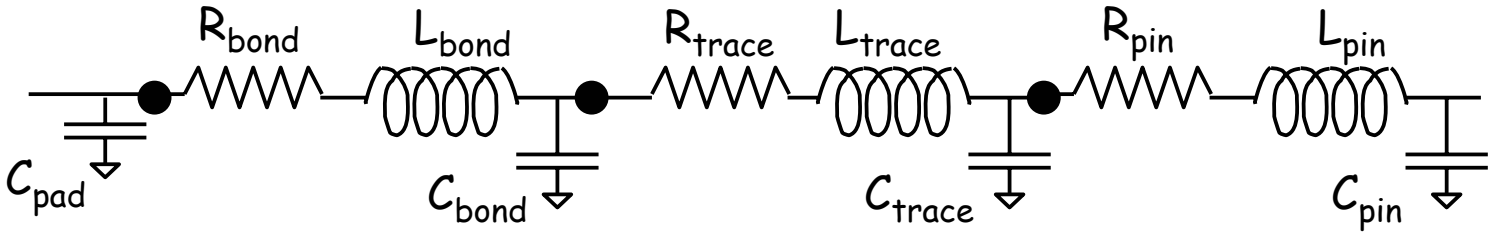
Summary of Package Parasitics



Adapted from [Weste'11]

Pin Parasitics





Wire bond, C_{bond}=1pF, L_{bond}=1nH

- bond wire L approx. 1nH/mm

Solder bump, C_{bond}=0.5pF, L_{bond}=0.1nH

68-pin DIP, C_{pin}=4pF, L_{pin}=35nH

256-pin PGA, C_{pin}=3-5pF, L_{pin}=5-15nH

BGA, C_{pin}=2-4pF, L_{pin}=1-8nH

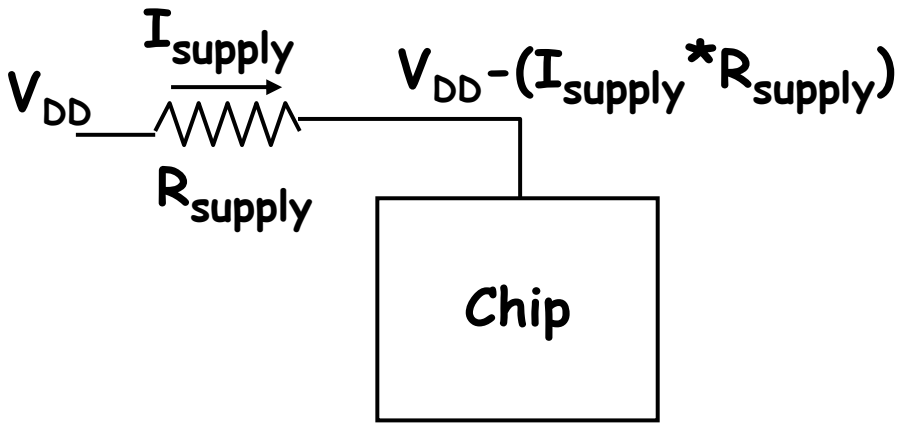
Adapted from [Terman'02]

Challenge: Power Delivery Scaling

$$\text{Power} = \text{Volts} \times \text{Amps}$$

- CPU power consumption is increasing
  - 2x per technology generation
- Supply voltages are dropping
  - have to control electric field strength as transistors shrink
  - keep power from growing even faster
- Power is going up, voltage is going down = current rising fast
  - 100W at 1V implies 100A of current

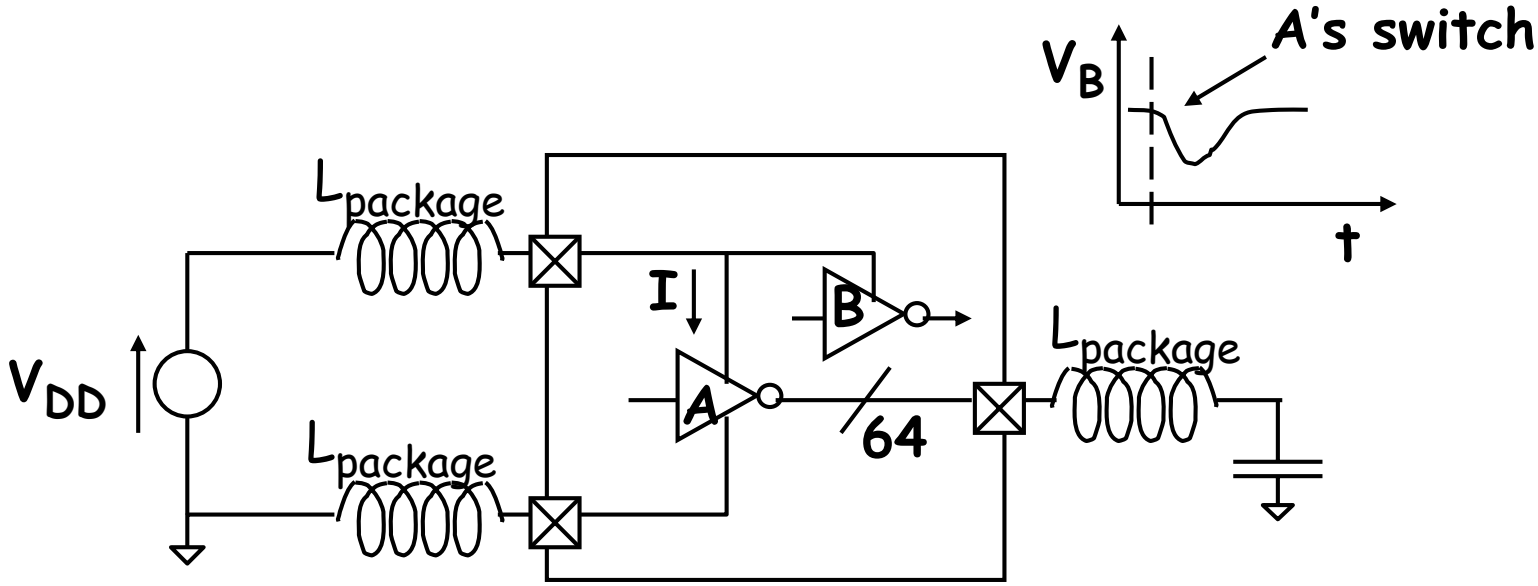
Challenge: Static IR Droop



- Want to keep voltage droop (V = IR) small
- Example, for 100W@1V, I=100A
  - 5% droop is 50mV
  - At 100A, need effective supply resistance < 0.0005 Ω
  - Dissipate 5W heat just in power supply leads
- Use multiple parallel Vdd/GND pins
- Need very short fat wires to board power regulator
- Want very low resistance on-chip power network

Adapted from [Terman'02]

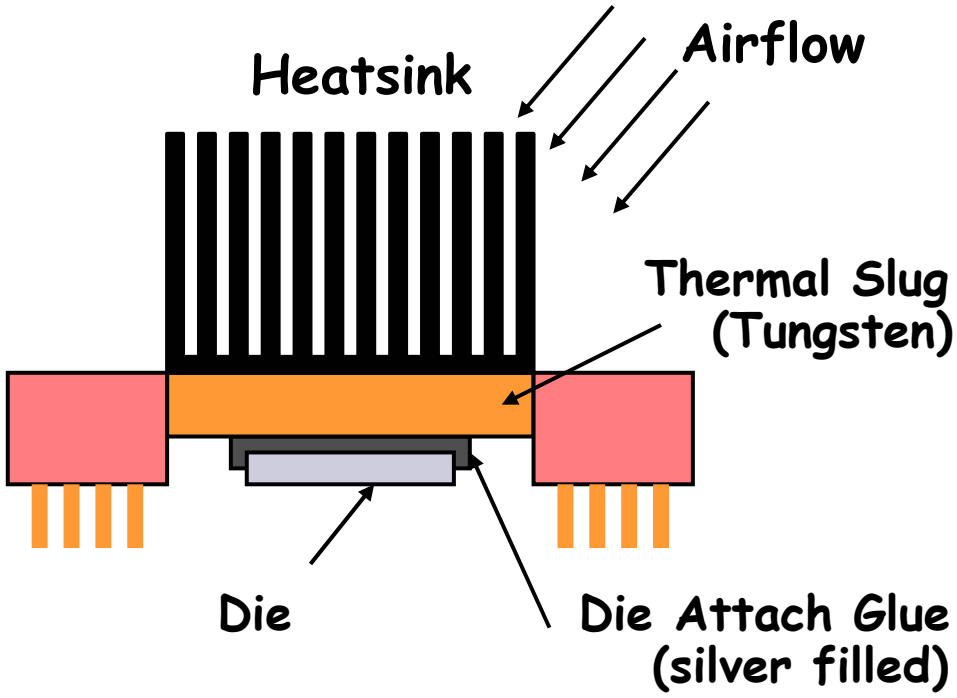
Challenge: Dynamic dI/dt Droop



- A large number of output drivers A switching high try to pull current through the power supply inductance, causing the internal power rail connected to gate B to droop (V=LdI/dt)
- Gates driven by B may switch incorrectly.

Adapted from [Terman'02]

Challenge: Heat Dissipation



Sample overall θ_{ja}:

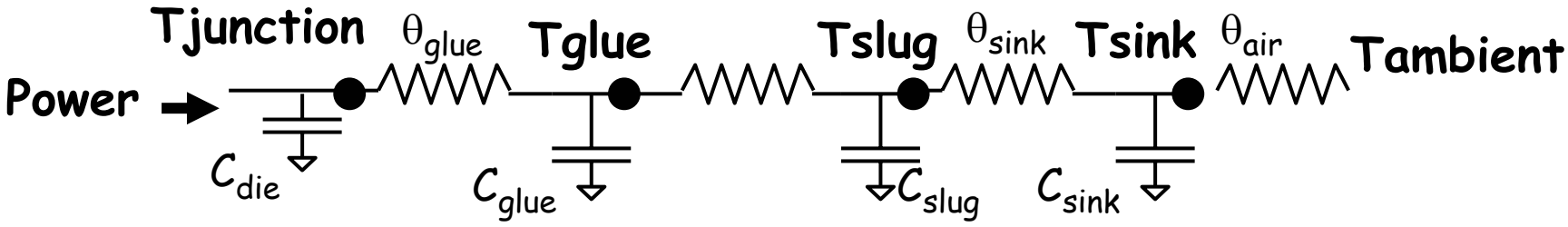
DIP 38°C/W still air

DIP 25°C/W forced air

PGA 5-10°C/W forced air

Microproc.and fan <3°C/W

(fluid pumped through die microchannels 0.02°C/W)



Adapted from [Terman'02]

Agenda

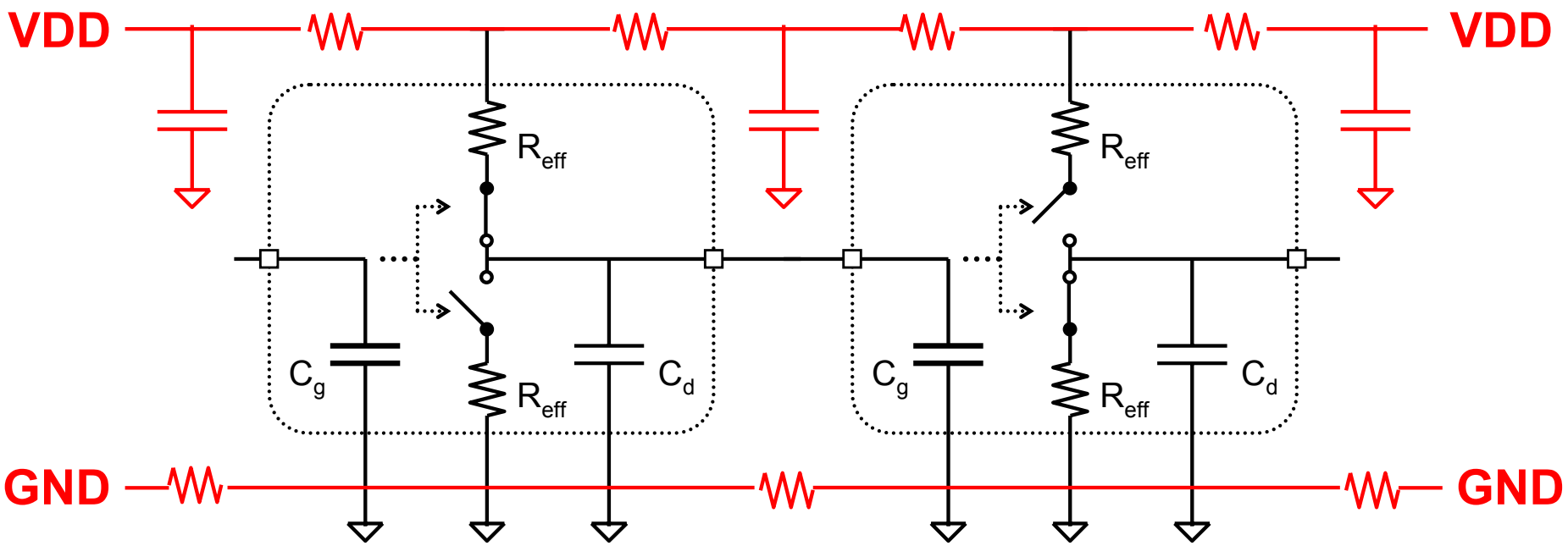
Packaging

Power Distribution

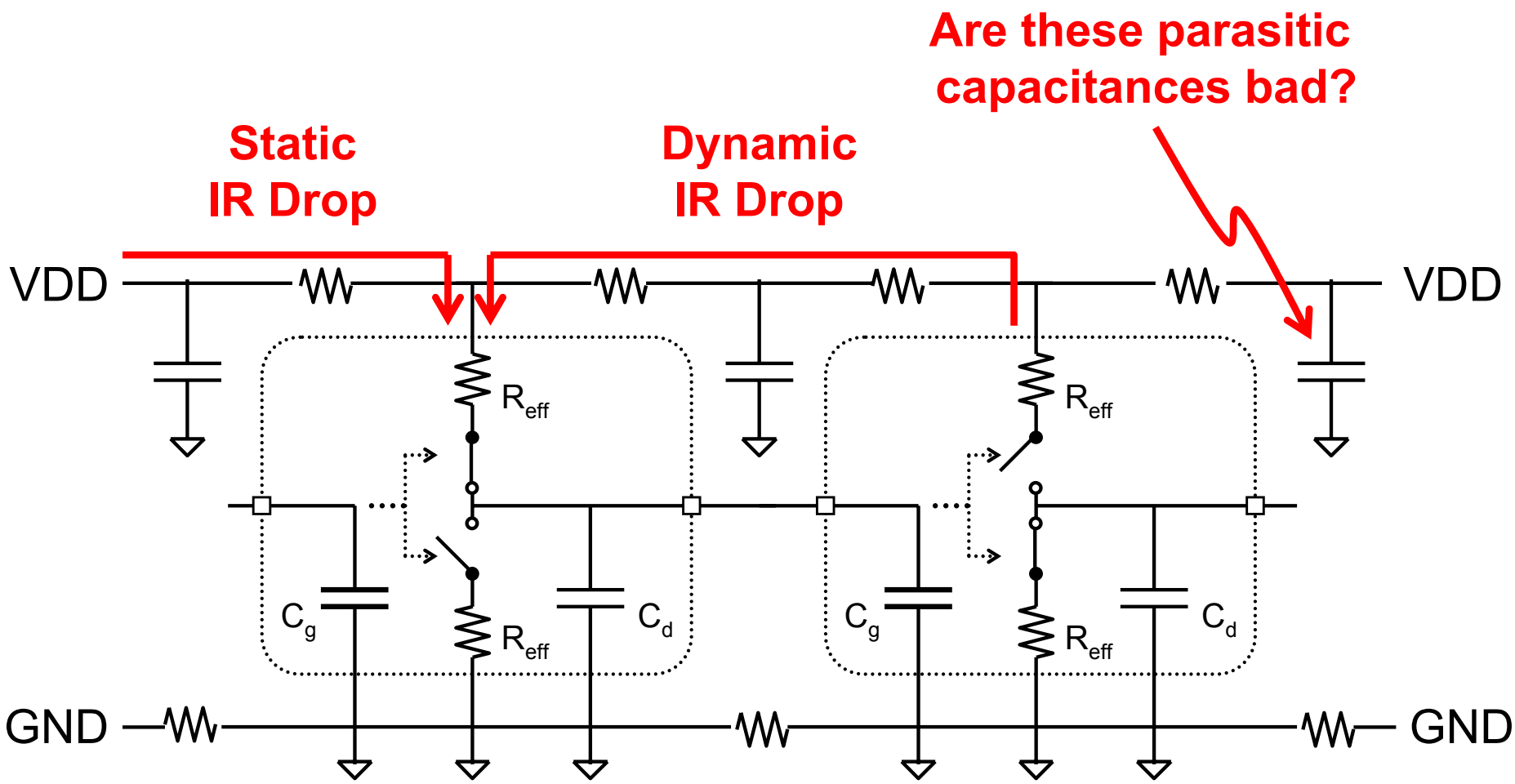
Clocking

I/O

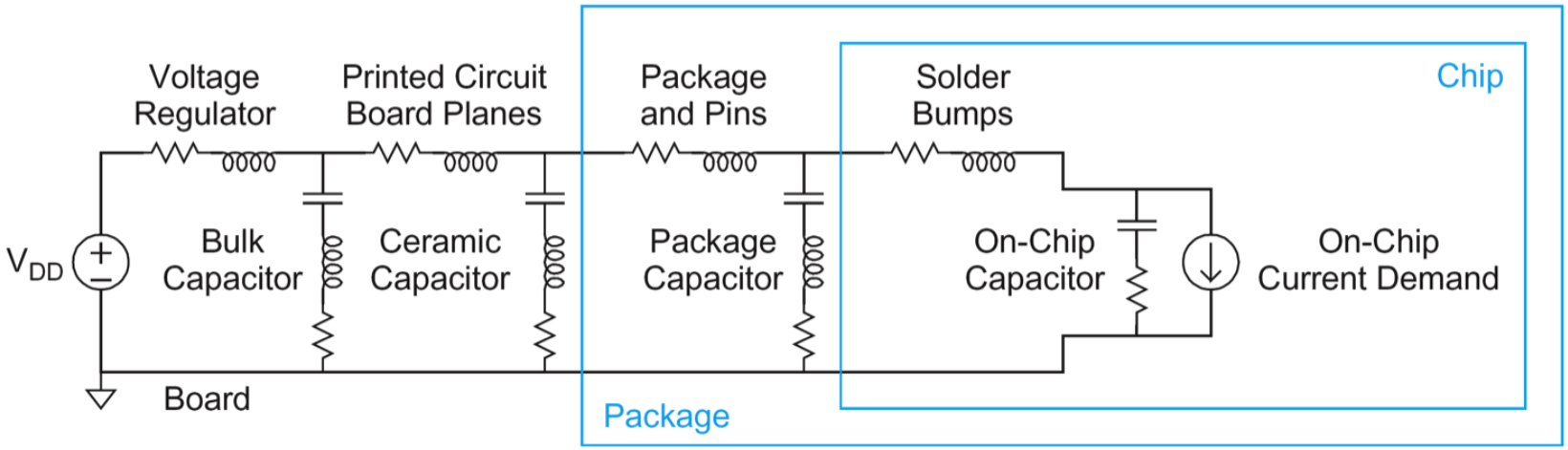
Power Distribution Network Parasitics

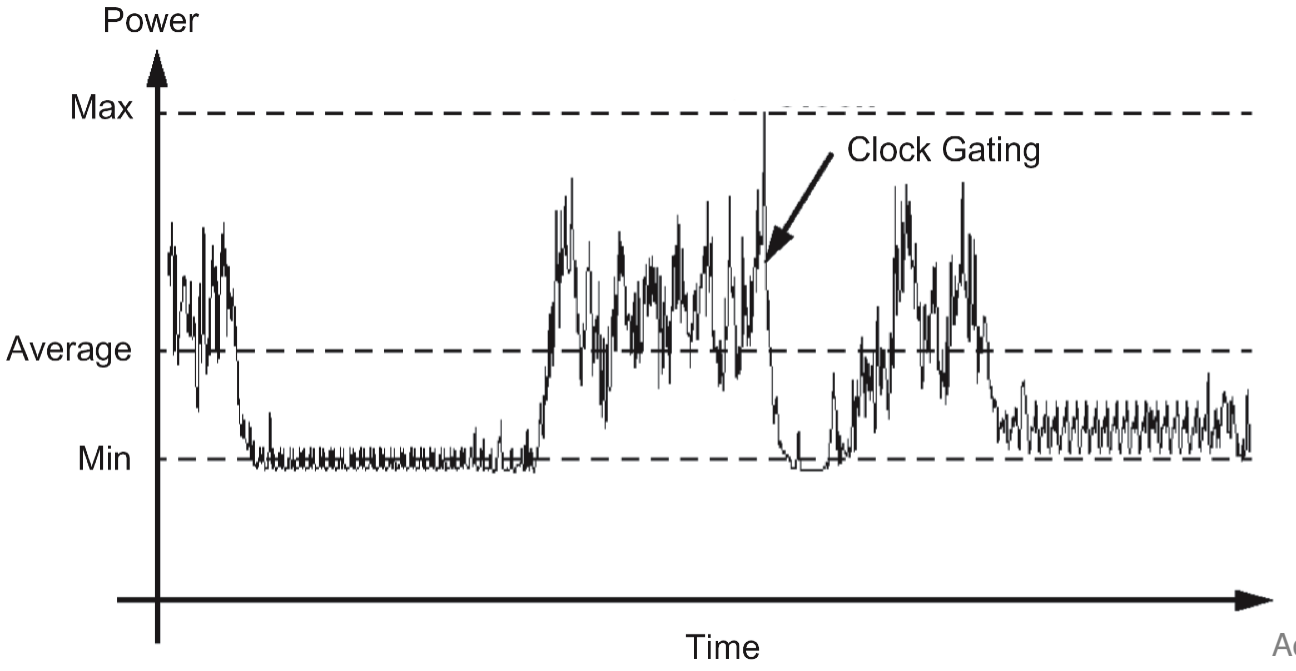


Static and Dynamic IR Drop



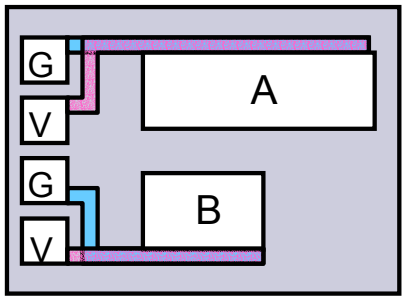
Realistic Power Distribution Networks



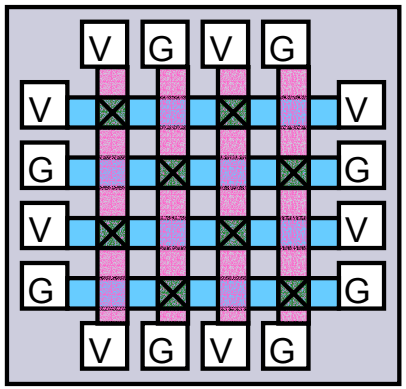


Adapted from [Weste'11]

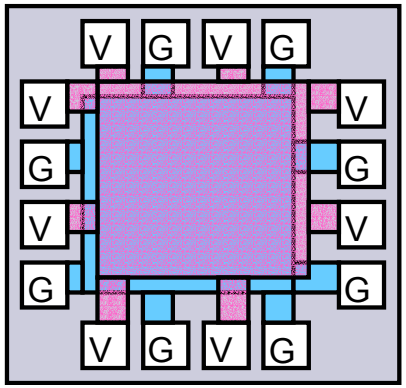
Various Approaches to Power Distribution



Routed power distribution on two stacked layers of metal (one for VDD, one for GND). OK for low-cost, low-power designs with few layers of metal.

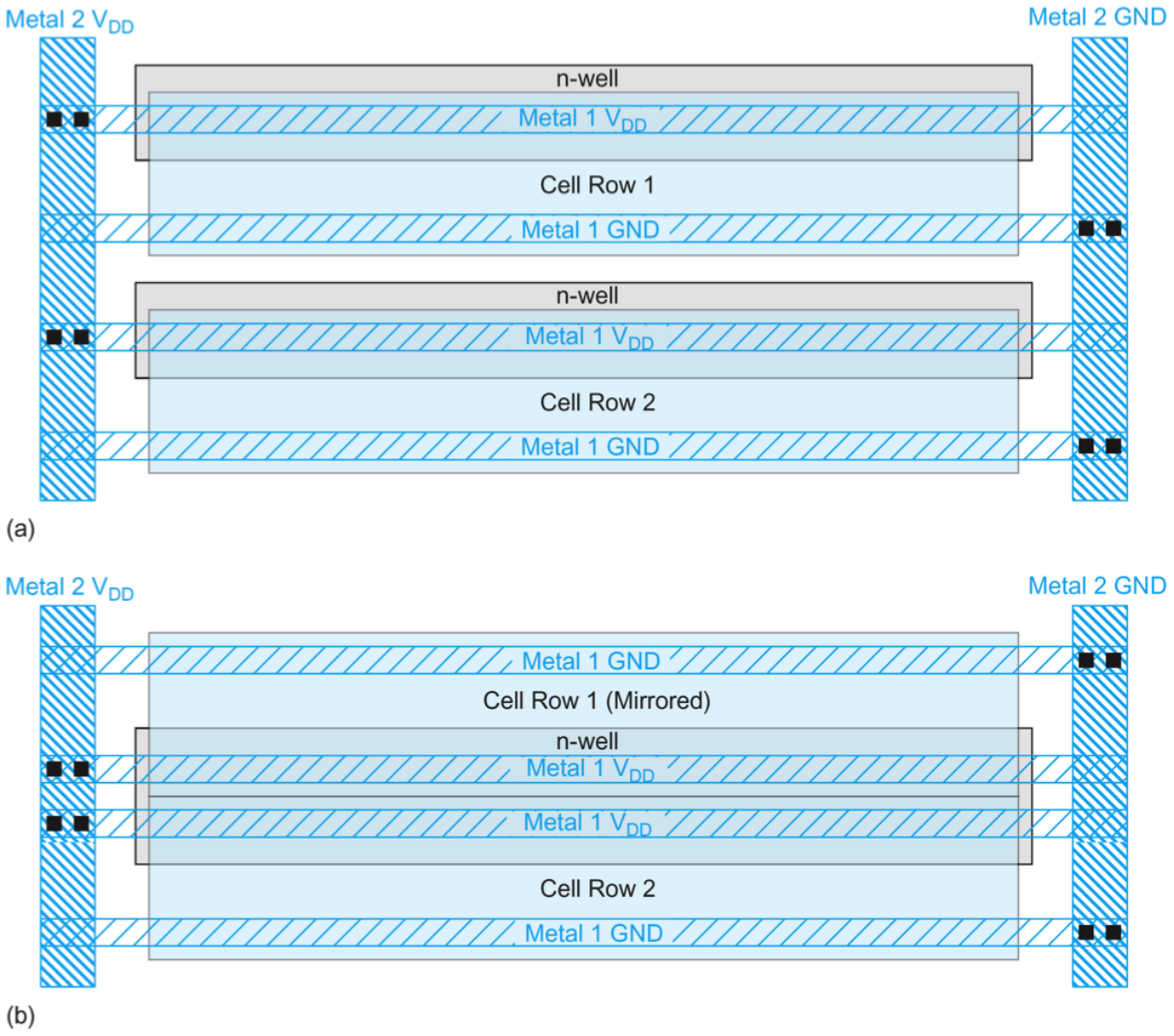


Power Grid. Interconnected vertical and horizontal power bars. Common on most high-performance designs. Often well over half of total metal on upper thicker layers used for VDD/GND.



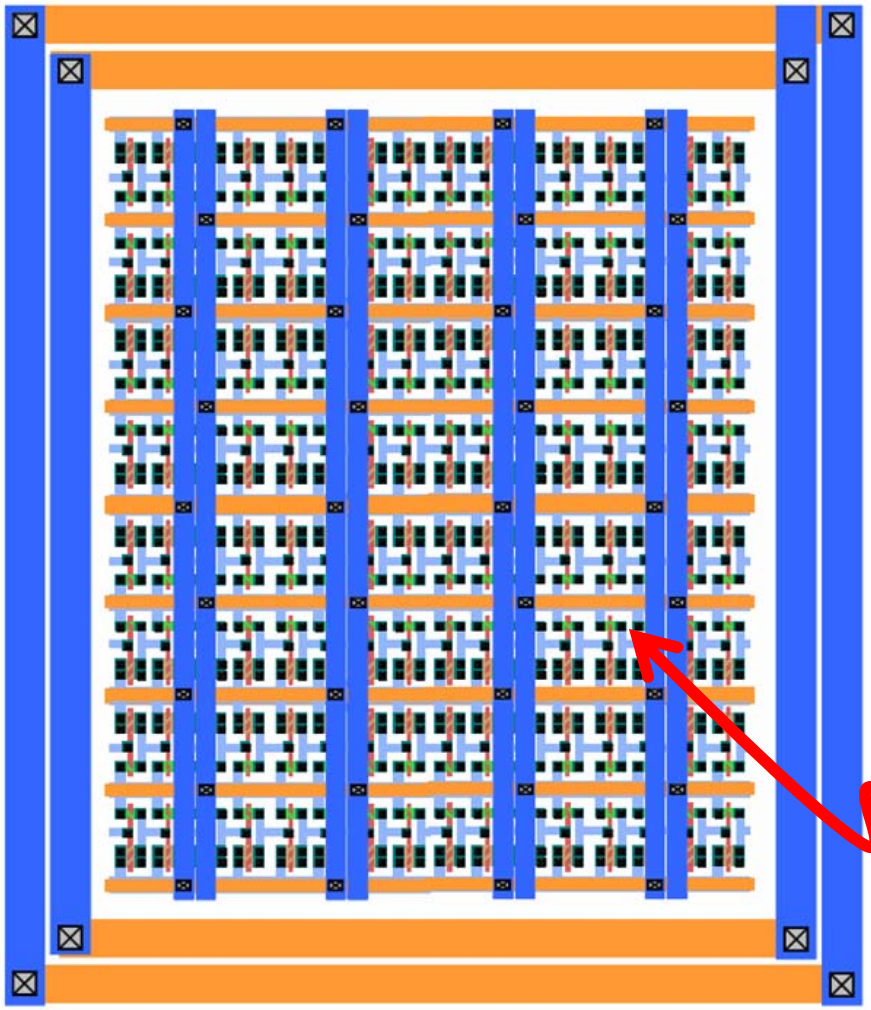
Dedicated VDD/GND planes. Very expensive. Only used on Alpha 21264. Simplified circuit analysis. Dropped on subsequent Alphas.

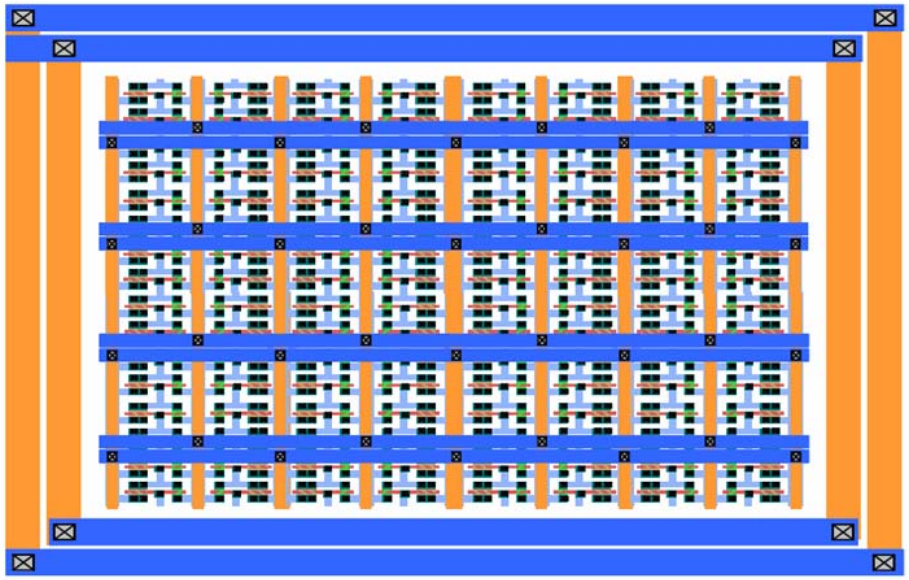
Power Distribution for Standard Cells



Adapted from [Weste'11]

Modular Power Distribution Networks

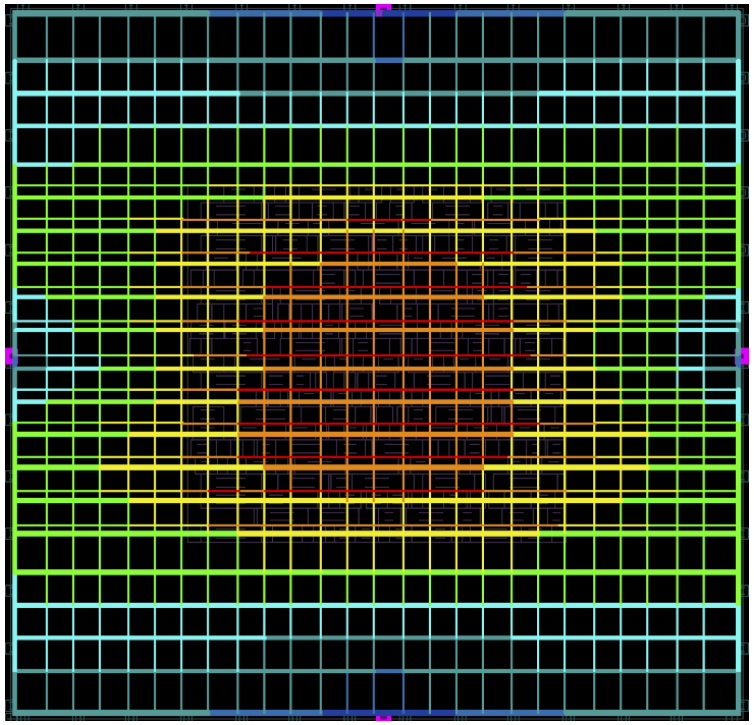


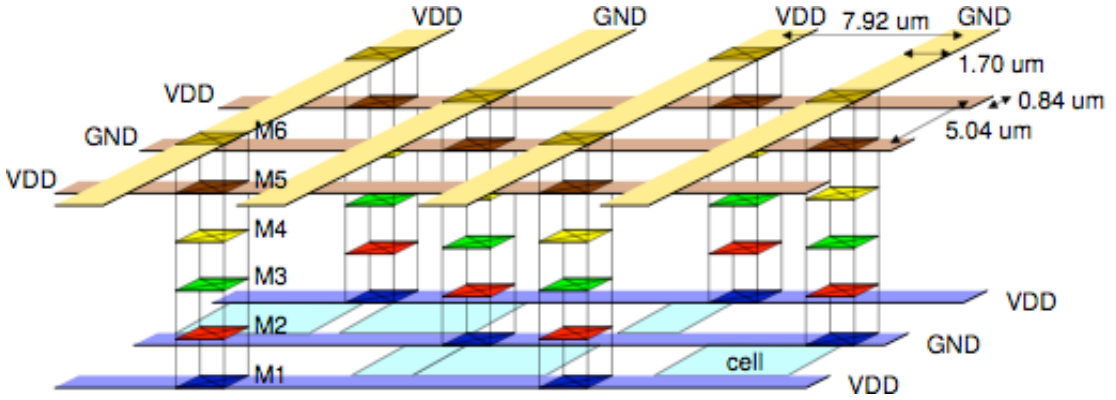


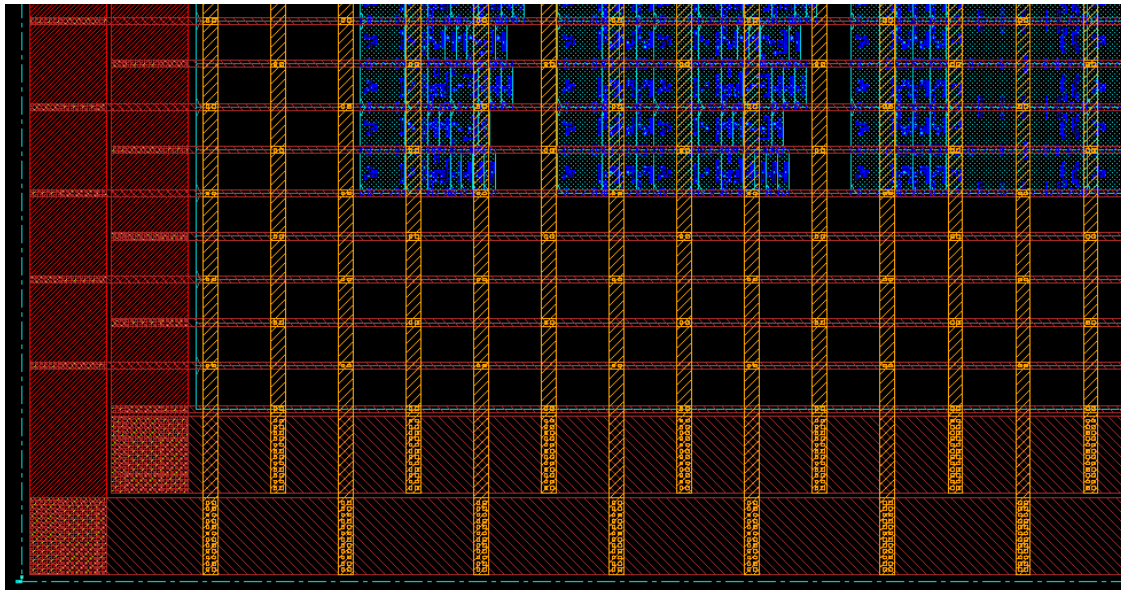
Early physical partitioning and prototyping is essential

Can use special filler cells to help add decoupling cap

Scale Power Distribution Network







Agenda

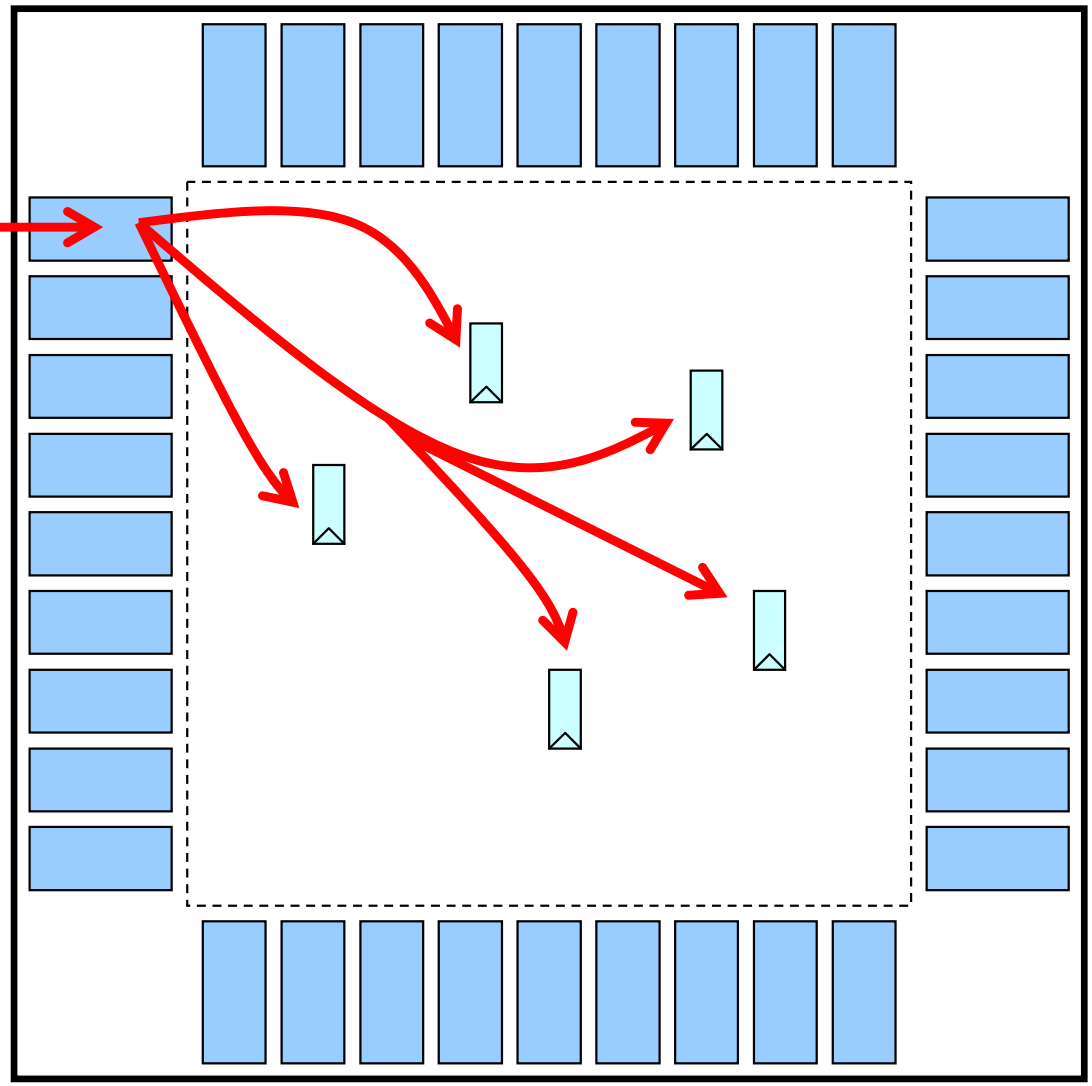
Packaging

Power Distribution

Clocking

I/O

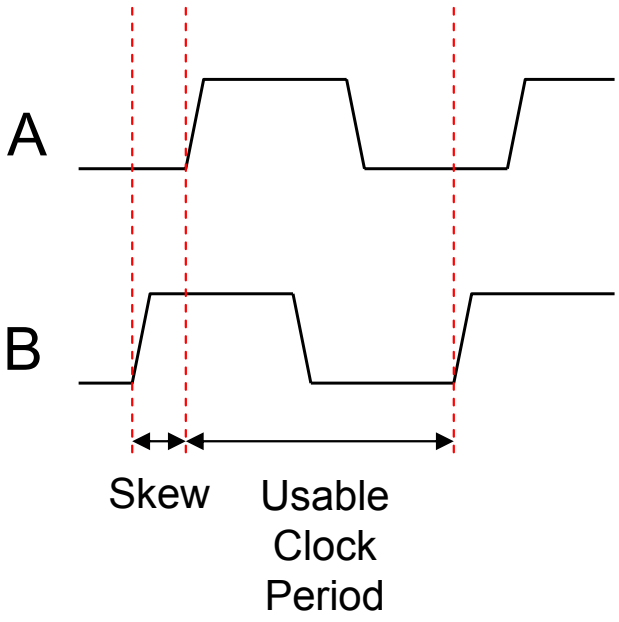
Goal of Clock Distribution

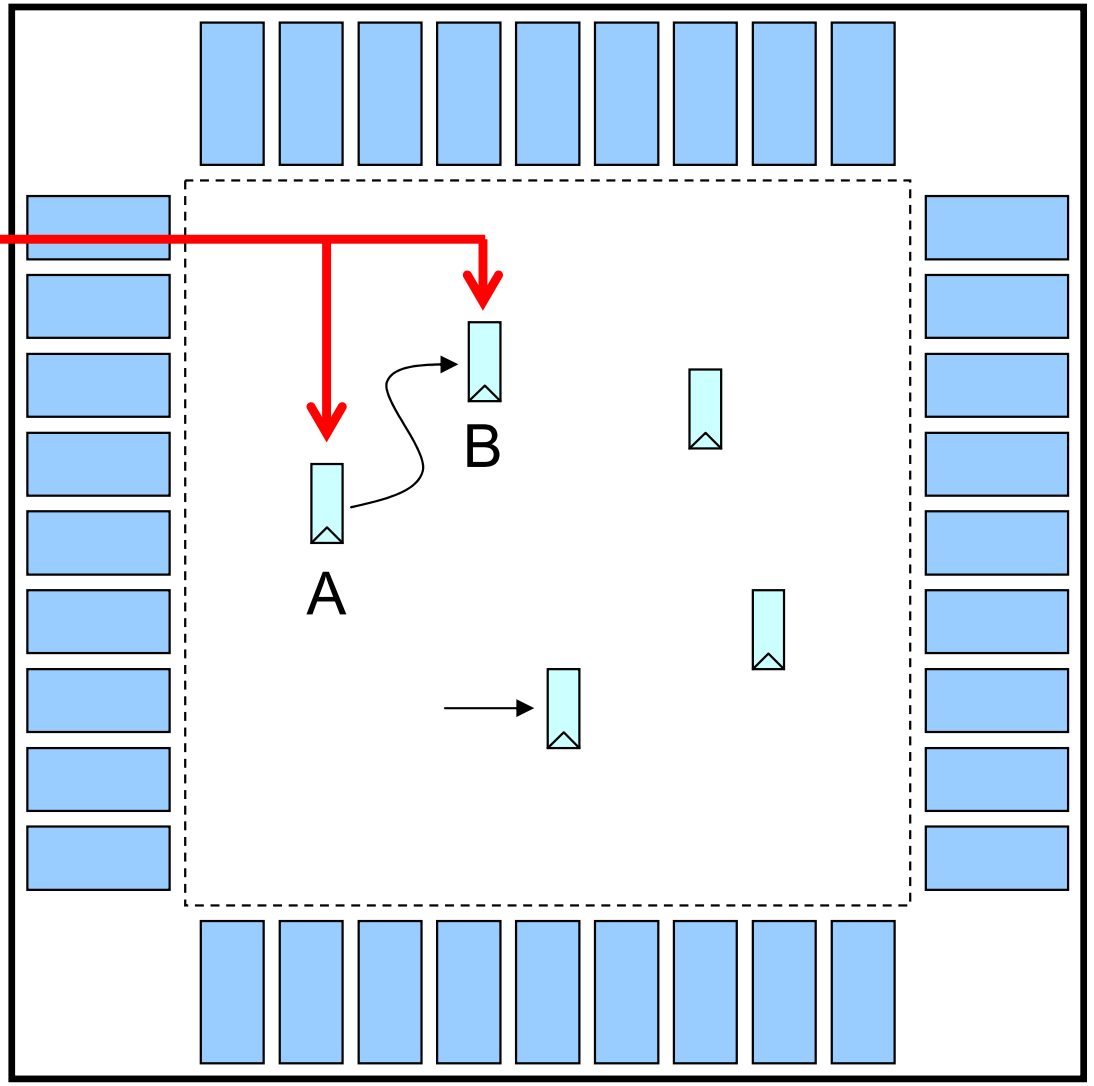


Cannot really distribute clock instantaneously with a perfectly regular period

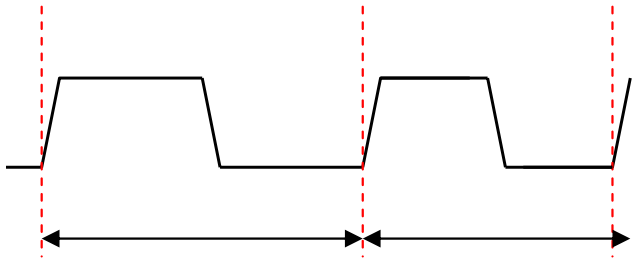
Clock Skew

Clock Skew
Difference in clock arrival time at two spatially distinct points

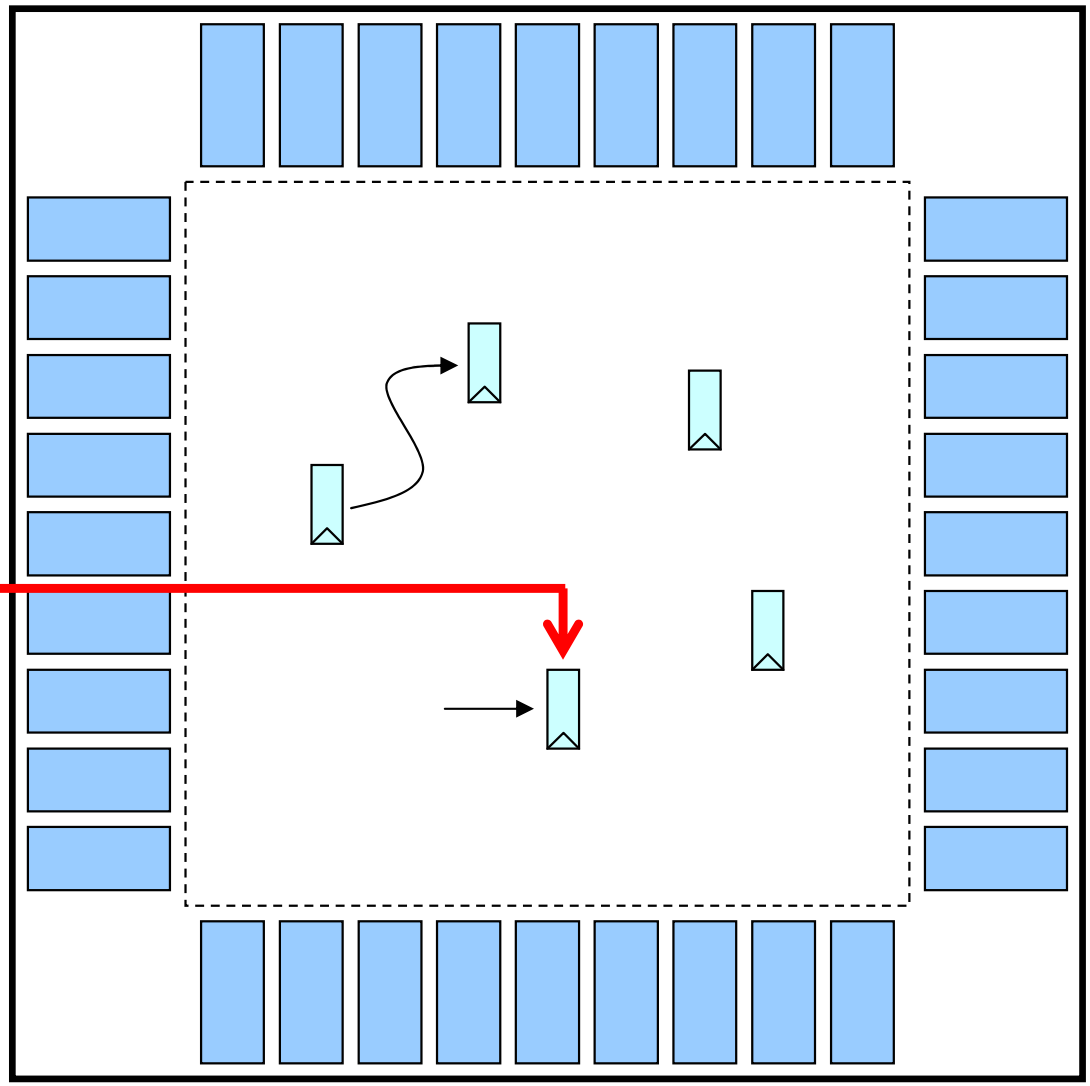




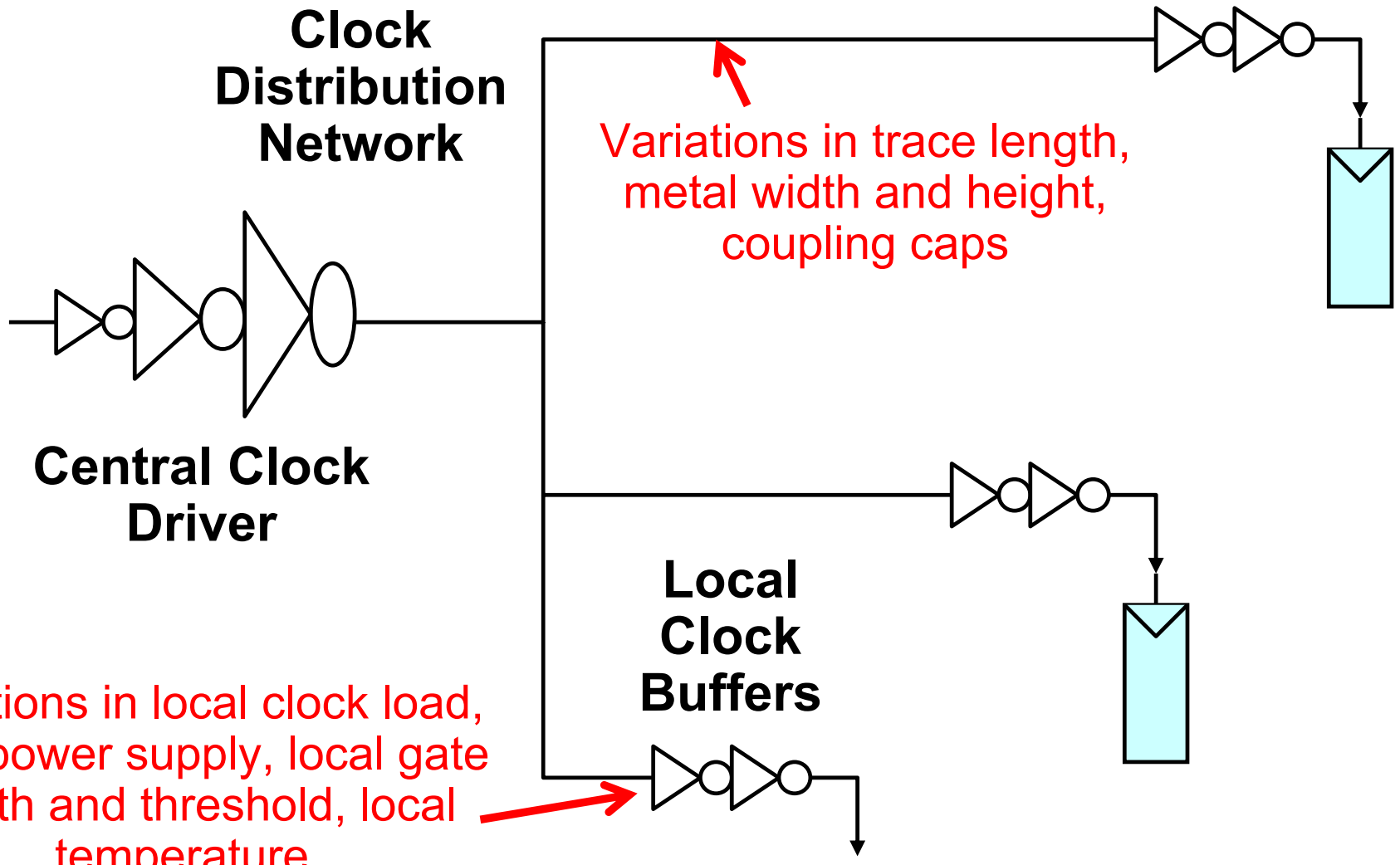
Clock Jitter



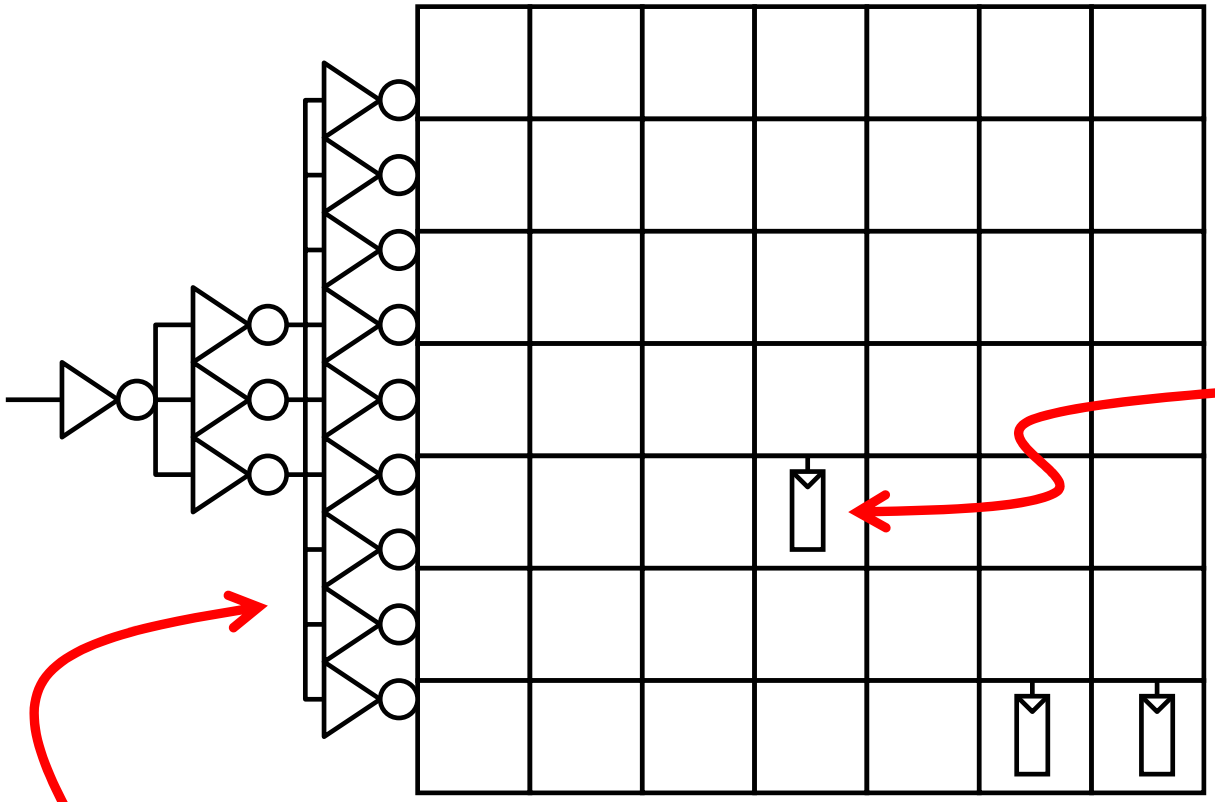
Clock Jitter
Difference in clock period over time



Sources of Clock Skew and Jitter



Clock Grids: Low Skew but High Power

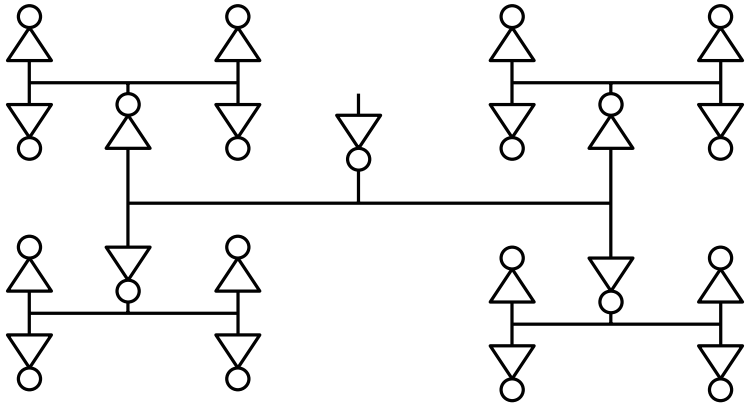


Grid feeds flops directly, no local buffers

Clock driver tree spans height of chip
Internal levels shorted together

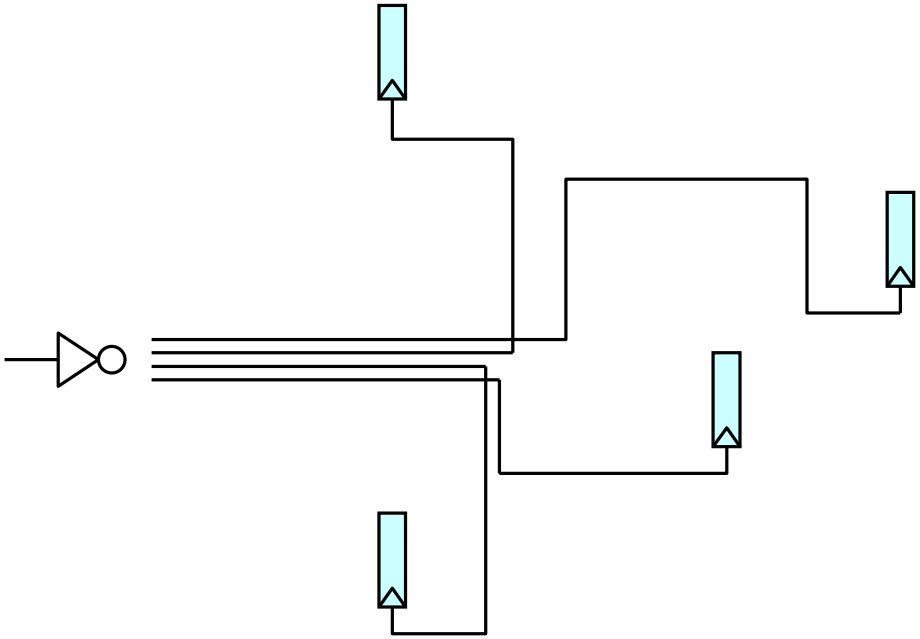
Clock Trees: More skew but Less Power

H-Tree



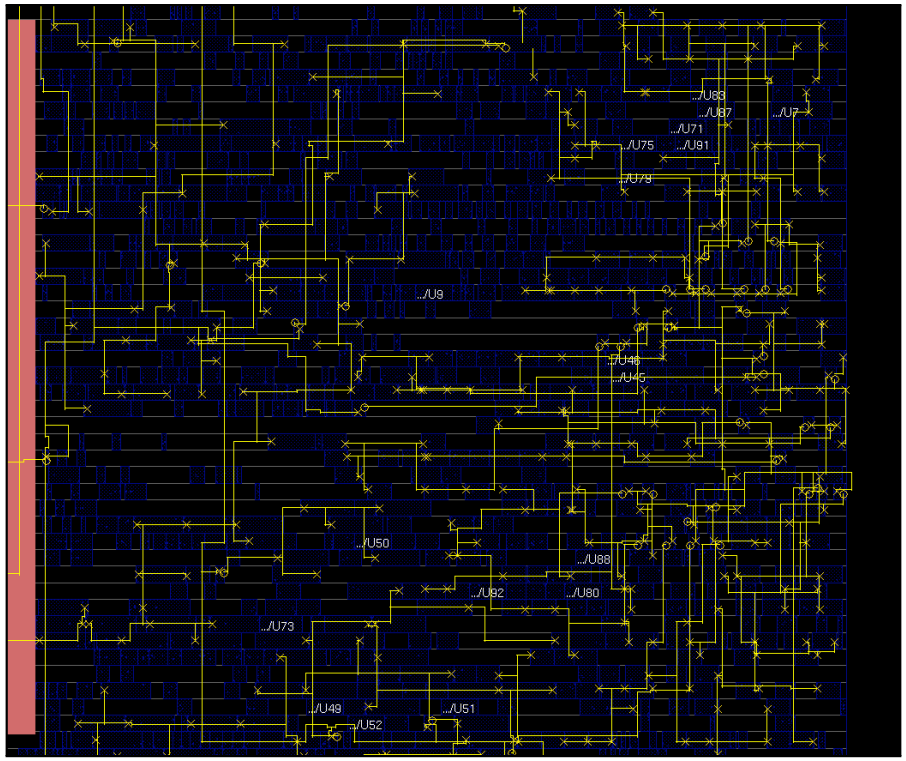
Recursive pattern to distribute signals uniformly with equal delay over area

RC-Tree

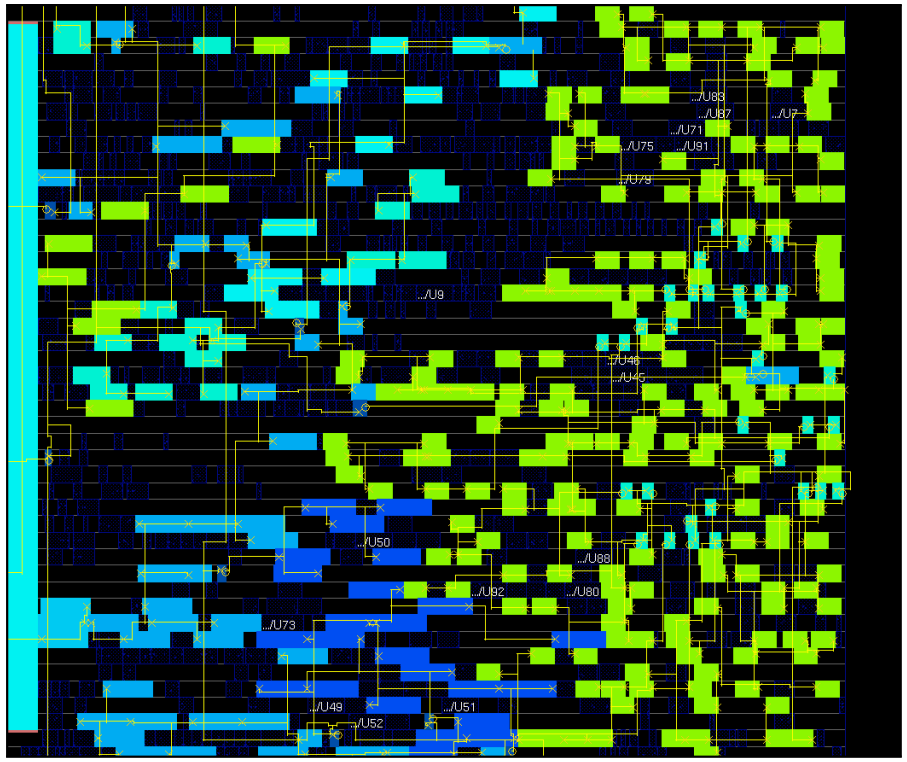


Each branch is individually routed to balance RC delay

Clock Tree Synthesis

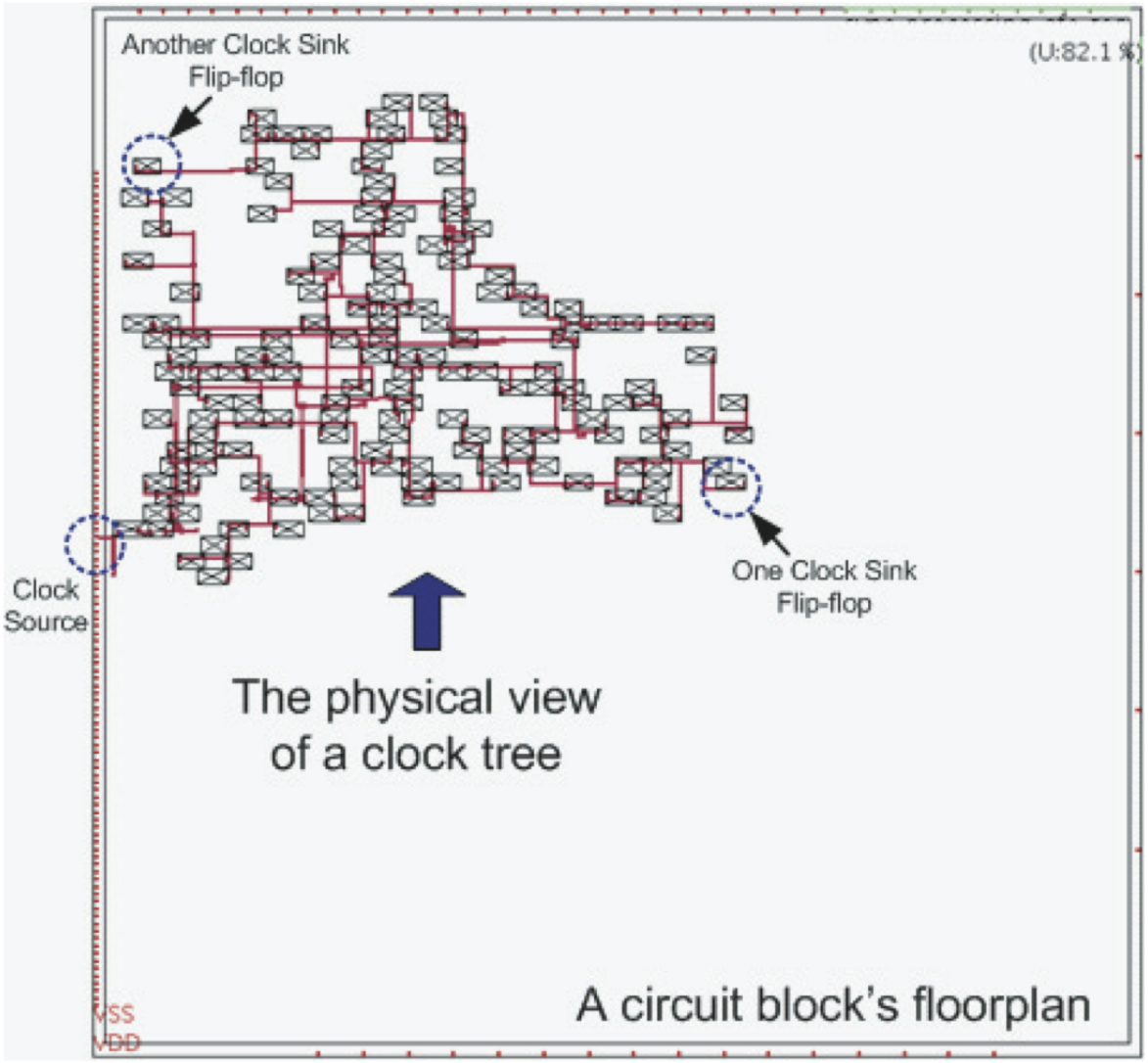


CAD tools generate balanced RC trees



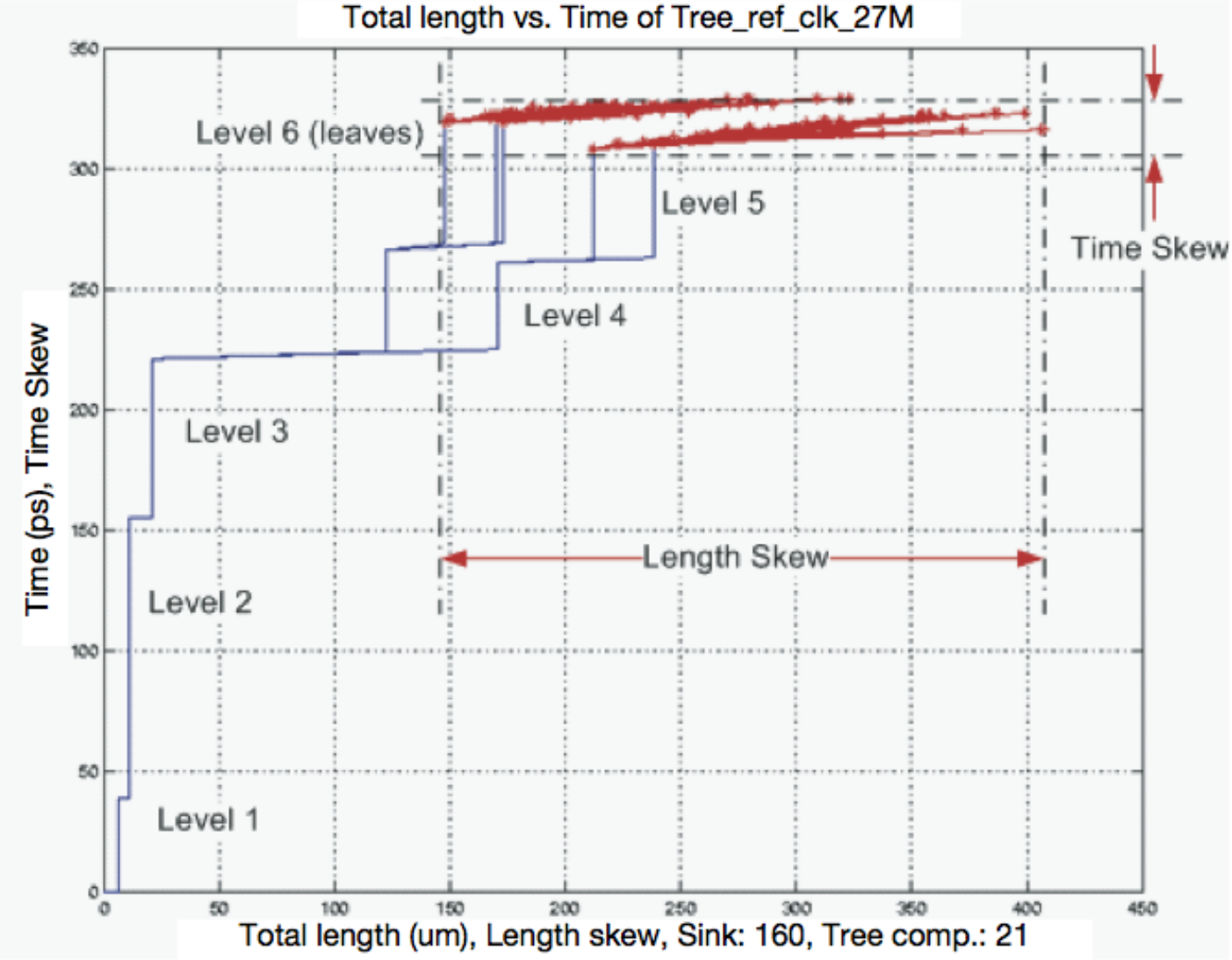
Static analysis to measure clock skew and factor it into static timing analysis

Example Skew/Jitter Analysis



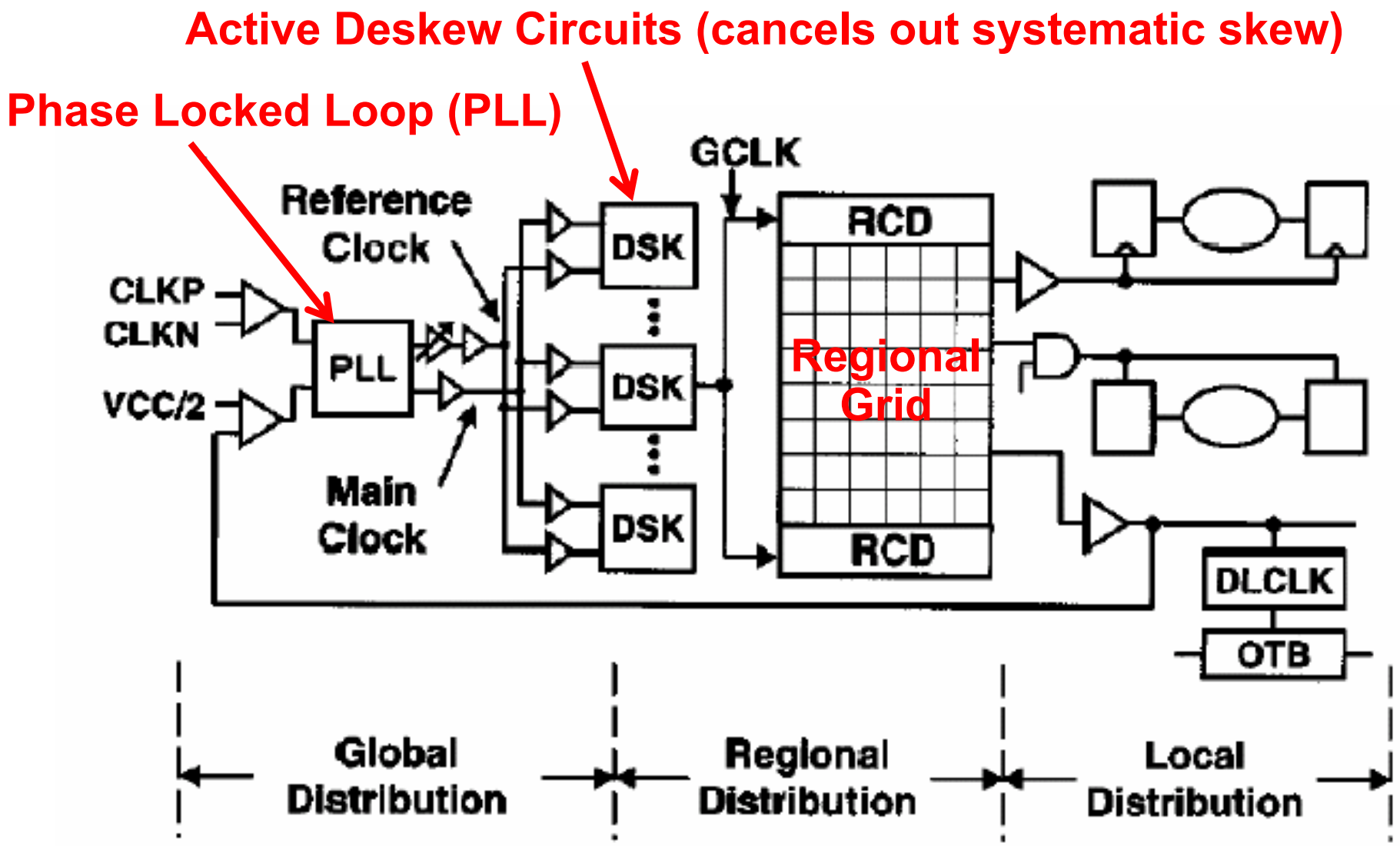
Adapted from [Xiu'08]

Example Skew/Jitter Analysis



Adapted from [Xiu'08]

Active Deskewing Circuits in Intel Itanium



Agenda

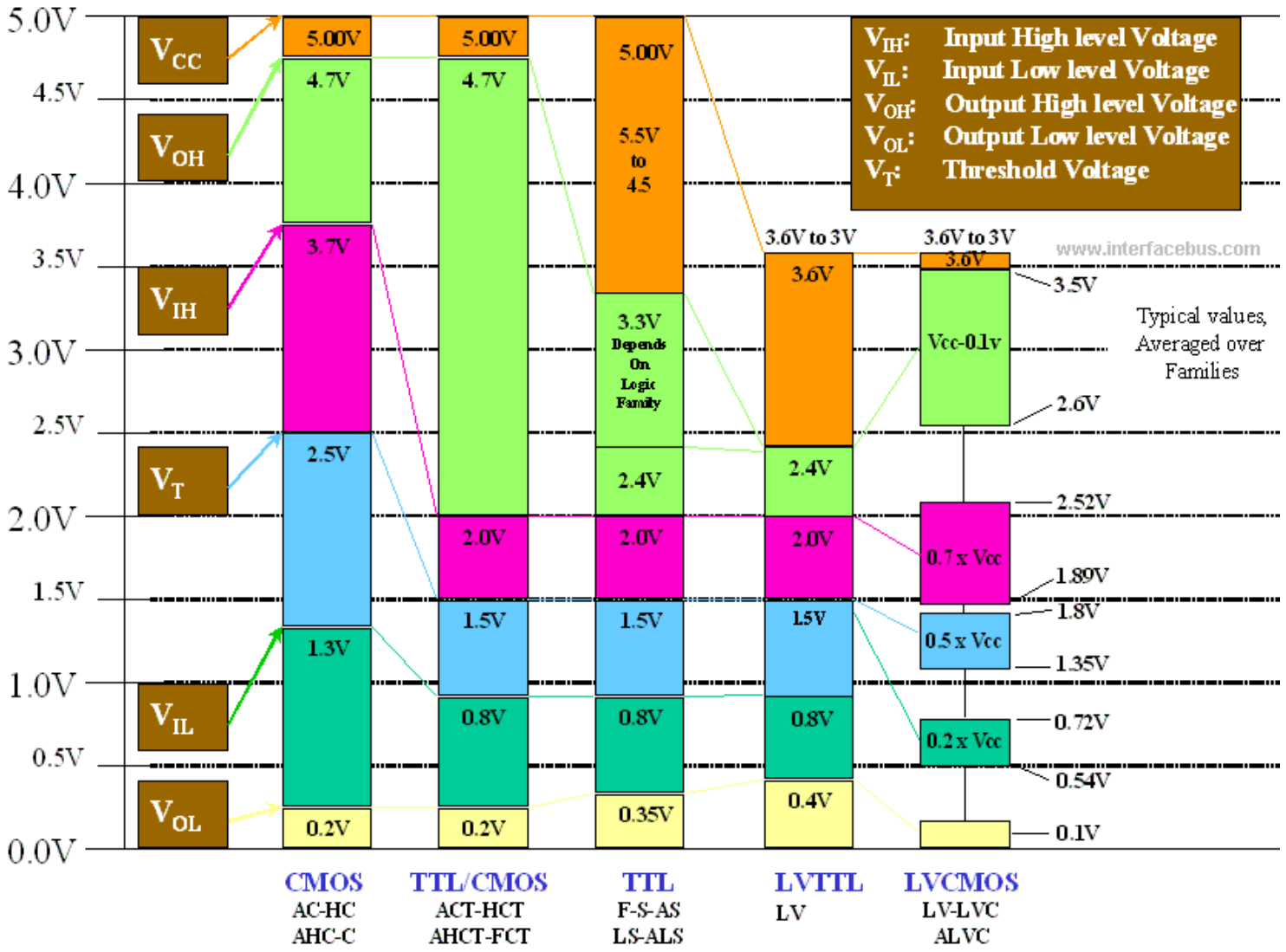
Packaging

Power Distribution

Clocking

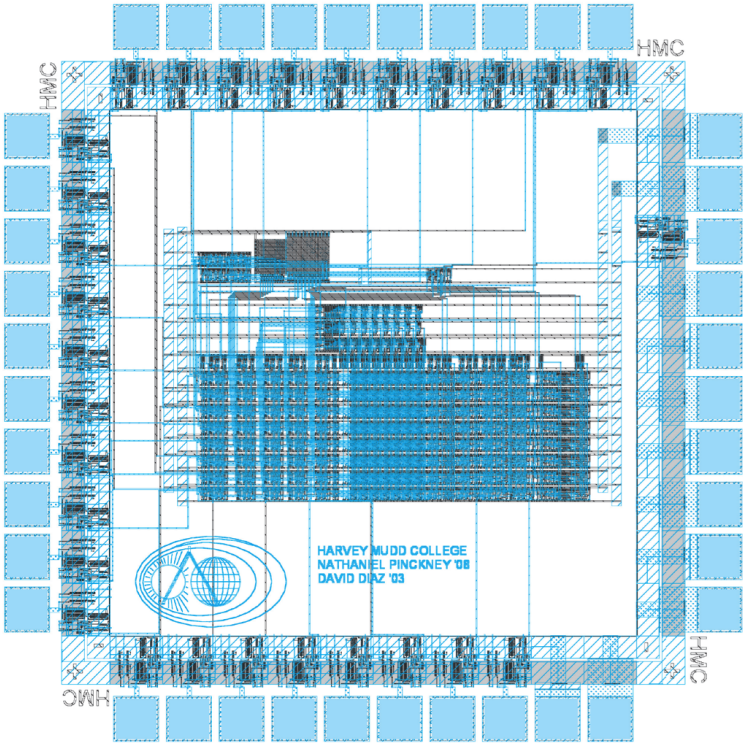
I/O

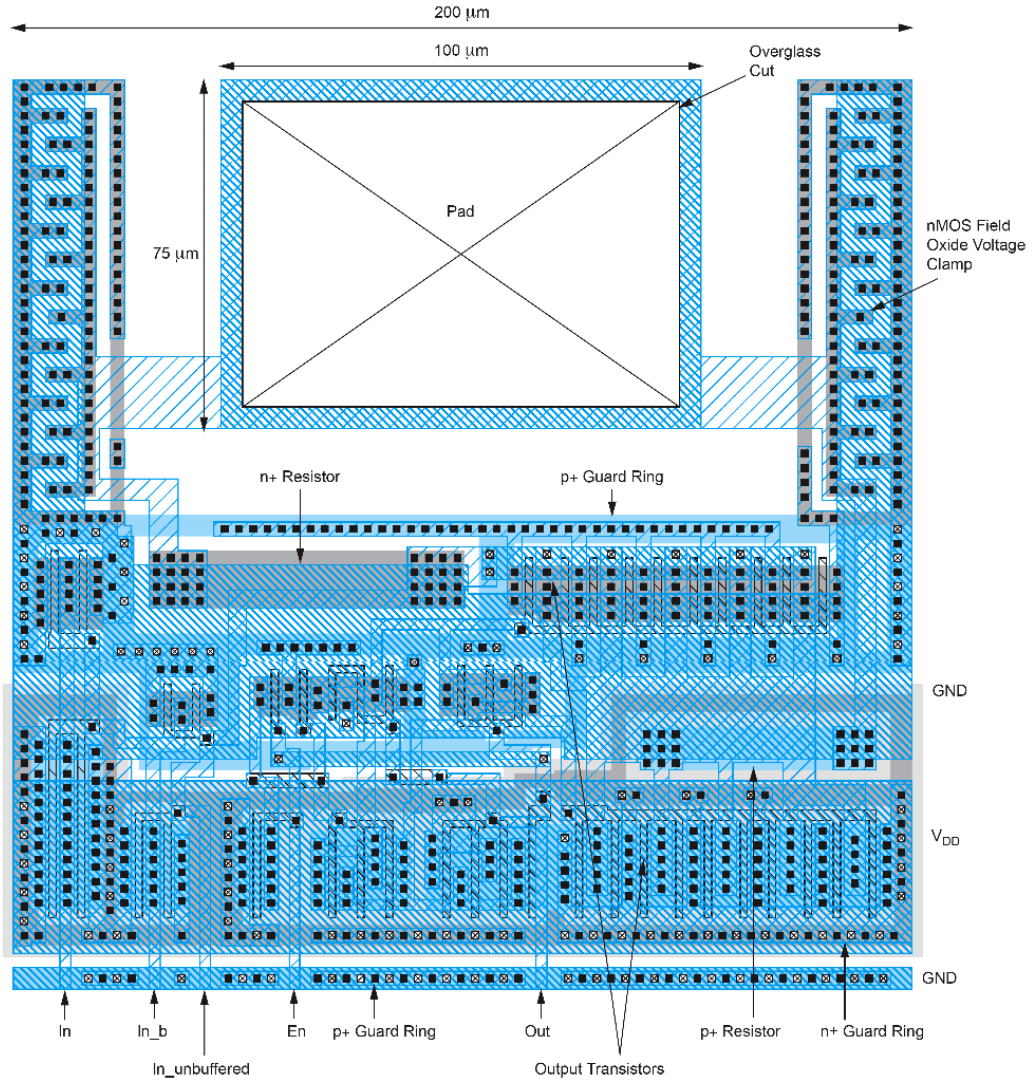
Single-Ended I/O Standards



Adapted from [www.interfacebus.com]

I/O Pads





Adapted from [Weste'11]

High-Speed Serial I/Os

- Pins are an expensive part of a system
  - Physical cost of adding pin to package
  - Size of package increases with more pins and on-pkg routing to pin
  - Bonding cost per pin
  - Size of motherboard depends on package size
  - More pins complicates board-level routing
  - Board testing time grows with number of pins
  - Reliability is function of number of solder connections
- Trend towards high-speed serial I/O
  - As computing performance grows, pins become system bottleneck
  - Want maximum bandwidth from available pins
  - Current SerDes run at 3–6 Gb/s per link at $<$200 mW

Acknowledgments

- [www.interface.com] “Chart of Low Voltage IC Switching.” http://www.interfacebus.com/Chart-of-Low-Voltage-IC-Switching.png
- [Terman’02] C. Terman and K. Asanović, MIT 6.371 Introduction to VLSI Systems, Lecture Slides, 2002.
- [Weste’11] N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective,” 4th ed, Addison Wesley, 2011.
- [Xiu’08] L. Xiu, “VLSI Circuit Design Methodologies,” Wiley-IEEE Press, 2008.