

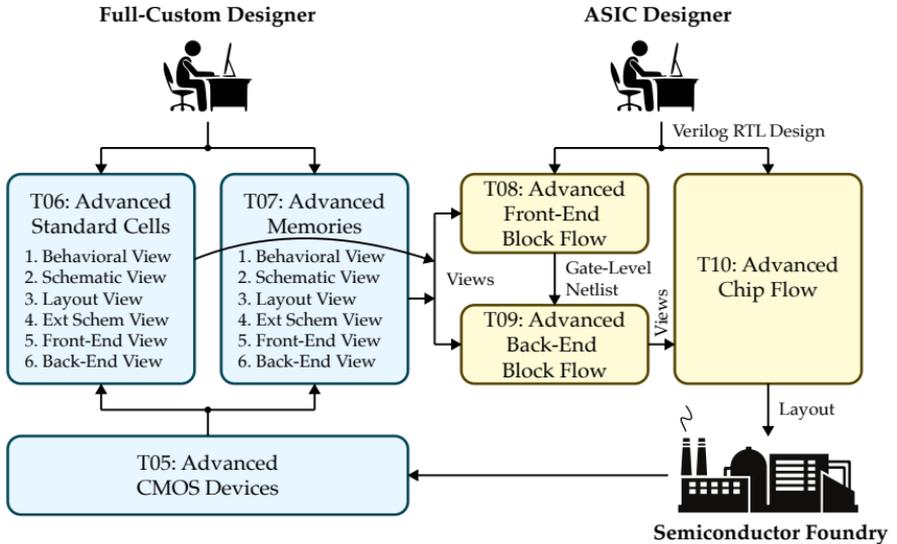
# ECE 6745 Complex Digital ASIC Design

## Topic 7: Advanced Memories

School of Electrical and Computer Engineering  
Cornell University

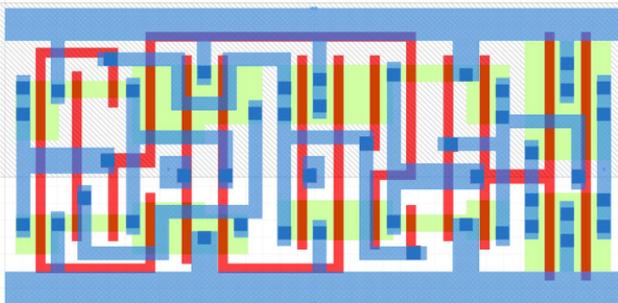
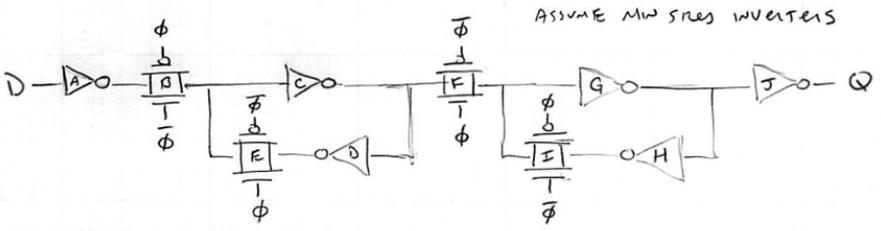
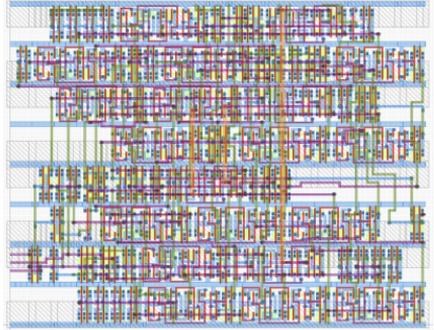
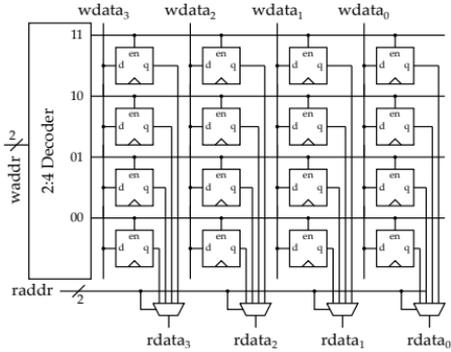
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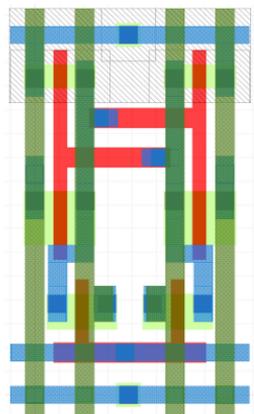
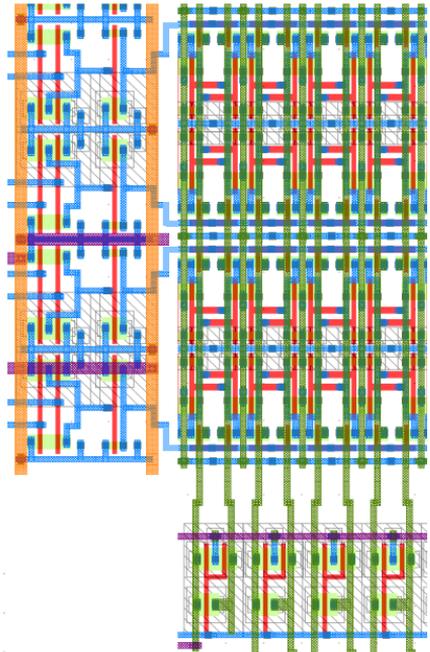
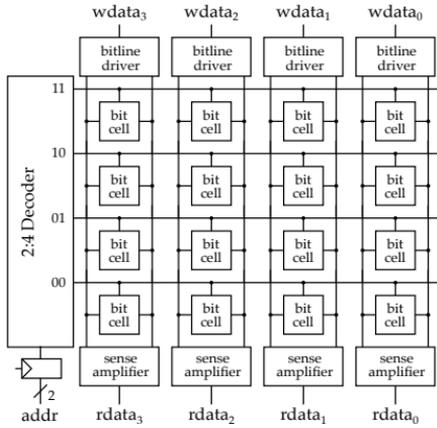


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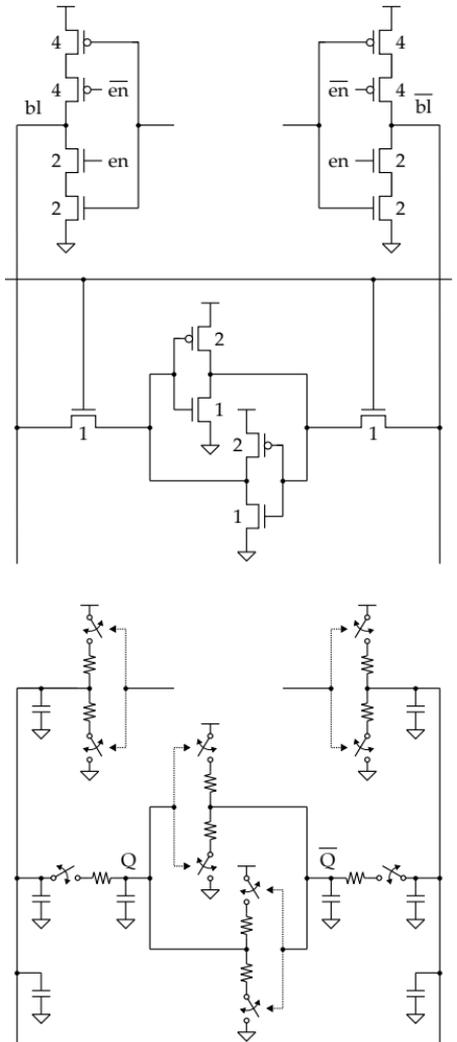
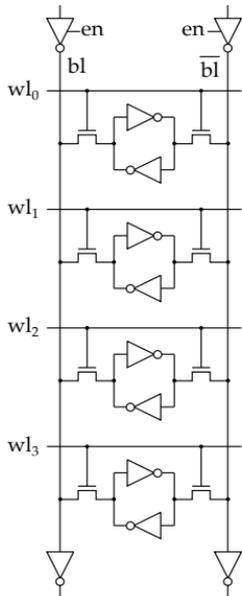
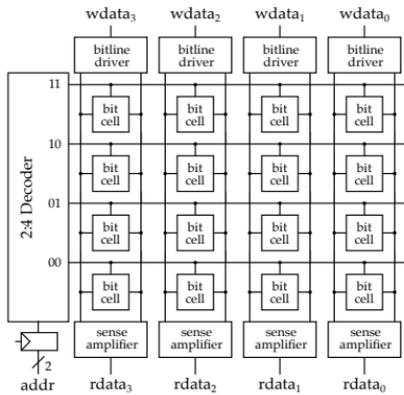
# 1. Register Files



## 2. SRAMs

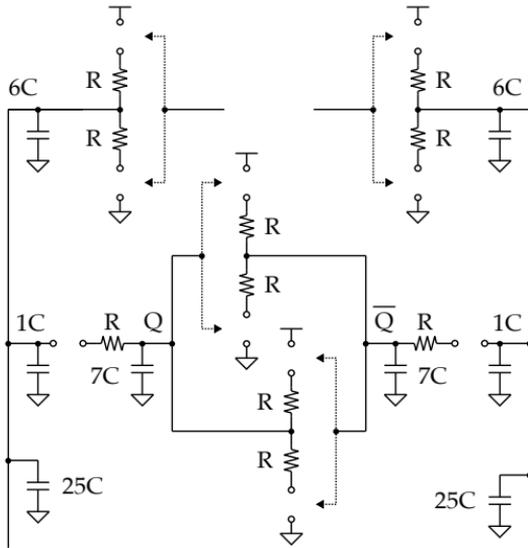


## 2. SRAMs

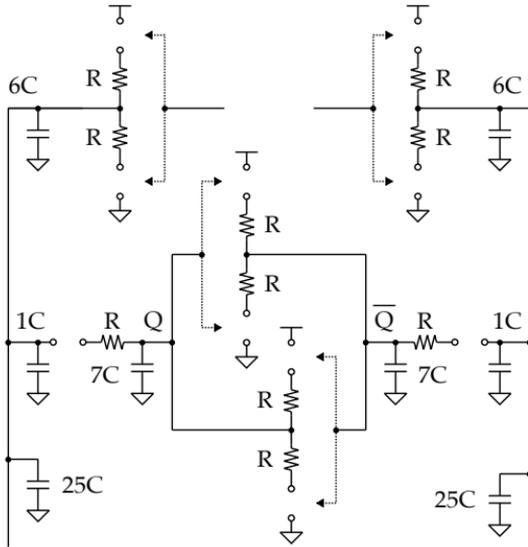


## 2.1. Read Operation

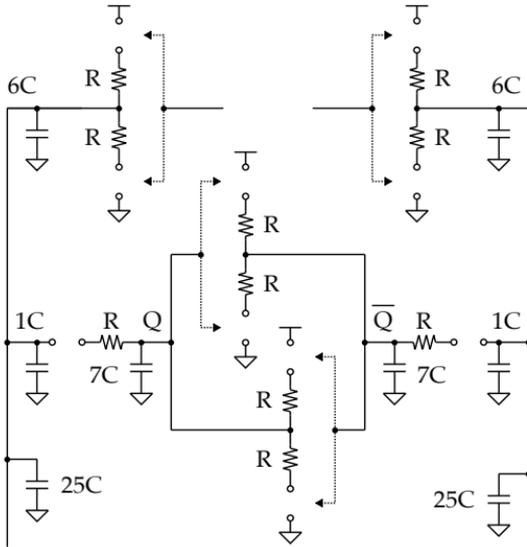
Analyzing read  $\overline{b1}$  without precharge



Analyzing read  $\overline{b1}$  with precharge

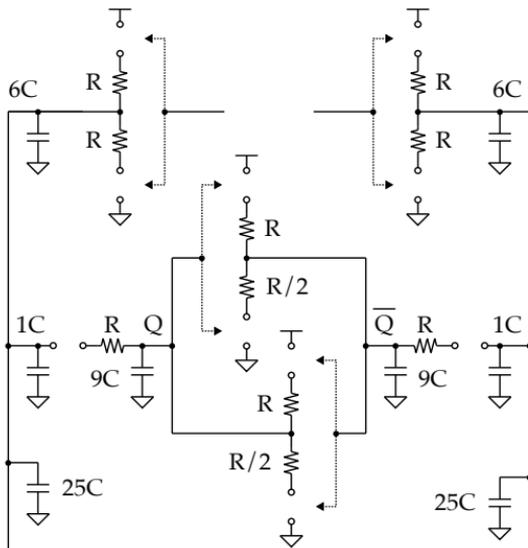


Analyzing read *bl* with precharge

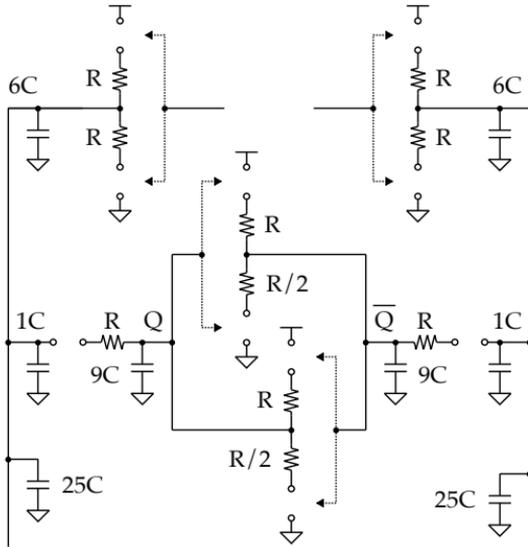


## 2.2. Write Operation

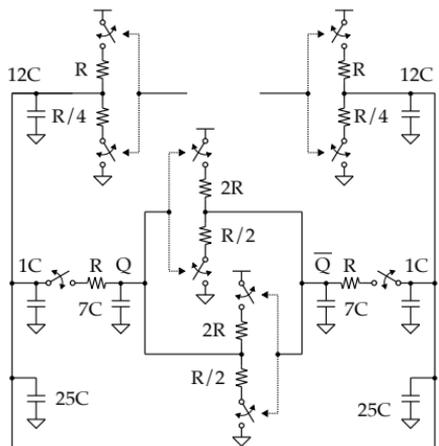
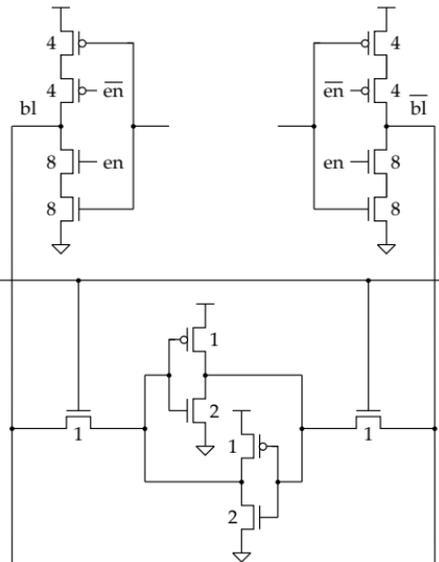
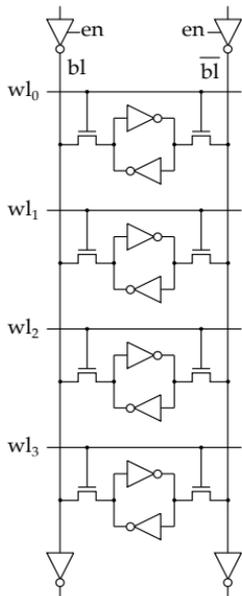
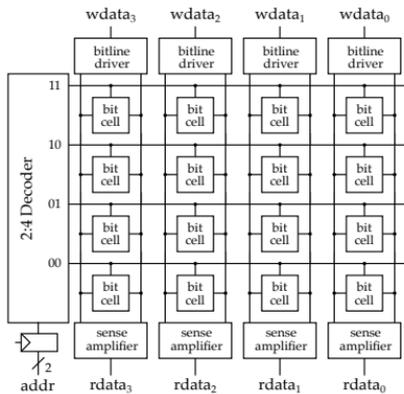
Analyzing write  $b1$



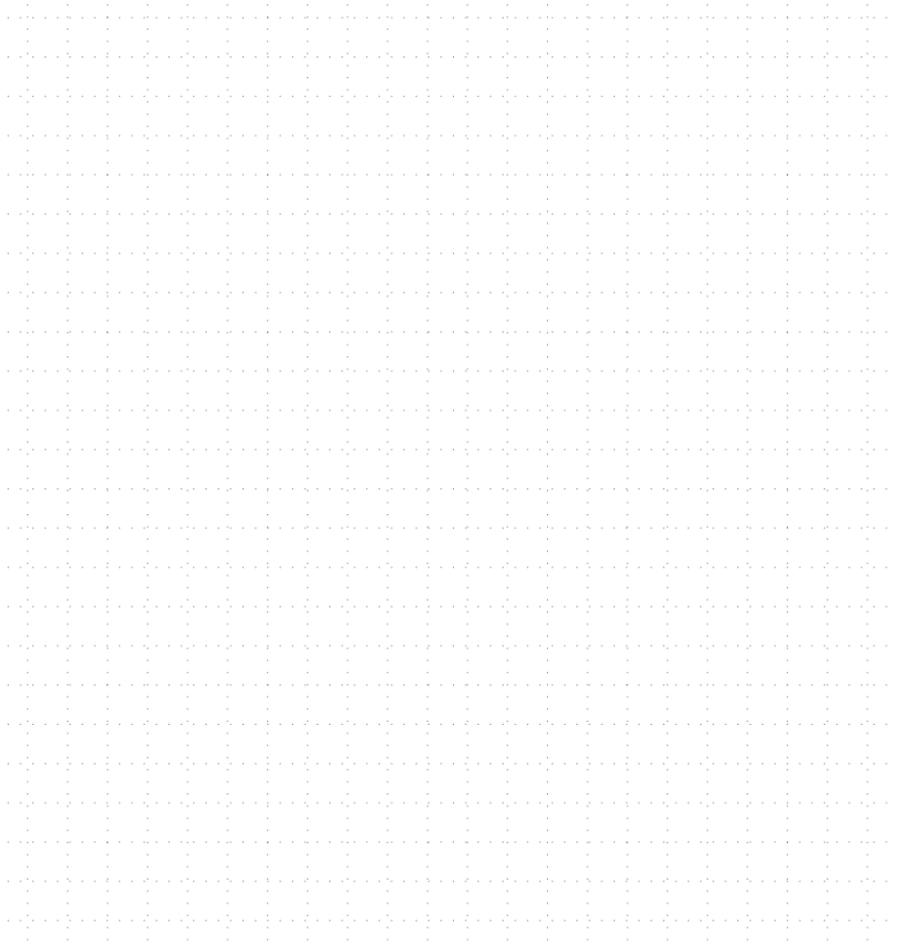
Analyzing write  $\bar{b}1$



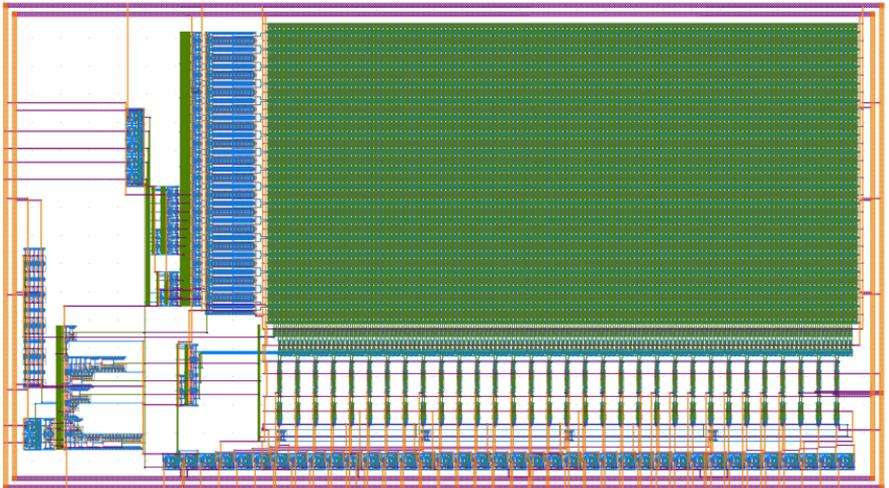
## 2.3. Delay and Energy



## 2.4. Column Muxing, Partial Writes, SubArrays, Banks



### 3. SRAM Generators



- Behavioral View
- Schematic View
- Layout View
- Extracted Schematic View
- Front-End View
- Back-End View