ECE 6745 Complex Digital ASIC Design
Topic 6: Advanced Standard Cells

School of Electrical and Computer Engineering
Cornell University

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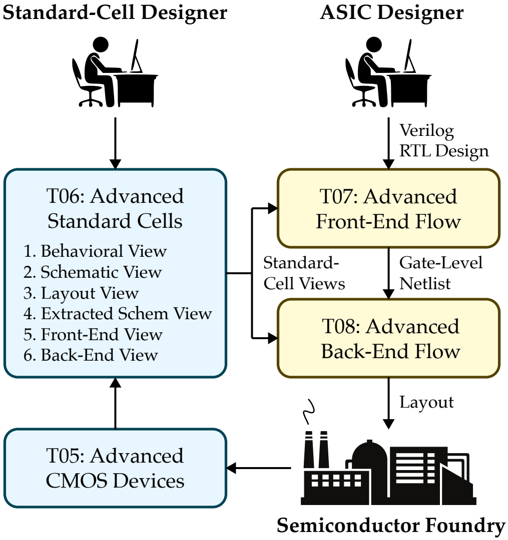
Standard-Cell Designer
ASIC Designer
Verilog RTL Design
T06: Advanced Standard Cells
1. Behavioral View
2. Schematic View
3. Layout View
4. Extracted Schem View
5. Front-End View
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T07: Advanced Front-End Flow
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Layout
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Semiconductor Foundry

1. Advanced Standard Cell Libraries

Behavioral View	Logical function of standard cell, used for gate-level sim
Schematic View	Transistor-level representation of standard cell, used for functional verification and LVS
Layout View	Layout of standard cell, used for DRC, LVS, RCX, fab
Extracted Schematic View	Transistor-level representation with extracted resistances & capacitances, used for LVS & timing characterization
Front-End View	High-level information about standard cell including area, input capacitance, logical function, and delay model; used in synthesis
Back-End View	Low-level information about standard cell including height, width, pin locs; used in placement and routing

- Advanced standard cell libraries can have additional views
  - Behavioral views in different hardware description languages
  - Formal verification views
  - Front-end views with different delay models
  - Front-end and back-end views for different tools
  - Full-custom design views
- Advanced standard cell libraries have thousands of standard cells
  - Different drive strengths
  - Combinational logic cells (simple, complex, mux, arithmetic)
  - Sequential cells (flip-flops, latches)
  - Physical cells (filler, tap, decoupling cap, antenna)
  - Cell variants (multiple channel lengths, multi-Vt, multi-Vdd)

This topic will be based on an open standard-cell library
for the FreePDK 45nm technology node

2. Combinational Standard Cells

2.1. INVX1

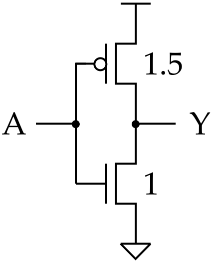
Behavioral View

A	Y
0	1
1	0

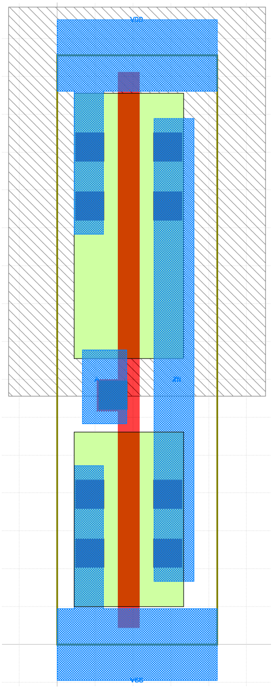
$$Y = \overline{A}$$

Might include hooks to model delay and check timing

Schematic View

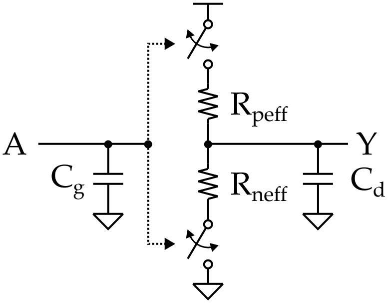


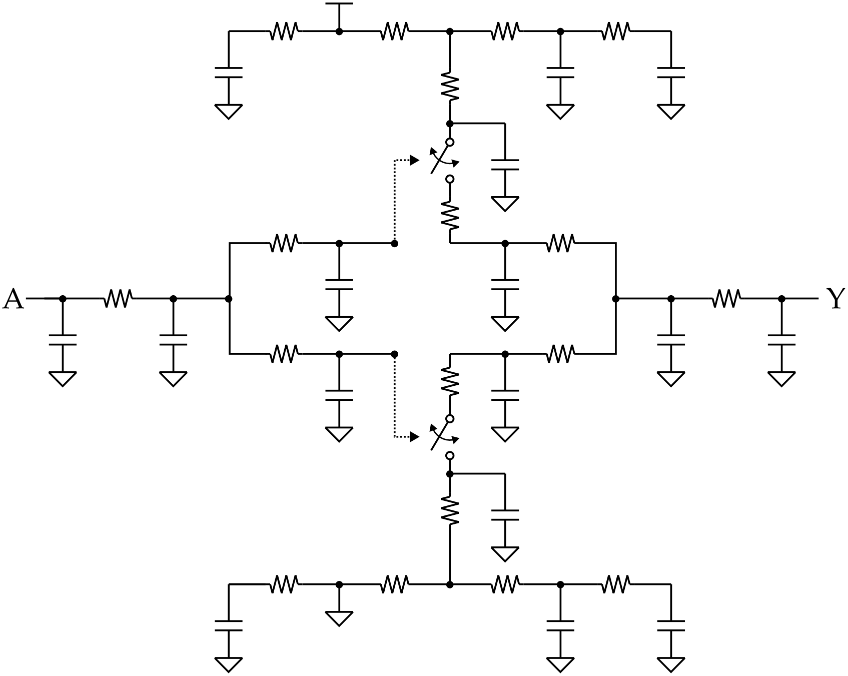
Layout View



- Micron design rules
- Diffusion sharing, transistor folding
- Transistor ordering to reduce switching capacitance
- Poly pitch alignment, dummy poly to improve lithography
- Use local interconnect (LI/M0) to reduce routing pressure
- Multiple contacts to reduce contact resistance
- Fatter pins which may or may not be on the routing grid

Extracted Schematic View





Front-End View

(numbers from open 45 nm library)

Cell Area	0.532 µm
Cell Leakage Power	14.35 nW
↪ when !A	10.10 nW
↪ when A	19.60 nW
A Input Cap	1.70 fF
↪ fall cap	1.55 fF
↪ rise cap	1.70 fF
Y Logic Function	$!A$

Non-Linear Delay Model for $t_{pd,1 \rightarrow 0}$

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.003	0.005	0.008	0.012	0.021	0.040	0.077
0.005	0.005	0.007	0.009	0.014	0.023	0.041	0.078
0.017	0.006	0.010	0.013	0.019	0.028	0.047	0.084
0.041	0.005	0.011	0.016	0.025	0.038	0.058	0.094
0.078	0.002	0.010	0.017	0.028	0.046	0.072	0.111
0.130	-0.003	0.006	0.015	0.030	0.051	0.084	0.133
0.199	-0.010	0.000	0.011	0.028	0.054	0.094	0.153

Negative delay means output reaches $V_{DD}/2$ before input reaches $V_{DD}/2$

Non-Linear Delay Model for $t_{pd,0 \rightarrow 1}$

	Load Capacitance (fF)						
Slew (ns)	0.001	0.005	0.017	0.041	0.078	0.130	0.199
0.001	0.006	0.010	0.014	0.023	0.042	0.078	0.151
0.005	0.007	0.011	0.016	0.025	0.043	0.080	0.153
0.017	0.012	0.017	0.022	0.031	0.049	0.086	0.159
0.041	0.017	0.025	0.032	0.044	0.062	0.098	0.171
0.078	0.023	0.033	0.042	0.058	0.081	0.118	0.190
0.130	0.031	0.042	0.054	0.072	0.102	0.146	0.218
0.199	0.041	0.054	0.066	0.088	0.122	0.176	0.256

Non-Linear Delay Model for t_{fall}

	Load Capacitance (fF)						
Slew (ns)	0.001	0.005	0.017	0.041	0.078	0.130	0.199
0.001	0.001	0.003	0.005	0.009	0.017	0.033	0.065
0.005	0.002	0.003	0.005	0.009	0.017	0.033	0.065
0.017	0.005	0.006	0.008	0.010	0.017	0.033	0.065
0.041	0.008	0.011	0.013	0.017	0.022	0.034	0.065
0.078	0.013	0.016	0.019	0.024	0.031	0.043	0.067
0.130	0.020	0.024	0.027	0.033	0.042	0.056	0.078
0.199	0.029	0.033	0.037	0.044	0.054	0.071	0.097

Non-Linear Delay Model for t_{rise}

	Load Capacitance (fF)						
Slew (ns)	0.001	0.005	0.017	0.041	0.078	0.130	0.199
0.001	0.003	0.007	0.011	0.020	0.037	0.072	0.141
0.005	0.003	0.007	0.011	0.020	0.037	0.072	0.141
0.017	0.006	0.009	0.012	0.020	0.037	0.072	0.141
0.041	0.010	0.014	0.018	0.024	0.038	0.072	0.141
0.078	0.015	0.020	0.025	0.033	0.045	0.073	0.141
0.130	0.021	0.027	0.032	0.042	0.058	0.082	0.141
0.199	0.029	0.035	0.041	0.053	0.072	0.100	0.149

Process, Voltage, Temperature Corners

Corner	Process	Voltage (V)	Temp (°C)
Typical-Typical	typical	1.10	25
Slow-Slow	slow	0.95	125
Fast-Fast	fast	1.25	0

Slow-Slow Non-Linear Delay Model for $t_{pd,1 \rightarrow 0}$

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.002	0.007	0.010	0.015	0.024	0.041	0.077	0.147
0.011	0.012	0.016	0.020	0.029	0.047	0.082	0.152
0.043	0.020	0.029	0.036	0.048	0.066	0.101	0.171
0.103	0.024	0.039	0.053	0.072	0.099	0.138	0.208
0.196	0.023	0.046	0.066	0.095	0.134	0.189	0.265
0.327	0.015	0.046	0.073	0.113	0.167	0.240	0.340
0.500	0.000	0.039	0.073	0.125	0.196	0.291	0.418

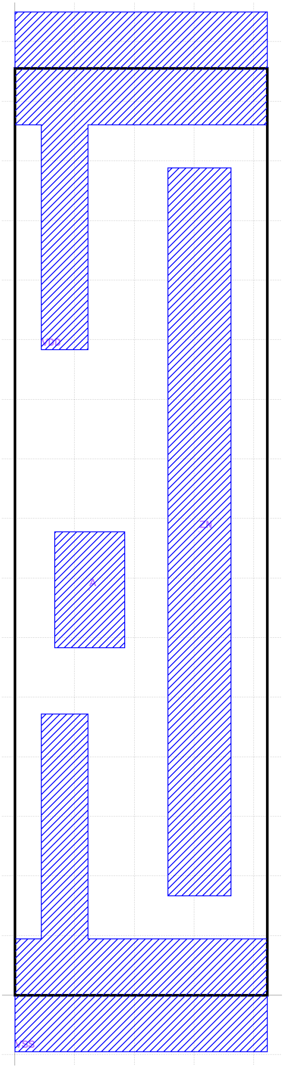
Fast-Fast Non-Linear Delay Model for $t_{pd,1 \rightarrow 0}$

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.003	0.004	0.006	0.010	0.017	0.032	0.062
0.004	0.003	0.005	0.007	0.011	0.018	0.033	0.063
0.013	0.003	0.006	0.009	0.013	0.021	0.036	0.065
0.030	0.002	0.006	0.010	0.016	0.026	0.042	0.071
0.058	-0.001	0.004	0.009	0.017	0.029	0.049	0.080
0.096	-0.005	0.001	0.006	0.016	0.031	0.055	0.092
0.146	-0.011	-0.005	0.002	0.013	0.030	0.058	0.102

Back-End View

- Pins can be polygons and do not necessarily need to be on grid
- Blockages enable standard cell and routing to use same metal layers

Cell Height	1.40 µm
Cell Width	0.38 µm
A Pin Location	(0.06,0.525) (0.165,0.525) (0.165,0.7) (0.06,0.7)
Y Pin Location	(0.23,0.15) (0.325,0.15) (0.325,1.25) (0.23,1.25)



2.2. NAND2X1

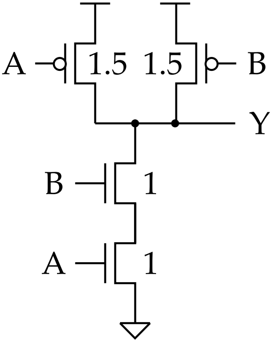
Behavioral View

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

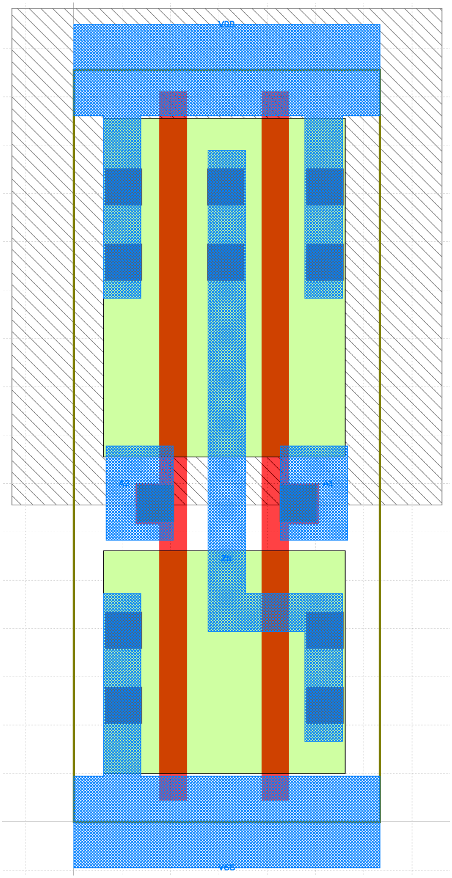
$$Y = \overline{AB}$$

Might include hooks to model delay and check timing

Schematic View

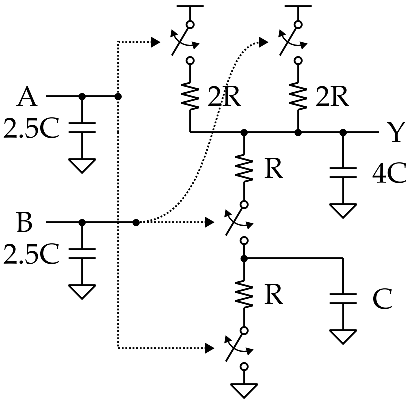


Layout View



Extracted Schematic View

(estimated $R_{p,\mathit{eff}} = 3 \times R_{n,\mathit{eff}}$)



List all possible input conditions

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

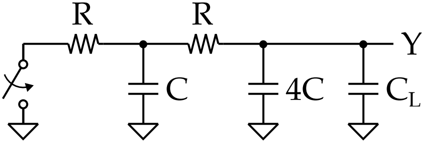
A	B	Y
0	$0 \to 1$	
0	$1 \to 0$	
1	$0 \to 1$	
1	$1 \to 0$	
$0 \to 1$	0	
$1 \to 0$	0	
$0 \to 1$	1	
$1 \to 0$	1	

- Estimate propagation delay for all input conditions which result in an output transition

$t_{pd,1 \to 0}$

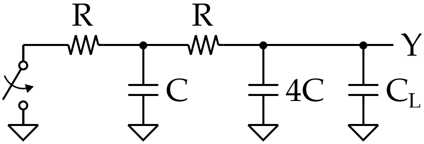
A $= 0 \to 1$

B $= 1$



Use Elmore's delay to estimate propagation delay of NAND2X1

$t_{pd,1\rightarrow 0}$
A $= 0 \rightarrow 1$
B $= 1$



$$\begin{aligned} t_{pd,1\rightarrow 0} &= RC + 2R(4C + C_L) \\ &= RC + 8RC + 2RC_L = 9RC + 2RC_L \end{aligned}$$

$t_{pd,1\rightarrow 0}$
A $= 1$
B $= 0 \rightarrow 1$

$t_{pd,0\rightarrow 1}$
A $= 1$
B $= 1 \rightarrow 0$

$t_{pd,0\rightarrow 1}$
A $= 1 \rightarrow 0$
B $= 1$

- Value-, Path-, and Load-Dependent Linear Delay Model

A	B	Y
1	$0 \rightarrow 1$	$t_{pd,1\rightarrow 0} = 8RC + 2RC_L$
1	$1 \rightarrow 0$	$t_{pd,0\rightarrow 1} = 8RC + 2RC_L$
$0 \rightarrow 1$	1	$t_{pd,1\rightarrow 0} = 9RC + 2RC_L$
$1 \rightarrow 0$	1	$t_{pd,0\rightarrow 1} = 10RC + 2RC_L$

- Path- and Load-Dependent Linear Delay Model

$$t_{pd,B\rightarrow Y} = 8RC + 2RC_L$$
$$t_{pd,A\rightarrow Y} = 10RC + 2RC_L$$

- Load-Dependent Linear Delay Model

$$t_{pd} = 10RC + 2RC_L$$

- Constant Delay Model

$$t_{pd} = 10RC + 2R(3C) = 16RC$$

- More Advanced Delay Models
  - Slew-, value-, path, and load-dependent non-linear delay model
  - Current source delay models

Front-End View

(numbers from open 45 nm library)

Cell Area	0.798 µm
Cell Leakage Power	17.39 nW
↪ when !A & !B	3.48 nW
↪ when !A & B	24.80 nW
↪ when A & !B	4.09 nW
↪ when A & B	37.21 nW

A Input Cap	1.60 fF
↪ fall cap	1.53 fF
↪ rise cap	1.60 fF
B Input Cap	1.66 fF
↪ fall cap	1.50 fF
↪ rise cap	1.66 fF
Y Logic Function	$!(A\&B)$

Non-Linear Delay Model for $t_{pd,1 \rightarrow 0}$ related to A

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.007	0.010	0.014	0.022	0.037	0.068	0.130
0.017	0.011	0.016	0.020	0.028	0.043	0.074	0.136
0.078	0.013	0.021	0.029	0.043	0.066	0.100	0.161
0.199	0.008	0.019	0.031	0.051	0.083	0.134	0.211

Non-Linear Delay Model for $t_{pd,1 \rightarrow 0}$ related to B

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.008	0.011	0.015	0.023	0.038	0.069	0.131
0.017	0.012	0.016	0.020	0.028	0.044	0.075	0.136
0.078	0.014	0.022	0.029	0.041	0.061	0.094	0.156
0.199	0.009	0.020	0.031	0.050	0.079	0.123	0.194

Non-linear delay models for every path, every value, every corner

Back-End View

Cell Height	1.40 µm
Cell Width	0.38 µm
A Pin Location	(0.385,0.525) (0.51,0.525) (0.51,0.7) (0.385,0.7)
B Pin Location	(0.06,0.525) (0.185,0.525) (0.185,0.7) (0.06,0.7)
Y Pin Location	(0.25,0.355) (0.43,0.355) (0.43,0.15) (0.5,0.15) (0.5,0.425) (0.32,0.425) (0.32,1.25) (0.25,1.25)