ECE 6745 Complex Digital ASIC Design
Topic 6: Advanced Standard Cells

School of Electrical and Computer Engineering
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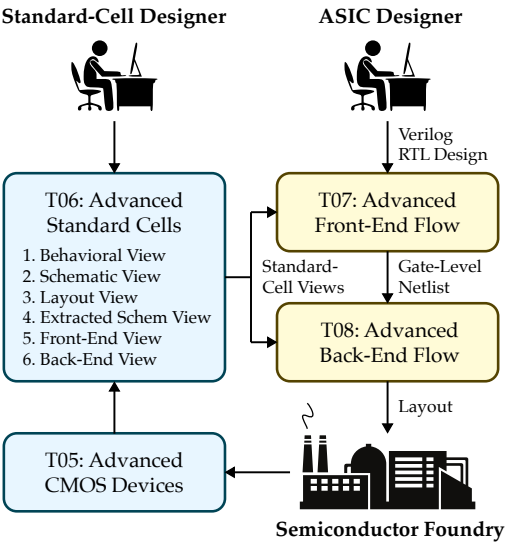


1. Advanced Standard Cell Libraries

Behavioral View	Logical function of standard cell, used for gate-level sim
Schematic View	Transistor-level representation of standard cell, used for functional verification and LVS
Layout View	Layout of standard cell, used for DRC, LVS, RCX, fab
Extracted Schematic View	Transistor-level representation with extracted resistances & capacitances, used for LVS & timing characterization
Front-End View	High-level information about standard cell including area, input capacitance, logical function, and delay model; used in synthesis
Back-End View	Low-level information about standard cell including height, width, pin locs; used in placement and routing

- Advanced standard cell libraries can have additional views
  - Behavioral views in different hardware description languages
  - Formal verification views
  - Front-end views with different delay models
  - Front-end and back-end views for different tools
  - Full-custom design views
- Advanced standard cell libraries have thousands of standard cells
  - Different drive strengths
  - Combinational logic cells (simple, complex, mux, arithmetic)
  - Sequential cells (flip-flops, latches)
  - Physical cells (filler, tap, decoupling cap, antenna)
  - Cell variants (multiple channel lengths, multi-Vt, multi-Vdd)

This topic will be based on an open standard-cell library
for the FreePDK 45nm technology node

2. Combinational Standard Cells

2.1. INVX1

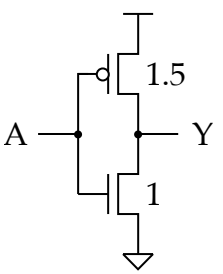
Behavioral View

A	Y
0	1
1	0

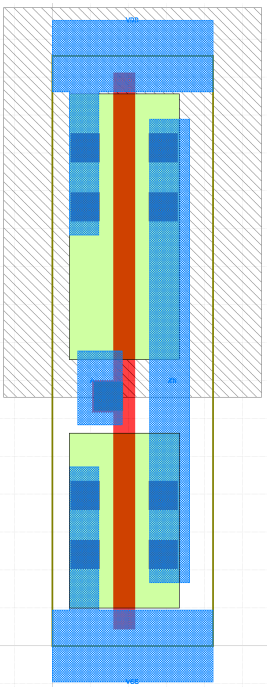
$Y = \overline{A}$

Might include hooks to model delay and check timing

Schematic View

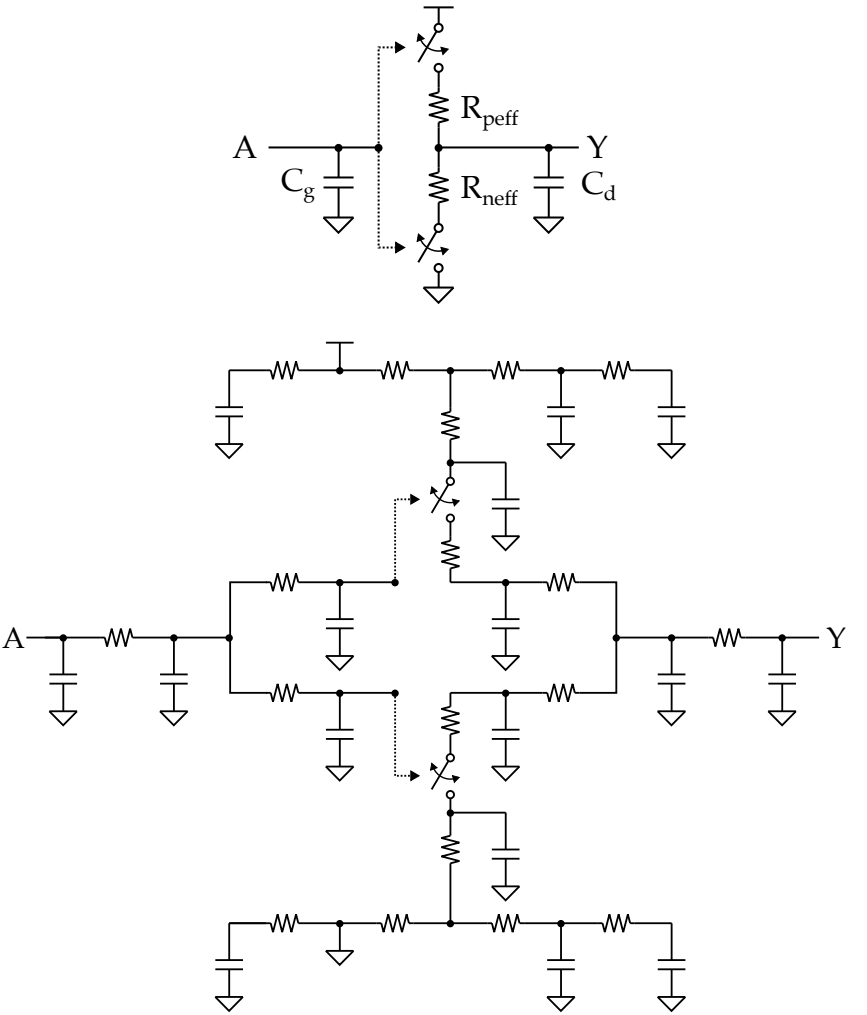


Layout View



- Micron design rules
- Diffusion sharing, transistor folding
- Transistor ordering to reduce switching capacitance
- Poly pitch alignment, dummy poly to improve lithography
- Use local interconnect (LI/M0) to reduce routing pressure
- Multiple contacts to reduce contact resistance
- Fatter pins which may or may not be on the routing grid

Extracted Schematic View



Front-End View *(numbers from open 45 nm library)*

Cell Area	0.532 µm
Cell Leakage Power	14.35 nW
↪ when !A	10.10 nW
↪ when A	19.60 nW
A Input Cap	1.70 fF
↪ fall cap	1.55 fF
↪ rise cap	1.70 fF
Y Logic Function	$!A$

Non-Linear Delay Model for $t_{pd,1 \to 0}$ (ns)

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.003	0.005	0.008	0.012	0.021	0.040	0.077
0.005	0.005	0.007	0.009	0.014	0.023	0.041	0.078
0.017	0.006	0.010	0.013	0.019	0.028	0.047	0.084
0.041	0.005	0.011	0.016	0.025	0.038	0.058	0.094
0.078	0.002	0.010	0.017	0.028	0.046	0.072	0.111
0.130	-0.003	0.006	0.015	0.030	0.051	0.084	0.133
0.199	-0.010	0.000	0.011	0.028	0.054	0.094	0.153

Negative delay means output reaches $V_{DD}/2$ before input reaches $V_{DD}/2$

Non-Linear Delay Model for $t_{pd,0 \to 1}$ (ns)

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.006	0.010	0.014	0.023	0.042	0.078	0.151
0.005	0.007	0.011	0.016	0.025	0.043	0.080	0.153
0.017	0.012	0.017	0.022	0.031	0.049	0.086	0.159
0.041	0.017	0.025	0.032	0.044	0.062	0.098	0.171
0.078	0.023	0.033	0.042	0.058	0.081	0.118	0.190
0.130	0.031	0.042	0.054	0.072	0.102	0.146	0.218
0.199	0.041	0.054	0.066	0.088	0.122	0.176	0.256

Non-Linear Delay Model for t_{fall} (ns)

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.001	0.003	0.005	0.009	0.017	0.033	0.065
0.005	0.002	0.003	0.005	0.009	0.017	0.033	0.065
0.017	0.005	0.006	0.008	0.010	0.017	0.033	0.065
0.041	0.008	0.011	0.013	0.017	0.022	0.034	0.065
0.078	0.013	0.016	0.019	0.024	0.031	0.043	0.067
0.130	0.020	0.024	0.027	0.033	0.042	0.056	0.078
0.199	0.029	0.033	0.037	0.044	0.054	0.071	0.097

Non-Linear Delay Model for t_{rise}

	Load Capacitance (fF) (ns)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.003	0.007	0.011	0.020	0.037	0.072	0.141
0.005	0.003	0.007	0.011	0.020	0.037	0.072	0.141
0.017	0.006	0.009	0.012	0.020	0.037	0.072	0.141
0.041	0.010	0.014	0.018	0.024	0.038	0.072	0.141
0.078	0.015	0.020	0.025	0.033	0.045	0.073	0.141
0.130	0.021	0.027	0.032	0.042	0.058	0.082	0.141
0.199	0.029	0.035	0.041	0.053	0.072	0.100	0.149

Corners are specific combinations of processor, voltage, and temperature conditions

PMOS	PMOS	Voltage (V)	Temp (°C)
typical	typical	1.10	25
slow	slow	0.95	125
fast	fast	1.25	0
slow	fast	1.25	0
fast	slow	1.25	0

Non-Linear Delay Model for $t_{pd,1 \to 0}$ at Slow-Slow 0.95 V 125 °C Corner

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.002	0.007	0.010	0.015	0.024	0.041	0.077	0.147
0.011	0.012	0.016	0.020	0.029	0.047	0.082	0.152
0.043	0.020	0.029	0.036	0.048	0.066	0.101	0.171
0.103	0.024	0.039	0.053	0.072	0.099	0.138	0.208
0.196	0.023	0.046	0.066	0.095	0.134	0.189	0.265
0.327	0.015	0.046	0.073	0.113	0.167	0.240	0.340
0.500	0.000	0.039	0.073	0.125	0.196	0.291	0.418

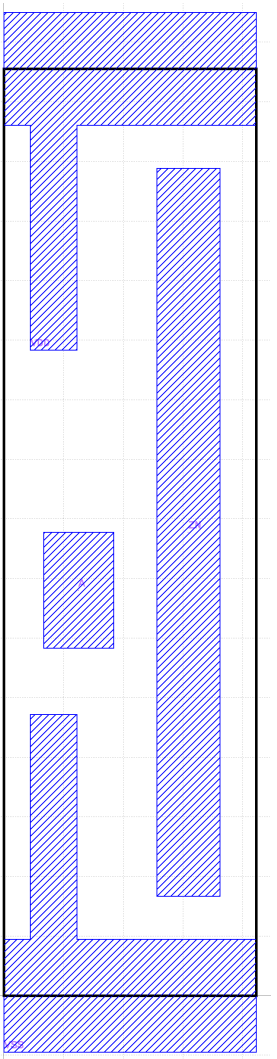
Non-Linear Delay Model for $t_{pd,1 \to 0}$ at Fast-Fast 1.25 V 0 °C Corner

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.003	0.004	0.006	0.010	0.017	0.032	0.062
0.004	0.003	0.005	0.007	0.011	0.018	0.033	0.063
0.013	0.003	0.006	0.009	0.013	0.021	0.036	0.065
0.030	0.002	0.006	0.010	0.016	0.026	0.042	0.071
0.058	-0.001	0.004	0.009	0.017	0.029	0.049	0.080
0.096	-0.005	0.001	0.006	0.016	0.031	0.055	0.092
0.146	-0.011	-0.005	0.002	0.013	0.030	0.058	0.102

Back-End View

- Pins can be polygons and do not necessarily need to be on grid
- Blockages enable standard cell and routing to use same metal layers

Cell Height	1.40 µm
Cell Width	0.38 µm
A Pin Location	(0.06,0.525) (0.165,0.525) (0.165,0.7) (0.06,0.7)
Y Pin Location	(0.23,0.15) (0.325,0.15) (0.325,1.25) (0.23,1.25)



2.2. NAND2X1

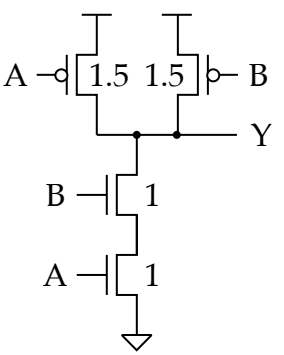
Behavioral View

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

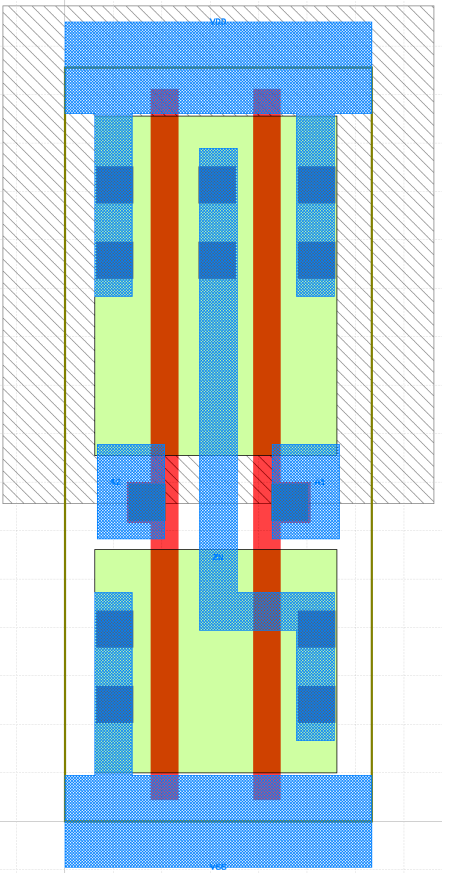
$Y = \overline{AB}$

Might include hooks to model delay and check timing

Schematic View

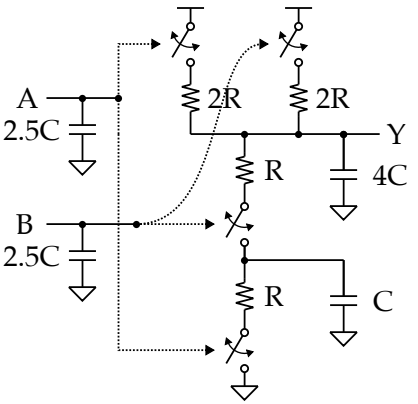


Layout View



Extracted Schematic View

(estimated $R_{p,eff} = 3 \times R_{n,eff}$)



List all possible input conditions

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

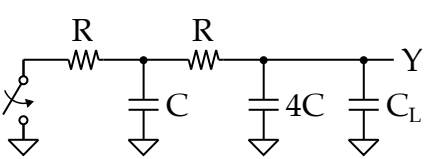
A	B	Y
0	$0 \rightarrow 1$	
0	$1 \rightarrow 0$	
1	$0 \rightarrow 1$	
1	$1 \rightarrow 0$	
$0 \rightarrow 1$	0	
$1 \rightarrow 0$	0	
$0 \rightarrow 1$	1	
$1 \rightarrow 0$	1	

- Estimate propagation delay for all input conditions which result in an output transition

$t_{pd,1 \rightarrow 0}$

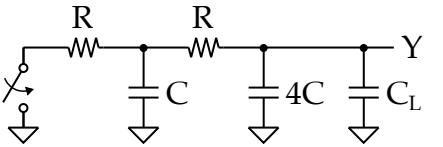
A $= 0 \rightarrow 1$

B $= 1$



Use Elmore's delay to estimate propagation delay of NAND2X1

$t_{pd,1\to 0}$
A $= 0 \to 1$
B $= 1$



$$t_{pd,1\to 0} = RC + 2R(4C + C_L)$$
$$= RC + 8RC + 2RC_L = 9RC + 2RC_L$$

$t_{pd,1\to 0}$
A $= 1$
B $= 0 \to 1$

$t_{pd,0\to 1}$
A $= 1$
B $= 1 \to 0$

$t_{pd,0\to 1}$
A $= 1 \to 0$
B $= 1$

- Value-, Path-, and Load-Dependent Linear Delay Model

A	B	Y
1	$0 \rightarrow 1$	$t_{pd,1\rightarrow 0} = 8RC + 2RC_L$
1	$1 \rightarrow 0$	$t_{pd,0\rightarrow 1} = 8RC + 2RC_L$
$0 \rightarrow 1$	1	$t_{pd,1\rightarrow 0} = 9RC + 2RC_L$
$1 \rightarrow 0$	1	$t_{pd,0\rightarrow 1} = 10RC + 2RC_L$

- Path- and Load-Dependent Linear Delay Model

$$t_{pd,B\rightarrow Y} = 8RC + 2RC_L$$
$$t_{pd,A\rightarrow Y} = 10RC + 2RC_L$$

- Load-Dependent Linear Delay Model

$$t_{pd} = 10RC + 2RC_L$$

- Constant Delay Model

$$t_{pd} = 10RC + 2R(3C) = 16RC$$

- More Advanced Delay Models
  - Slew-, value-, path, and load-dependent non-linear delay model
  - Current source delay models

Front-End View *(numbers from open 45 nm library)*

Cell Area	0.798 µm
Cell Leakage Power	17.39 nW
↪ when !A & !B	3.48 nW
↪ when !A & B	24.80 nW
↪ when A & !B	4.09 nW
↪ when A & B	37.21 nW

A Input Cap	1.60 fF
↪ fall cap	1.53 fF
↪ rise cap	1.60 fF
B Input Cap	1.66 fF
↪ fall cap	1.50 fF
↪ rise cap	1.66 fF
Y Logic Function	$!(A\&B)$

Non-Linear Delay Model for $t_{pd,1\to 0}$ related to A

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.007	0.010	0.014	0.022	0.037	0.068	0.130
0.017	0.011	0.016	0.020	0.028	0.043	0.074	0.136
0.078	0.013	0.021	0.029	0.043	0.066	0.100	0.161
0.199	0.008	0.019	0.031	0.051	0.083	0.134	0.211

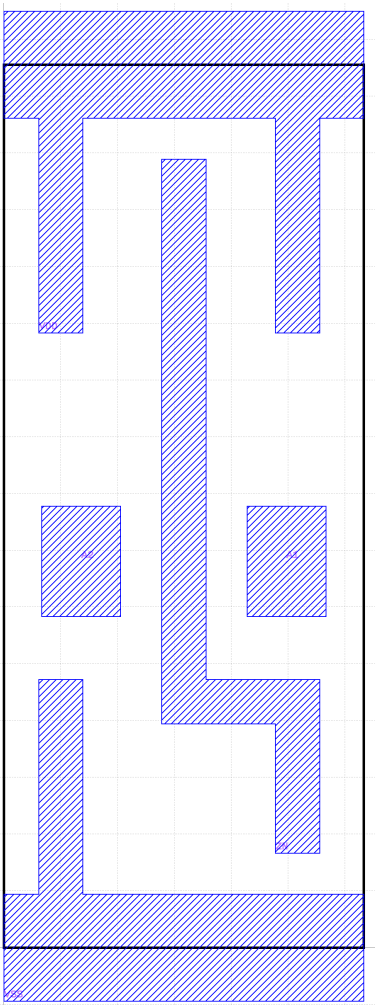
Non-Linear Delay Model for $t_{pd,1\to 0}$ related to B

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.008	0.011	0.015	0.023	0.038	0.069	0.131
0.017	0.012	0.016	0.020	0.028	0.044	0.075	0.136
0.078	0.014	0.022	0.029	0.041	0.061	0.094	0.156
0.199	0.009	0.020	0.031	0.050	0.079	0.123	0.194

Non-linear delay models for every path, every value, every corner

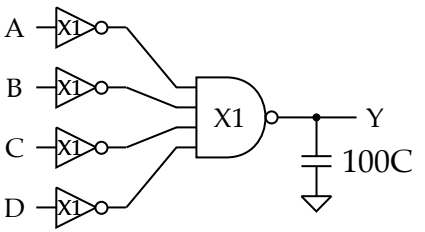
Back-End View

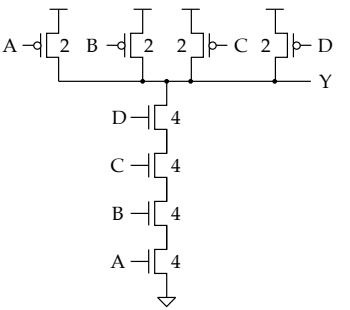
Cell Height	1.40 µm
Cell Width	0.38 µm
A Pin Location	(0.385,0.525) (0.51,0.525) (0.51,0.7) (0.385,0.7)
B Pin Location	(0.06,0.525) (0.185,0.525) (0.185,0.7) (0.06,0.7)
Y Pin Location	(0.25,0.355) (0.43,0.355) (0.43,0.15) (0.5,0.15) (0.5,0.425) (0.32,0.425) (0.32,1.25) (0.25,1.25)



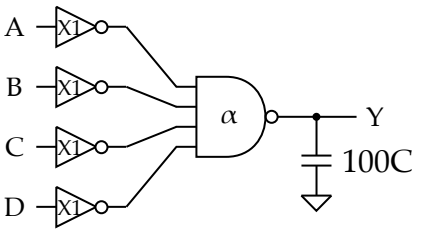
2.3. Cell Drive Strengths

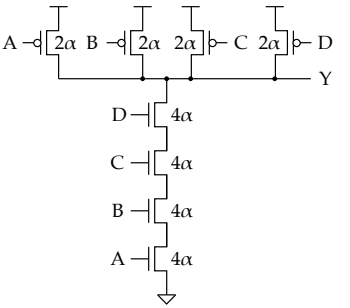
- Consider the following 2-stage implementation of a four-input OR gate driving a large load (i.e., large fanout)

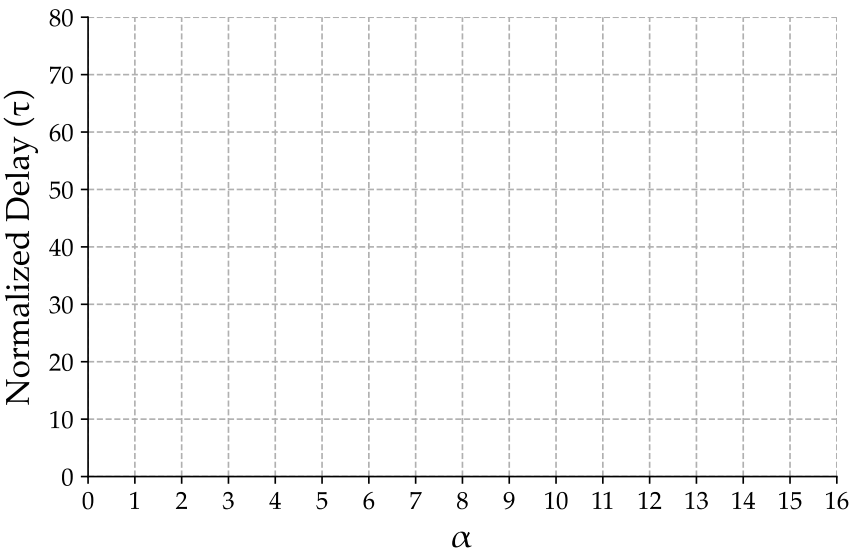




- Consider using a larger NAND4 standard cell
- Calculate delay for NAND4X2, NANDX4, NANDX8, NANDX16

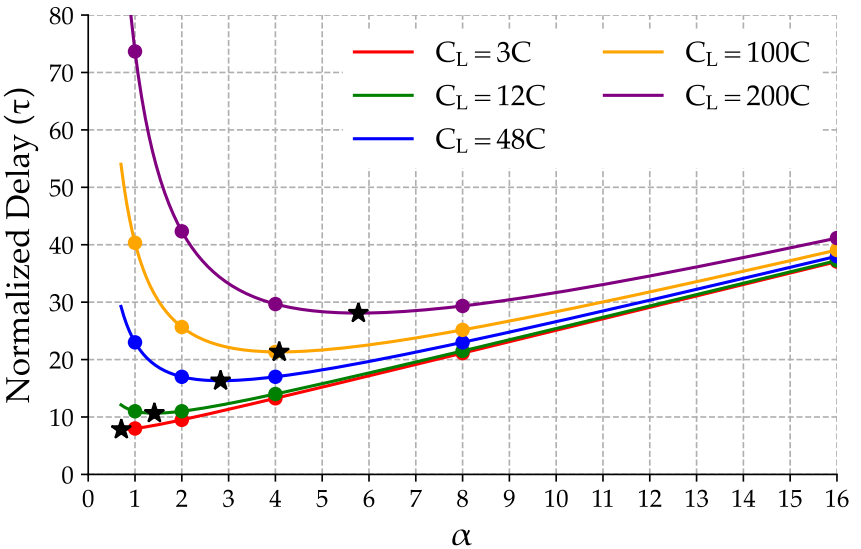






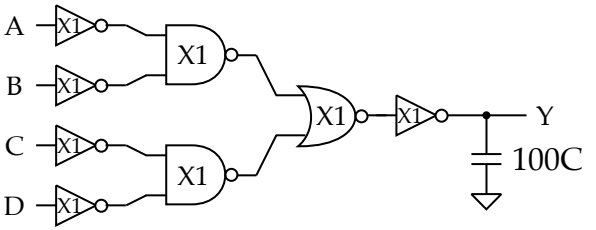
- Find optimal sizing
  - Write equation for delay as a function of α
  - Take partial derivative with respect to α, set equal to zero, solve

Key Result: Optimal path delay is when the load delays are balanced across all gates along the path

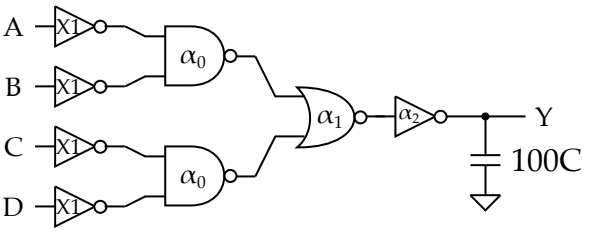


- Standard cell libraries usually provide
  - X1, X2, X4, X8, X16, X32 drive strengths for inverters
  - X1, X2, X4 drive strengths for most other gates
- Even with discrete drive strengths, actual delay is close to optimal
  - For bigger loads simply add inverters at the output

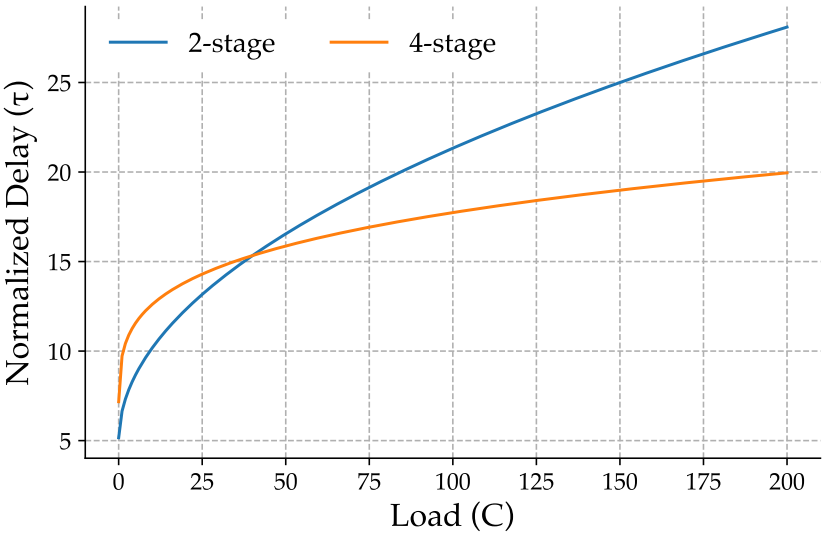
- Consider the following 4-stage implementation of a four-input OR gate driving a large load (i.e., large fanout)



- Find optimal sizing
  - Optimal path delay is when the load delays are balanced

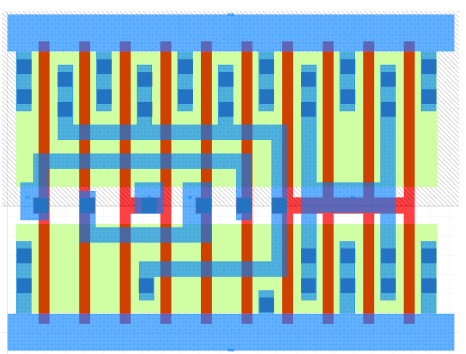


- Optimal delay vs output load assuming full-custom sizing
- Similar trend for standard cells (as long as multiple drive strengths are available!)



2.4. Simple Logic Cells

Inverters	INVX1, INVX2, INVX4, INVX8, INVX16, INVX32
Buffers	BUFX1, BUFX2, BUFX4, BUFX8, BUFX16, BUFX32
2-input NAND	NAND2X1, NAND2X2, NAND2X4
3-input NAND	NAND3X1, NAND3X2, NAND3X4
4-input NAND	NAND4X1, NAND4X2, NAND4X4
2-input NOR	NOR2X1, NOR2X2, NOR2X4
3-input NOR	NOR3X1, NOR3X2, NOR3X4
4-input NOR	NOR4X1, NOR4X2, NOR4X4
2-input AND	AND2X1, AND2X2, AND2X4
3-input AND	AND3X1, AND3X2, AND3X4
4-input AND	AND4X1, AND4X2, AND4X4
2-input OR	OR2X1, OR2X2, OR2X4
3-input OR	OR3X1, OR3X2, OR3X4
4-input OR	OR4X1, OR4X2, OR4X4



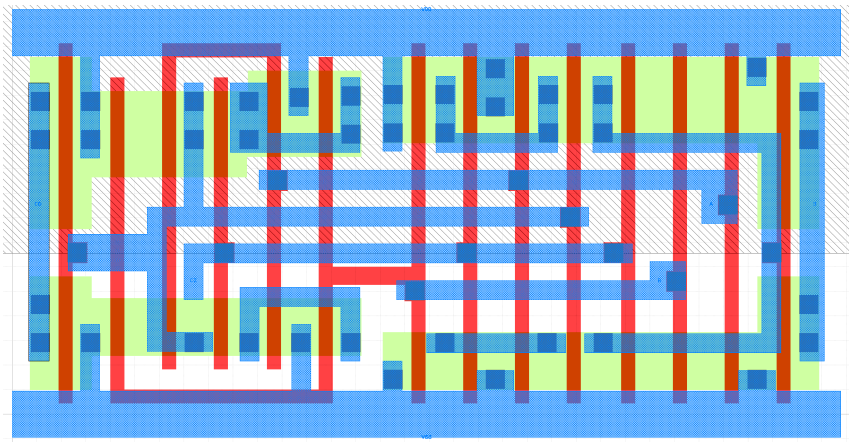
layout from
open 45 nm library

2.5. Complex Logic Cells

2-input XOR	XOR2X1, XOR2X2
2-input XNOR	XNOR2X1, XNOR2X2
3-input And-Or-Inverting	AOI21X1, AOI21X2, AOI21X4
4-input And-Or-Inverting	AOI22X1, AOI22X2, AOI22X4
	AOI211X1, AOI211X2, AOI211X4
5-input And-Or-Inverting	AOI211X1, AOI211X2, AOI211X4
6-input And-Or-Inverting	AOI222X1, AOI222X2, AOI222X4
3-input Or-And-Inverting	OAI21X1, OAI21X2, OAI21X4
4-input Or-And-Inverting	OAI22X1, OAI22X2, OAI22X4
	OAI211X1, OAI211X2, OAI211X4
5-input Or-And-Inverting	OAI211X1, OAI211X2, OAI211X4
6-input Or-And-Inverting	OAI222X1, OAI222X2, OAI222X4

2.6. Mux and Arithmetic Cells

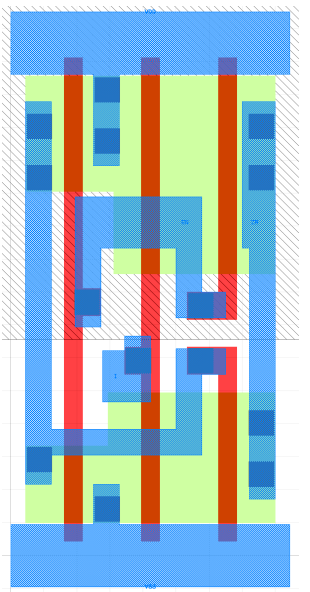
2-input Multiplexors	MUX2X1, MUX2X2
Adders	HAX1, FAX1



layout from open 45 nm library

2.7. Special Cells

Tri-State Buffers	TBUFX1, TBUFX2, TBUFX4, TBUFX8, TBUFX16
Tri-State Inverters	TINVX1
Tie	LOGIC0X1, LOGIC1X1



2.8. More Cells

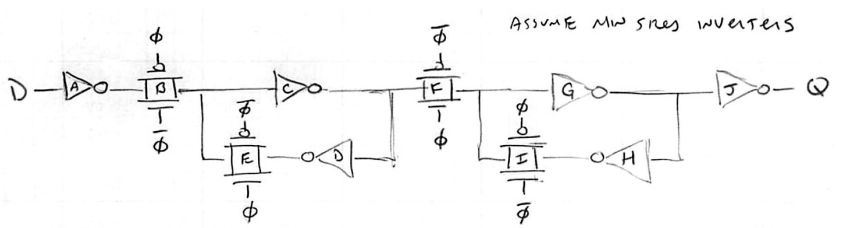
- Even more AOI and OAI standard cells
- IAO and IOA standard cells
- Multi-input XOR, XNOR standard cells
- Majority gate standard cells
- Non-inverting multiplexor standard cells
- Booth encoding standard cells
- Multiple channel lengths
- Multiple threshold voltages
- Multiple supply voltages (level converting standard cells)

3. Sequential Standard Cells

Behavioral View	Must model sequential behavior
Schematic View	Same as combinational
Layout View	Same as combinational
Extracted Schematic View	Same as combinational
Front-End View	Must model sequential timing
Back-End View	Same as combinational

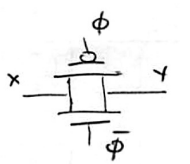
3.1. DFFX1

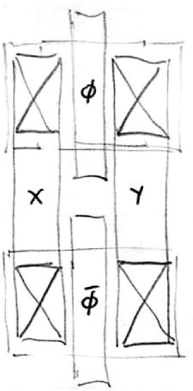
- Why do we add extra inverters at the input and output?



Setup Time	Latest the input can change before edge while still capturing the value
Hold Time	Earliest the input can change after edge while still capturing the value
Clock-to-Q Propagation Delay	Maximum delay after clock rises until the output is guaranteed to be stable
Clock-to-Q Contamination Delay	Minimum delay after clock rises until the output might change

RC Model for Transmission Gate

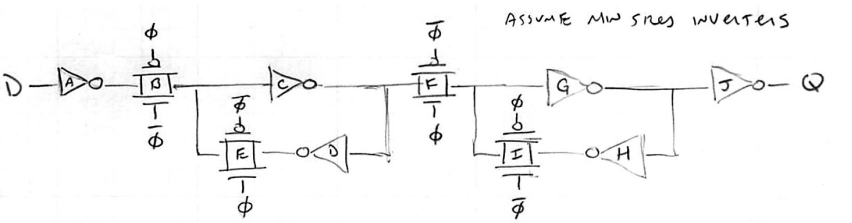




- Assume size of NMOS and PMOS are both minimum width
- Assume a transistor passing a weak value has 2x worse effective resistance
- Derive an RC model for this transmission gate

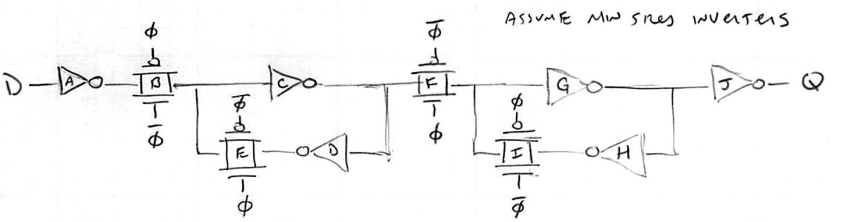
Setup Time

- To calculate the setup time we ask ourselves, "How far does the input signal need to propagate so that we can reliably flip the leader latch before the clock edge?"



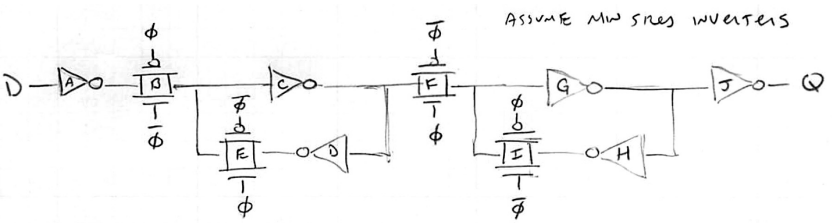
Clock-to-Q Propagation Delay

- To calculate the propagation delay, we ask ourselves, “How long does it take after the rising edge to propagate the internal state?”



Hold Time

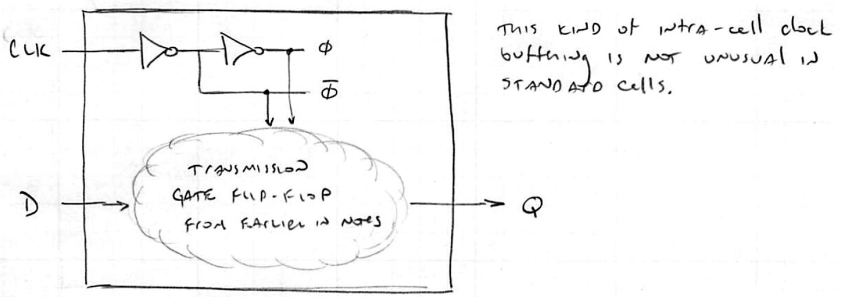
- Hold time is how long we need to keep the input stable *after* the rising edge in order to prevent corrupting the state



- If we assume θ and $\overline{\theta}$ change instantaneously on the rising clock edge, then we actually have a *negative* hold time
- If the input changes right after the edge then by the time it gets to the first transmission gate (gate B) that gate is already open and input signal cannot corrupt the state
- In fact, the input can change a little *before* the edge since it takes some time to propagate through the first inverter

Internal Clock Delay

- What if we assume there is some delay between the clock input pin of our cell and the actual θ and $\overline{\theta}$ signals?

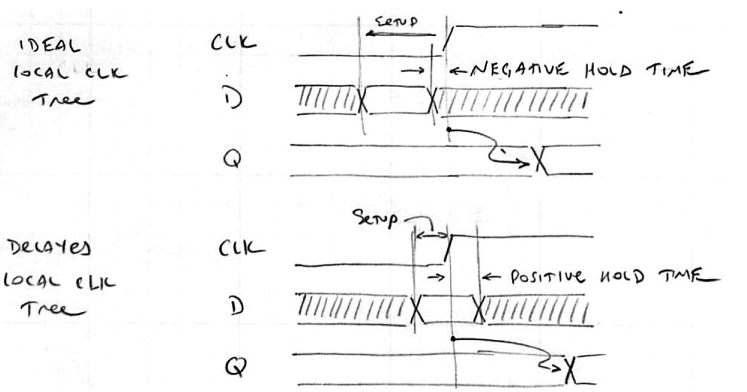


- How does this impact setup time, propagation delay, hold time?
- Remember that all three metrics are defined with respect to the clock pin of the cell *not* the internal θ and $\overline{\theta}$ signals
- First calculate the delay through the local clock tree (clock insertion delay), then factor this into these three metrics

Calculate the delay through the local clock tree

- What is the output load on the local clock tree?

- Essentially what we have done is shift the sampling window



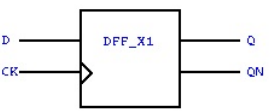
NANGATE

DFF_X1

Databook Build Date: Thursday Feb 17 15:07 2011

Conditions for characterization library **NangateOpenCellLibrary**, corner **NangateOpenCellLibrary_typical_typical**: Vdd= **1.10**V, Tj= **25.0** deg. C .
Additional corners: NangateOpenCellLibrary [NangateOpenCellLibrary_slow_slow], NangateOpenCellLibrary [NangateOpenCellLibrary_fast_fast], NangateOpenCellLibrary [NangateOpenCellLibrary_worst_low_worst_low], NangateOpenCellLibrary [NangateOpenCellLibrary_low_temp_low_temp].
Output transition is defined from **30%** to **70%** (rising) and from **70%** to **30%** (falling) output voltage.
Propagation delay is measured from **50%** (input rise) or **50%** (input fall) to **50%** (output rise) or **50%** (output fall).

Description	Pos. edge Flip-Flop with drive strength X1
Strength	1
Cell Area	4.522 um^2
Equation	Q = "(D)" QN = "(!(D))"
Clock	CK
Type	Sequential
Input	D
Output	Q, QN
PG Pins	VDD (primary_power), VSS (primary_ground)



State Table					
CK	D	$IQ_{(int)}$	$IQN_{(int)}$	Q	QN
R	L	-	-	L	H
R	H	-	-	H	L
F	-	L	H	L	H
F	-	H	L	H	L

Propagation Delay [ns]					
Input Transition [ns]		0.0012		0.1985	
Load Capacitance [fF]		0.3656	60.73	0.3656	60.73
CK to Q	fall	0.08	0.15	0.10	0.18
	rise	0.08	0.22	0.11	0.25
CK to QN	fall	0.06	*0.15*	0.08	*0.17*
	rise	0.06	*0.21*	0.08	*0.23*

Output Transition [ns]					
Input Transition [ns]		0.0012		0.1985	
Load Capacitance [fF]		0.3656	60.73	0.3656	60.73
CK to Q	fall	0.01	0.07	0.01	0.07
	rise	0.01	0.14	0.01	0.14
CK to QN	fall	0.01	*0.07*	0.01	*0.07*
	rise	0.01	*0.14*	0.01	*0.14*

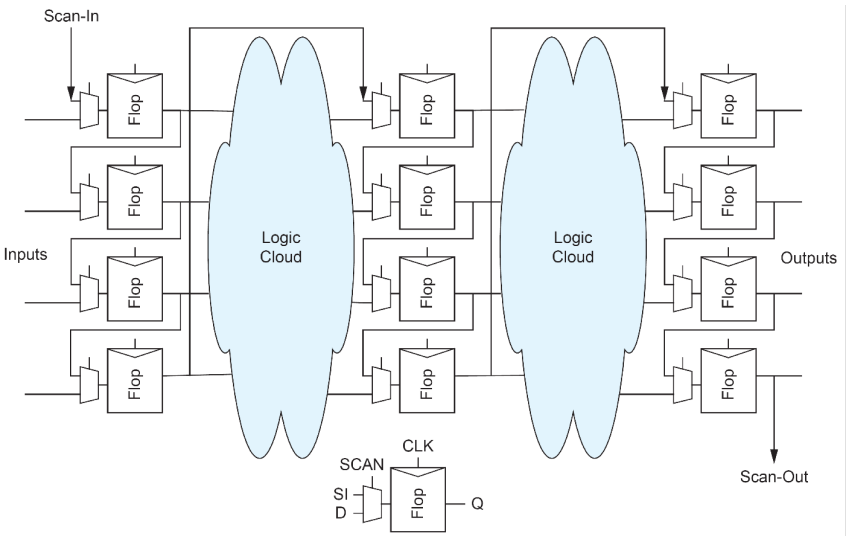
Constraints Time [ns]		
Setup CK to D	fall	0.10
	rise	0.06
Hold CK to D	fall	0.15
	rise	0.12

Capacitance [fF]	
CK	0.9497
D	1.1403

Leakage [nW]
79.11

3.2. Scan Flip-Flops

- Flip-flops with extra scan input
  - Serially scan in a value for every flip-flop
  - Toggle clock
  - Serially scan out the value of every flip-flop



NANGATE

SDFF_X1

Databook Build Date: Thursday Feb 17 15:07 2011

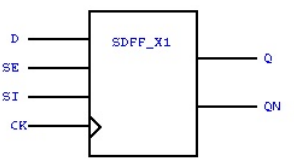
Conditions for characterization library **NangateOpenCellLibrary**, corner **NangateOpenCellLibrary_typical_typical**: Vdd= **1.10**V, Tj= **25.0** deg. C .

Additional corners: NangateOpenCellLibrary [NangateOpenCellLibrary_slow_slow], NangateOpenCellLibrary [NangateOpenCellLibrary_fast_fast], NangateOpenCellLibrary [NangateOpenCellLibrary_worst_low_worst_low], NangateOpenCellLibrary [NangateOpenCellLibrary_low_temp_low_temp].

Output transition is defined from **30%** to **70%** (rising) and from **70%** to **30%** (falling) output voltage.

Propagation delay is measured from **50%** (input rise) or **50%** (input fall) to **50%** (output rise) or **50%** (output fall).

Description	Pos. edge Flip-Flop with scan, and drive strength X1
Strength	1
Cell Area	6.118 um^2
Equation	Q = "(((SE * SI) + (D * !SE)))" QN = "(!(((SE * SI) + (D * !SE))))"
Clock	CK
Type	Sequential
Scan Enable	SE
Scan Data	SI
Input	D
Output	Q, QN
PG Pins	VDD (primary_power), VSS (primary_ground)



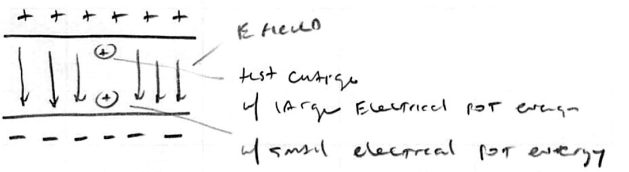
State Table								
CK	D	SE	SI	$IQ_{(int)}$	$IQN_{(int)}$	Q	QN
R	L	L	-	-	-	L	H
R	H	L	-	-	-	H	L
R	-	H	L	-	-	L	H
R	-	H	H	-	-	H	L
F	-	-	-	L	H	L	H
F	-	-	-	H	L	H	L

Propagation Delay [ns]					
Input Transition [ns]		0.0012		0.1985	
Load Capacitance [fF]		0.3656	60.5774	0.3656	60.5774
CK to Q	fall	0.06	0.15	0.08	0.17
	rise	0.06	0.21	0.07	0.22
CK to QN	fall	0.08	*0.15*	0.10	*0.17*
	rise	0.09	*0.23*	0.10	*0.25*

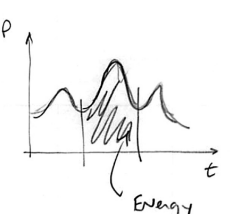
Output Transition [ns]					
Input Transition [ns]		0.0012		0.1985	
Load Capacitance [fF]		0.3656	60.5774	0.3656	60.5774
CK to Q	fall	0.01	0.07	0.01	0.07
	rise	0.01	0.14	0.01	0.14
CK to QN	fall	0.01	*0.07*	0.01	*0.07*
	rise	0.01	*0.14*	0.01	*0.14*

3.3. CLKGATEX1

- Extracted schematic view for timing *and* energy characterization
  - Energy is a measure of work
  - Power is the rate at which work is done

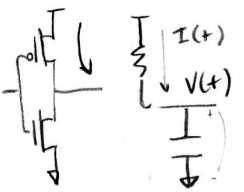


Electric Potential Energy	Capacity for doing work which arises from position of charge in electric field	Joules
Electric Potential	Electric potential energy of a position per unit charge	Volts $1V = 1J/C$ $\Delta V = \Delta E/Q$
Current	Rate at which charge flows past position	Amps $1A = 1C/S$ $I = Q/\Delta t$
Power	Rate at which electric energy is supplied or consumed	Watts $1W = 1J/S$ $P = \Delta E/\Delta t = \frac{\Delta V \cdot Q}{Q/I} = VI$



$$E = \int_0^T P(t)\,dt$$

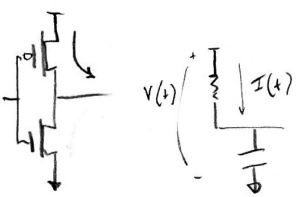
Energy Stored on a Capacitor



$$
\begin{aligned}
E_C &= \int_0^\infty P(t)dt = \int_0^\infty V(t)I(t)dt \\
&= \int_0^\infty V(t)\frac{dQ}{dt}dt = \int_0^\infty V(t)\frac{Cdv}{dt}dt \\
&= C\int_0^{V_{DD}} V(t)dV = \frac{1}{2}CV_{DD}{}^2
\end{aligned}
$$

- So on $1 \rightarrow 0$ input transition, $\frac{1}{2}CV_{DD}{}^2$ is stored on capacitor
- This energy is released on $0 \rightarrow 1$ input transition

Energy Delivered From Power Supply



$$
\begin{aligned}
E_{\text{supply}} &= \int_0^\infty P(t)dt = \int_0^\infty V_{DD}I(t)dt \\
&= V_{DD}\int_0^\infty \frac{dQ}{dt}dt = V_{DD}\int_0^\infty \frac{Cdv}{dt}dt \\
&= CV_{DD}\int_0^{V_{DD}} dV = CV_{DD}{}^2
\end{aligned}
$$

- $0 \rightarrow 1$ output transition
  - $CV_{DD}{}^2$ energy is delivered from power supply
  - half dissipated as heat in PMOS; half stored on the capacitor
- $1 \rightarrow 0$ output transition
  - no energy is delivered from power supply
  - remaining energy on capacitor dissipated as heat in NMOS
- Let α be the activity factor, probability of $0 \rightarrow 1$ output transition

$$E = \alpha CV_{DD}{}^2$$

- Front-end view characterizes energy as:
  - $E_{0 \to 1} = C_L V_{DD}^2 + E_{internal,0 \to 1}$
  - $E_{1 \to 0} = E_{internal,1 \to 0}$
- Internal energy is stored in front-end view and includes:
  - Energy to charge up parasitic diffusion capacitance
  - Short circuit energy when both PMOS and NMOS are briefly on
- Internal energy is still a function of load capacitance since the load impacts how long both transistors are on

Non-Linear Energy Model for $E_{internal,1 \to 0}$ (pJ)

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	0.000	0.000	0.000	0.000	0.000	0.000	-0.001
0.005	0.000	0.000	0.000	0.000	0.000	0.000	-0.001
0.017	0.000	0.000	0.000	0.000	0.000	-0.001	-0.001
0.041	0.288	0.149	0.031	-0.001	-0.001	-0.001	-0.001
0.078	0.972	0.824	0.649	0.409	0.159	-0.001	-0.002
0.130	1.891	1.765	1.588	1.265	0.831	0.423	0.157
0.199	3.064	2.982	2.823	2.482	1.898	1.213	0.643

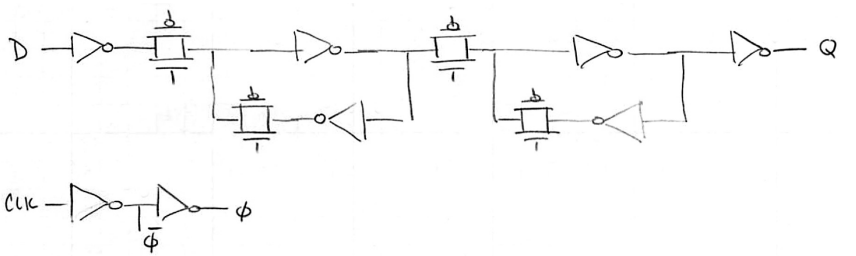
Negative energy means net current briefly returned to power supply

Non-Linear Energy Model for $E_{internal,0 \to 1}$ (pJ)

	Load Capacitance (fF)						
Slew (ns)	0.366	1.898	3.796	7.591	15.183	30.365	60.730
0.001	1.847	1.913	1.943	1.976	1.918	1.993	1.804
0.005	1.785	1.828	1.850	1.878	1.861	1.924	1.788
0.017	1.890	1.926	1.897	1.907	1.908	1.891	1.916
0.041	2.169	2.197	2.245	2.176	1.994	1.979	1.838
0.078	2.904	2.822	2.735	2.759	2.532	2.170	2.082
0.130	4.073	3.908	3.757	3.549	3.379	2.891	2.591
0.199	5.652	5.456	5.225	4.893	4.422	4.003	3.154

Flip-Flop Energy

- Dynamic energy in a flip-flop comes from two sources:
  - toggling the data lines
  - toggling the clock
- First, let's label all of the gate and parasitic caps



- Estimate worst case energy per write/read access by calculating the maximum switched cap while assuming every node toggles

- Let's assume the following:
  - data activity factor of 0.1
  - clock activity factor of 1 (toggles once per cycle!)

$$E_{\text{data}} = \alpha C {V_{dd}}^2 = (0.1) \times 52\ \text{C} \times 1.15\ \text{fF/C} \times (1.8\ \text{V})^2 = 19\ \text{fJ}$$
$$E_{\text{clock}} = \alpha C {V_{dd}}^2 = (1.0) \times 20\ \text{C} \times 1.15\ \text{fF/C} \times (1.8\ \text{V})^2 = 75\ \text{fJ}$$

- Once we factor in activity factor, clock energy is significantly higher than data energy
- Let's estimate the total data/clock energy for multi-bit register

- Clock gating only toggles the clock when the register is enabled

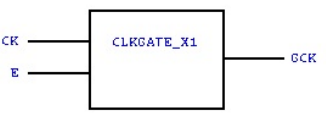
- Let's estimate the total data/clock energy with clock gating

NANGATE CLKGATE_X1

Databook Build Date: Thursday Feb 17 15:07 2011

Conditions for characterization library **NangateOpenCellLibrary**, corner **NangateOpenCellLibrary_typical_typical**: Vdd= **1.10**V, Tj= **25.0** deg. C .
Additional corners: NangateOpenCellLibrary [NangateOpenCellLibrary_slow_slow], NangateOpenCellLibrary [NangateOpenCellLibrary_fast_fast], NangateOpenCellLibrary [NangateOpenCellLibrary_worst_low_worst_low], NangateOpenCellLibrary [NangateOpenCellLibrary_low_temp_low_temp].
Output transition is defined from **30%** to **70%** (rising) and from **70%** to **30%** (falling) output voltage.
Propagation delay is measured from **50%** (input rise) or **50%** (input fall) to **50%** (output rise) or **50%** (output fall).

Strength	1
Cell Area	3.458 um^2
Enable	E
Type	Sequential
Output	GCK
PG Pins	VDD (primary_power), VSS (primary_ground)



State Table			
CK	E	$IQ_{(int)}$	GCK
L	L	-	L
L	H	-	L
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

Propagation Delay [ns]					
Input Transition [ns]		0.0012		0.1985	
Load Capacitance [fF]		0.3656	60.73	0.3656	60.73
CK to GCK	fall	0.02	0.18	0.08	0.24
	rise	0.02	0.17	0.04	0.19

Output Transition [ns]					
Input Transition [ns]		0.0012		0.1985	
Load Capacitance [fF]		0.3656	60.73	0.3656	60.73
CK to GCK	fall	0.00	0.14	0.01	0.14
	rise	0.00	0.14	0.01	0.14

Constraints Time [ns]		
Setup CK to E	fall	0.10
	rise	0.10
Hold CK to E	fall	0.13
	rise	0.11

Capacitance [fF]	
CK	1.8379
E	0.9152

Leakage [nW]
48.65

Input Pin Power Consumption [nW/GHz]			
Input Transition [ns]		0.0012	0.1985
CK	fall	4942.58	7243.83
	rise	1307.26	3467.12
E	fall	1575.33	1868.05
	rise	672.73	920.23

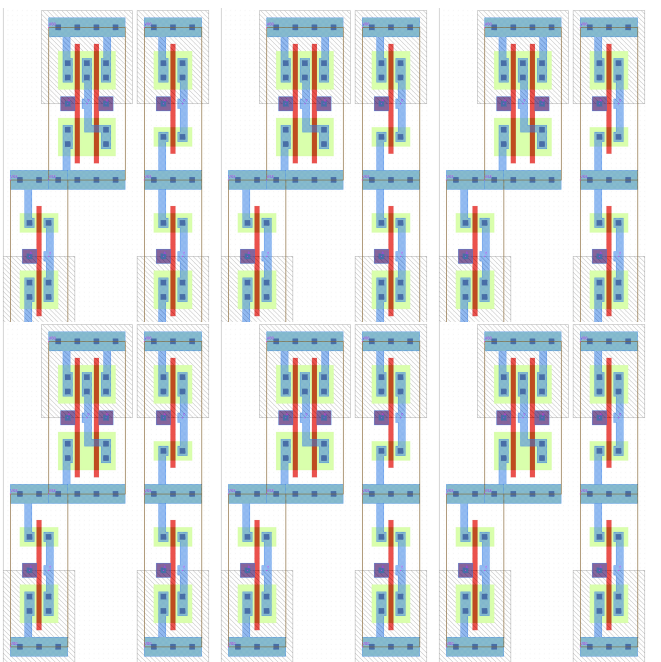
Dynamic Power Consumption [uW/GHz]					
Input Transition [ns]		0.0012		0.1985	
Load Capacitance [fF]		0.3656	60.73	0.3656	60.73
CK to GCK	fall	5.07	7.03	8.20	10.90
	rise	3.11	3.54	6.66	7.18

3.4. More Cells

Latches	DLHX1, DLHX2, DLLX1, DLHX1, TLATX1
Flip-Flops	DFFX1, DFFX2
Flip-Flops (reset)	DFFRX1, DFFRX2
Flip-Flops (set)	DFFSX1, DFFSX2
Flip-Flops (both)	DFFRSX1, DFFRSX2
Scan Flip-Flops	DFFX1, DFFX2
Scan Flip-Flops (reset)	DFFRX1, DFFRX2
Scan Flip-Flops (set)	DFFSX1, DFFSX2
Scan Flip-Flops (both)	DFFRSX1, DFFRSX2
Clock buffers	CLKBUFX1, CLKBUFX2, CLKBUFX3
Clock gate	CLKGATEX1, CLKGATEX2 CLKGATEX2, CLKGATEX4, CLKGATEX8

4. Physical Standard Cells

Filler Cells	Connect wells, power/ground rails, various widths
Tap Cells	Well/substrate contacts for “tapless” libraries
Decap Cells	Decoupling capacitance between Vdd and ground
Endcap Cells	Place at end of each row to avoid DRC violations
Antenna Cells	Insert diodes to avoid antenna DRC violations



5. Commercial Flow

Behavioral View	Verilog	`stdcells.v`
Schematic View	SPICE	`stdcells.sp`
Layout View	GDS	`stdcells.gds`
Extracted Schematic View	SPICE	`stdcells-rcx.sp`
Front-End View	Liberty	`stdcells.lib`
Back-End View	LEF	`stdcells.lef`

Liberty files often compiled into binary .db format

Behavioral View → Verilog *(from open 45 nm library)*

```
module INV_X1 (A, ZN);
  input A;
  output ZN;

  not(ZN, A);

  specify
    (A => ZN) = (0.1, 0.1);
  endspecify

endmodule
```

```
module NAND2_X1 (A1, A2, ZN);
  input A1;
  input A2;
  output ZN;

  not(ZN, i_10);
  and(i_10, A1, A2);

  specify
    (A1 => ZN) = (0.1, 0.1);
    (A2 => ZN) = (0.1, 0.1);
  endspecify

endmodule
```

Front-End View → Liberty

```
cell (INV_X1)
{
  drive_strength     : 1;
  area               : 0.532000;
  cell_leakage_power : 14.353185;
  leakage_power () { when : "!A"; value : 10.102224; }
  leakage_power () { when :  "A"; value : 18.604146; }

  pin (A) {
    direction        : input;
    capacitance      : 1.700230;
    fall_capacitance : 1.549360;
    rise_capacitance : 1.700230;
  }

  pin (ZN) {
    direction        : output;
    max_capacitance  : 60.730000;
    function         : "!A";

    timing () {
      related_pin    : "A";
      timing_sense   : negative_unate;

      cell_fall(Timing_7_7) {
        index_1(" 0.001, 0.004, 0.017, 0.040, 0.078, 0.130, 0.198");
        index_2(" 0.365, 1.897, 3.795, 7.591,15.182,30.365,60.730");
        values (" 0.003, 0.005, 0.007, 0.012, 0.021, 0.039, 0.076", \
                " 0.004, 0.006, 0.009, 0.013, 0.022, 0.041, 0.078", \
                " 0.005, 0.009, 0.013, 0.019, 0.028, 0.046, 0.083", \
                " 0.005, 0.010, 0.016, 0.024, 0.038, 0.057, 0.094", \
                " 0.002, 0.009, 0.016, 0.028, 0.045, 0.072, 0.111", \
                "-0.002, 0.006, 0.015, 0.029, 0.051, 0.084, 0.133", \
                "-0.010, 0.000, 0.011, 0.028, 0.054, 0.093, 0.152");
      }

    ...
}
```

Back-End View → LEF

```
MACRO INV_X1
  CLASS    core;
  SYMMETRY X Y;
  SIZE     0.38 BY 1.4;

  PIN A
    DIRECTION INPUT;
    PORT LAYER metal1;
      POLYGON 0.06 0.525 0.165 0.525 0.165 0.7 0.06 0.7;
    END
  END A

  PIN ZN
    DIRECTION OUTPUT;
    PORT LAYER metal1;
      POLYGON 0.23 0.15 0.325 0.15 0.325 1.25 0.23 1.25;
    END
  END ZN

  PIN VDD
    DIRECTION INOUT;
    USE       power;
    SHAPE     ABUTMENT;
    PORT LAYER metal1;
      POLYGON 0 1.315 0.04 1.315 0.04 0.975 0.11 ...;
    END
  END VDD

  PIN VSS
    DIRECTION INOUT;
    USE       ground;
    SHAPE     ABUTMENT;
    PORT LAYER metal1;
      POLYGON 0 -0.085 0.38 -0.085 0.38 0.085 0.11 ...;
    END
  END VSS

END INV_X1
```

Standard-Cell Design Flow