ECE 6745 Complex Digital ASIC Design
Topic 2: Basic Standard Cells

School of Electrical and Computer Engineering
Cornell University

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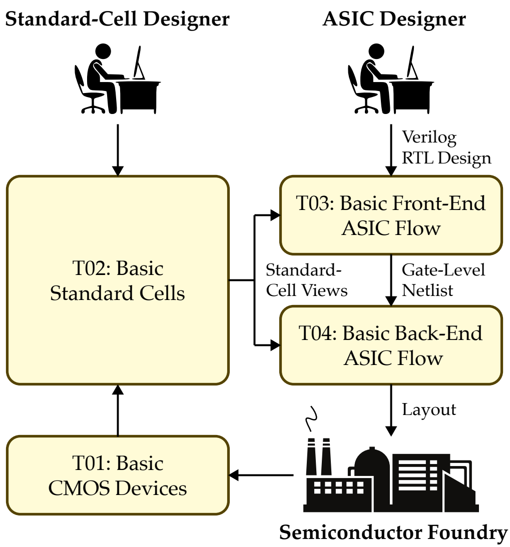
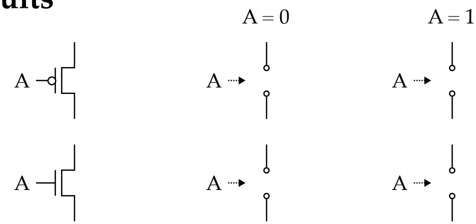
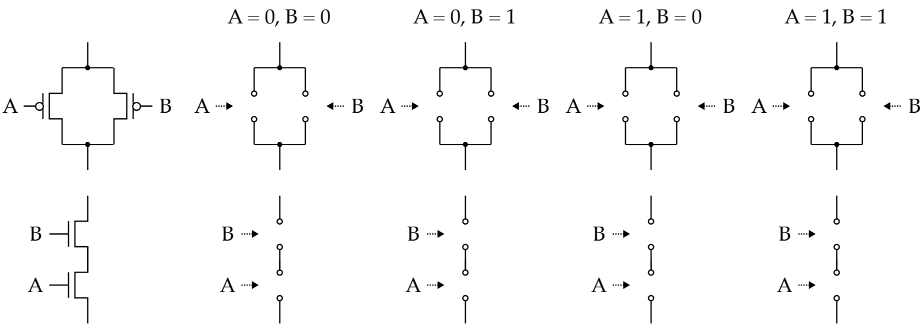

Standard-Cell Designer
ASIC Designer
Verilog
RTL Design
T03: Basic Front-End ASIC Flow
T02: Basic Standard Cells
Standard-
Cell Views
Gate-Level
Netlist
T04: Basic Back-End ASIC Flow
Layout
T01: Basic CMOS Devices
Semiconductor Foundry

1. Static CMOS Circuits

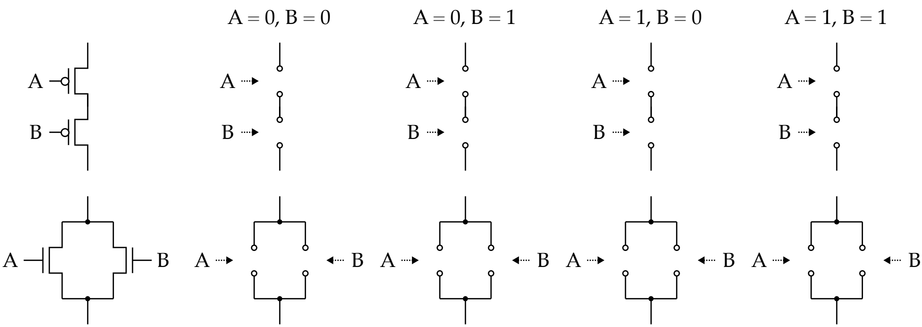
- A PMOS transistor is the complement of an NMOS transistor



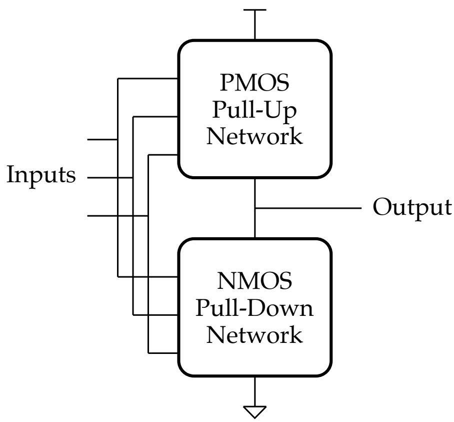
- PMOS in parallel are the complement of NMOS in series



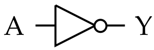
- PMOS in series are the complement of NMOS in parallel



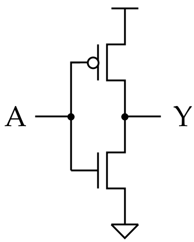
- Static CMOS circuits are divided into two parts:
  - Pull-up network exclusively uses PMOS transistors
  - Pull-down network exclusively uses NMOS transistors
- Pull-up network is the complement of the pull-down network
  - Every input is connected to exactly one PMOS and one NMOS
  - If one network is ON, the other network is OFF
  - Both networks are never ON at the same time
    (i.e., there is never a direct current path from VDD to ground)
  - Both networks are never OFF at the same time
    (i.e., the output should never be floating)



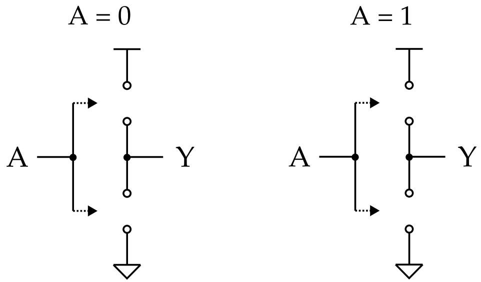
1.1. Inverter Circuit



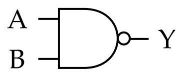
A	*Y*
0	1
1	0



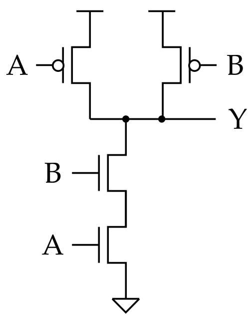
Switch-Level Model



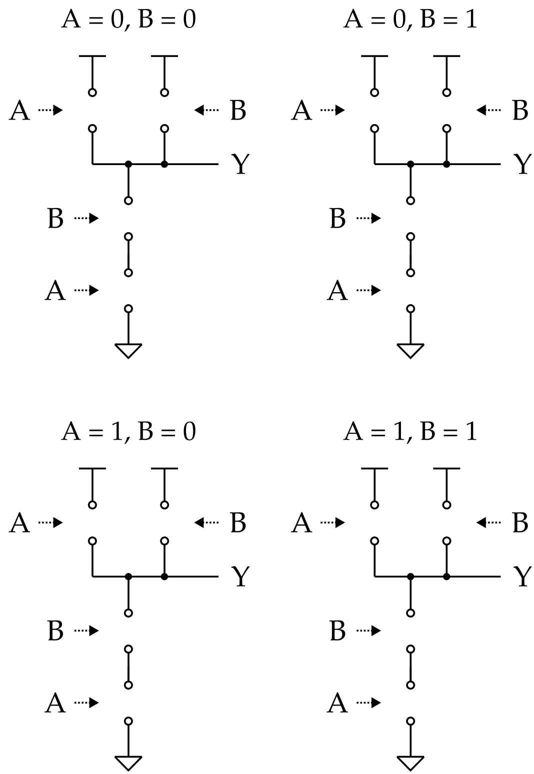
1.2. NAND2 Circuit



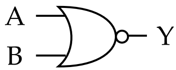
A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0



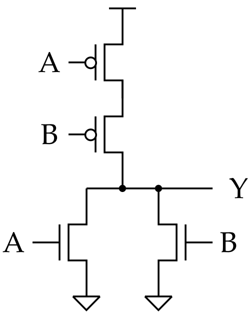
Switch-Level Model



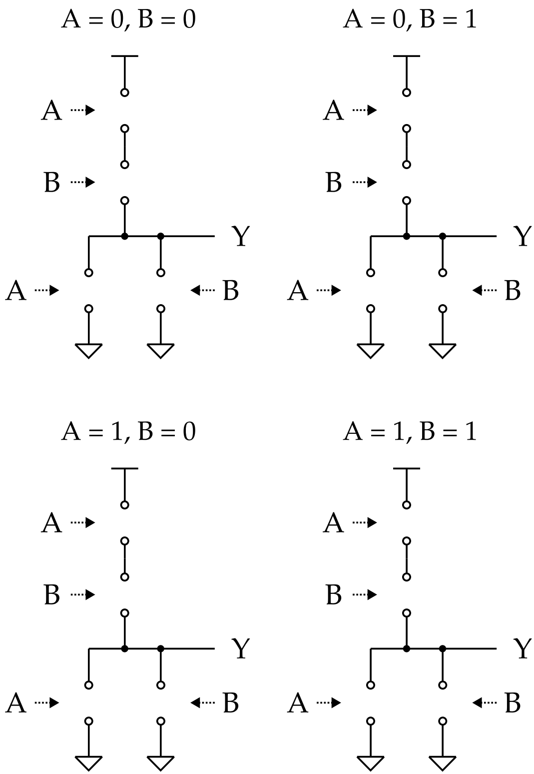
1.3. NOR2 Circuit



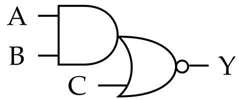
A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	0



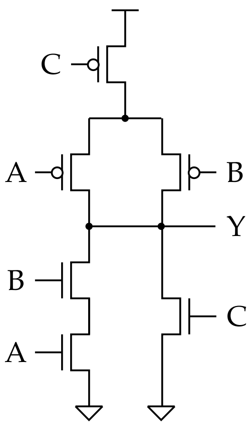
Switch-Level Model



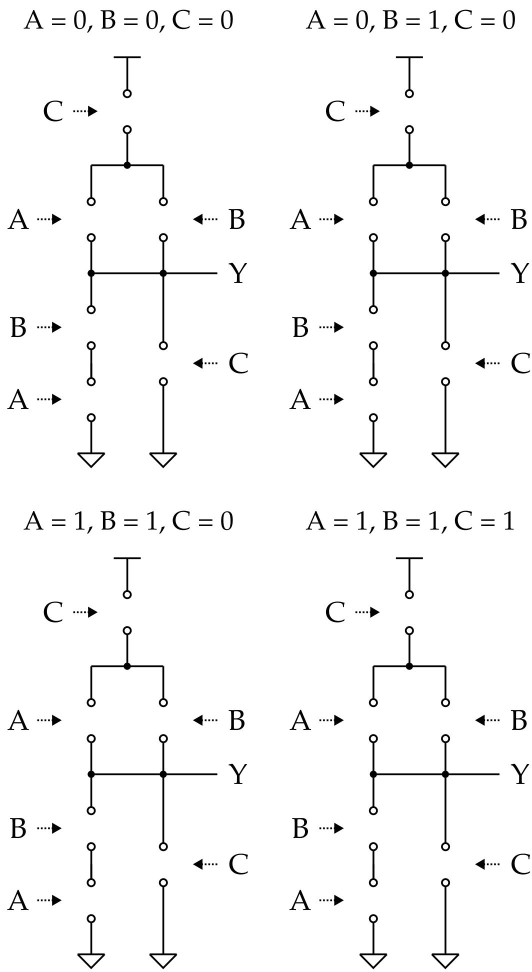
1.4. AOI21 Circuit



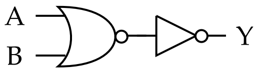
A	*B*	*C*	*Y*
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

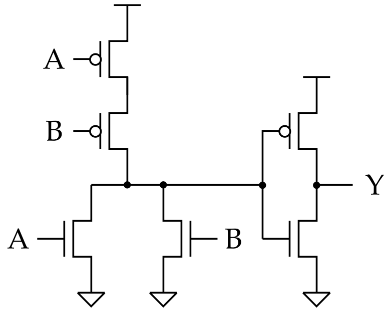


Switch-Level Model



1.5. Multi-Stage Circuits

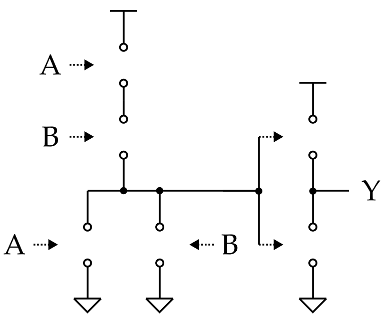




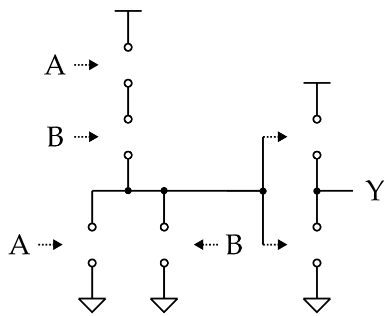
A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

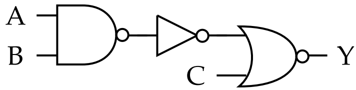
Switch-Level Model

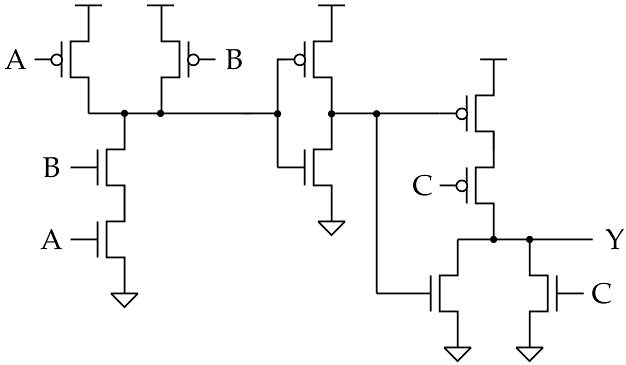
A = 0, B = 0



A = 0, B = 1

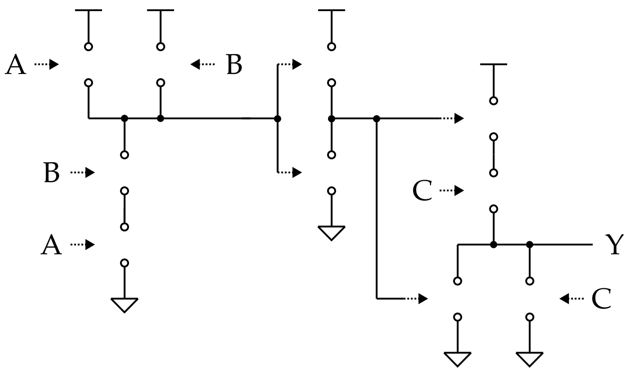




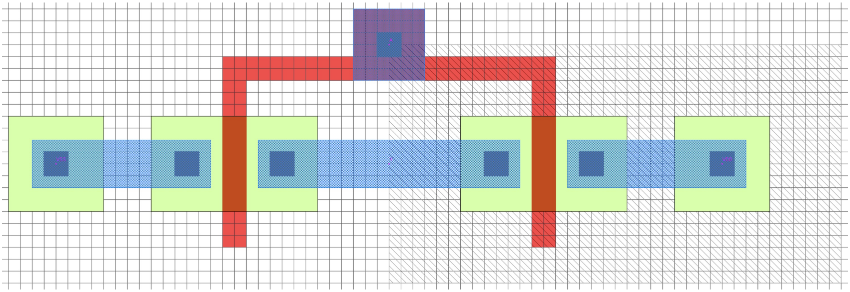


Switch-Level Model

A = 1, B = 1, C = 0

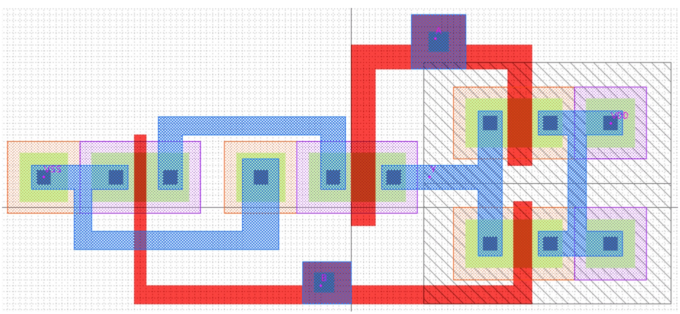


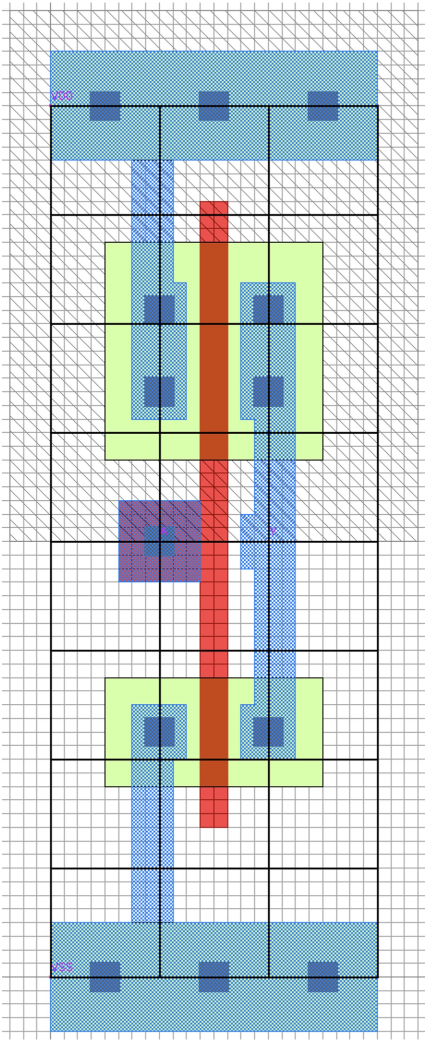
2. Full-Custom vs. Standard Cell Design



2.1. Full-Custom Design

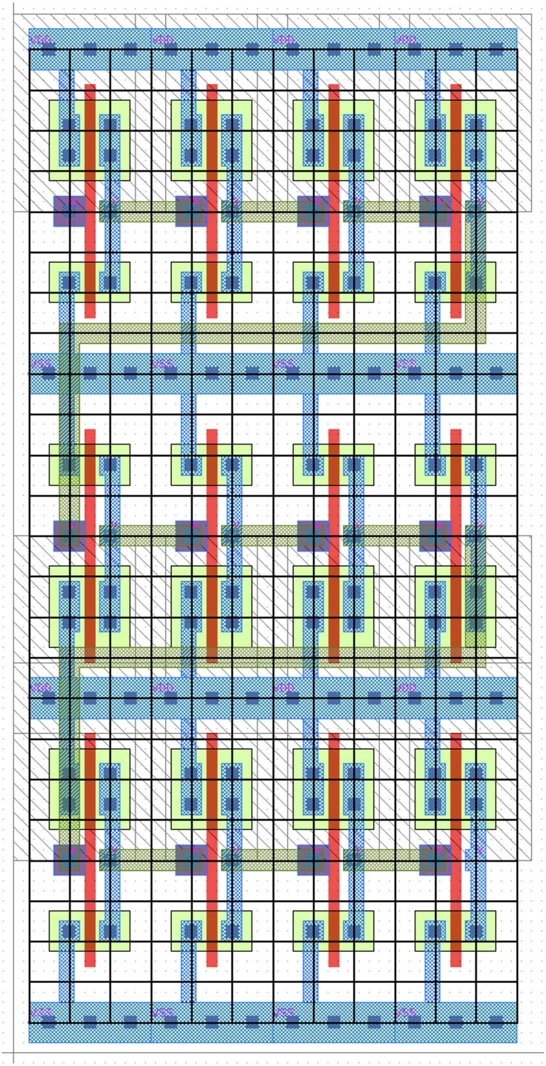
- Transistors can be in any position and any orientation
- N-well can be any size and in any location
- VDD and ground can use any metal layer and any location
- Substrate and n-well contacts can be in any location
- Metal routing is unconstrained
- Cells can be any height and any width
- Pins can be on any layer and in any location
- Cells can have any drive strengths with non-equal rise and fall times





2.2. Standard-Cell Design

- Standard transistor positions and orientation (PMOS at top, NMOS at bottom, vertical gates)
- Standard n-well size and location (n-well at top)
- Standard VDD and ground metal layer and locations (on metal 1, VDD rail 8λ tall at top, ground rail 8λ tall at bottom)
- Standard n-well and substrate contacts
- Standard boundry and extension of n-well, VDD, and ground rails beyond boundry (origin is in lower left)
- Standard metal 2+ routing grid (8λ track spacing)
- Standard cell height (64λ)
- Standard cell width (aligned to routing grid, i.e., 8λ, 16λ, 24λ, etc)
- Standard routing (all routing must be on polysilicon or metal 1)
- Standard pin layer and locations (on metal 1 and on routing grid)
- Standard set of available drive strengths



- Standard cells are designed to be abutted in rows
  - n-wells align
  - VDD rails align
  - Ground rails align
  - N-well contacts align
  - Substrate contacts align
- Each row is flipped vertically with respect to previous row
  - Enables sharing VDD and ground rails
- Standard-cell design rules ensure composing standard cells will not create any DRC violations
- Metal 2+ always routed on the routing grid

2.3. Standard-Cell Views

Behavioral View	Logical function of the standard cell, used for gate-level simulation
Schematic View	Transistor-level representation of standard cell, used for functional verification and layout-vs-schematic (LVS)
Layout View	Layout of standard cell, used for design-rule checking (DRC), layout-vs-schematic (LVS), resistance/capacitance extraction (RCX), and fabrication
Extracted Schematic View	Transistor-level representation with extracted resistance and capacitances, used for layout-vs-schematic (LVS) and timing characterization
Front-End View	High-level information about standard cell including area, input capacitance, logical function, and delay model; used in synthesis
Back-End View	Low-level information about standard cell including height, width, and pin locations; used in placement and routing

3. Standard Cells

- We will initially focus on the following seven basic standard cells
  - INVX1 : NOT gate (inverter)
  - NAND2X1 : 2-input NAND gate
  - NOR2X1 : 2-input NOR gate
  - AOI21X1 : 3-input AND-OR-Inverting gate
  - TIEHI : Tie output to logic one
  - TIELO : Tie output to logic zero
  - FILL : Filler cell
- X1 suffix means these standard cells all have the same drive strength (i.e., approximately the same effective resistance)
- We will later discuss more advanced standard cells
  - More complex combinational logic cells
  - Sequential logic cells (i.e., flip-flops)
  - Cells with larger drive stengths

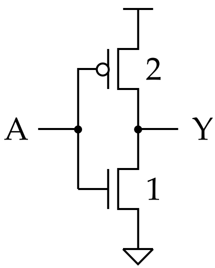
3.1. INVX1

Behavioral View

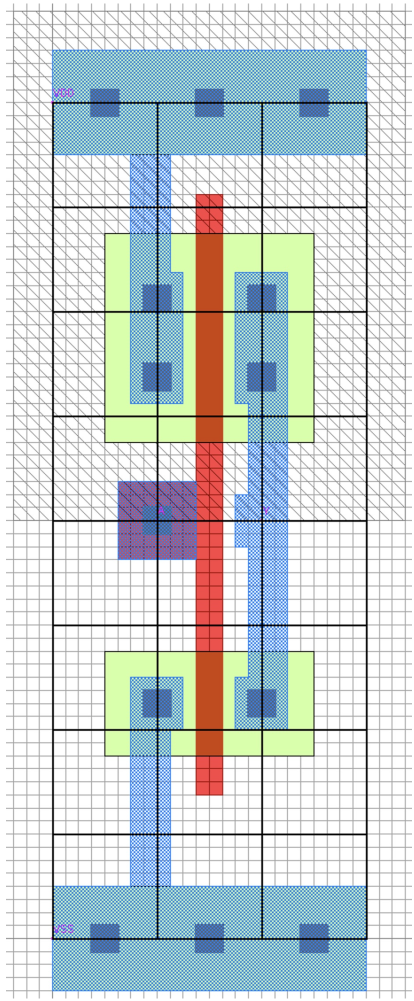
A	Y
0	1
1	0

$$Y = \overline{A}$$

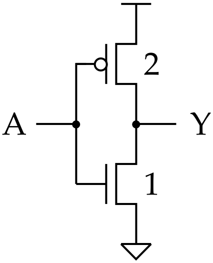
Schematic View

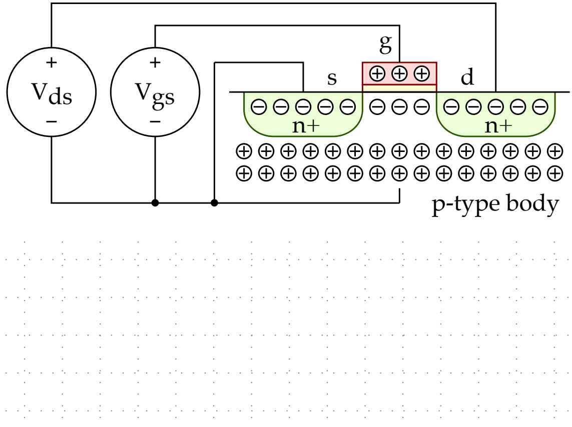


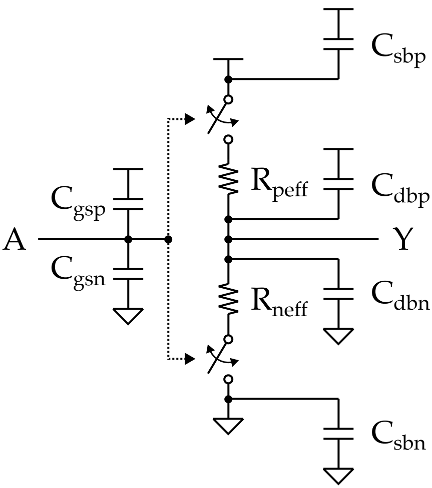
Layout View



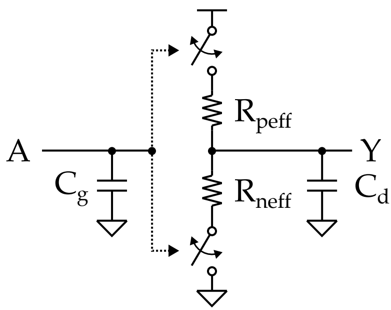
Extracted Schematic View



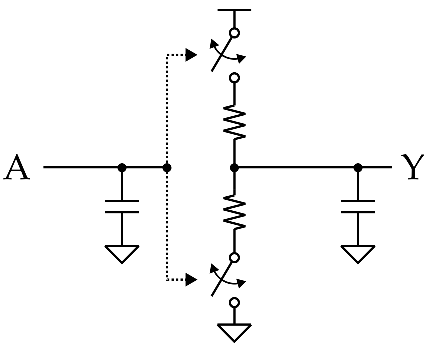


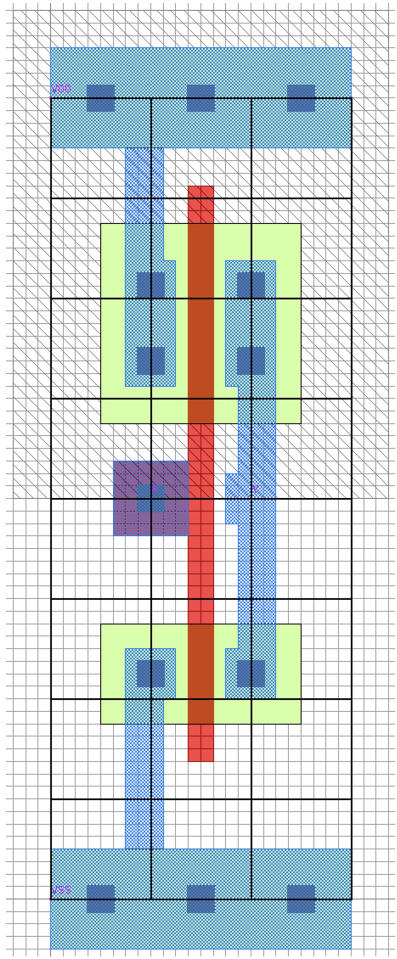


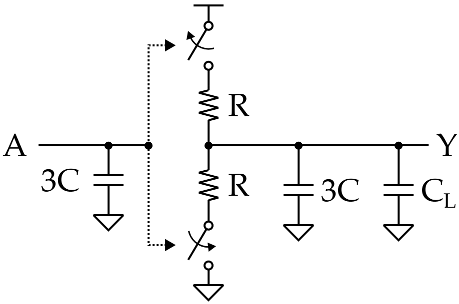
- C_{sb} capacitors do not actually switch, so ignore
- C_d and C_g capacitors tied to constant voltage sources so lump together

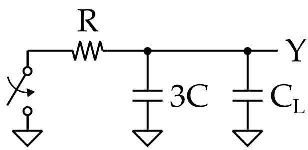


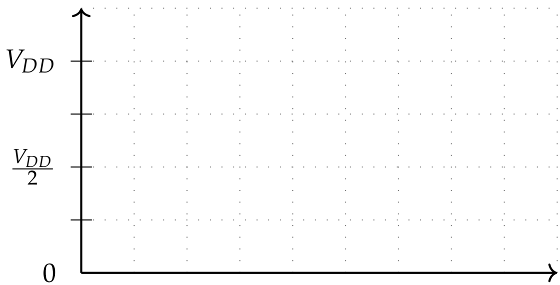
- C_g is the gate capacitance
- C_d is the diffusion capacitance or parasitic capacitance
- Let's use normalized units
  - Let R be the effective resistance of a minimum-sized NMOS
  - Let C be the gate capacitance of a minimum-sized NMOS
  - Let C be the diffusion capacitance of a minimum-sized NMOS
- Recall $R_{peff} = 2 \times R_{neff}$ for same transistor width









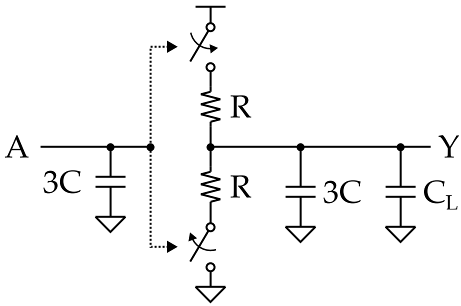


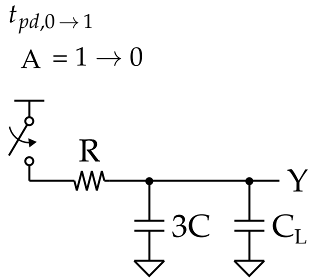
- Let t_{pd} be the time until $V_Y = V_{DD}/2$ (propagation delay)
- Let $\tau = R(3C + C_L) = 3RC + RC_L$ (time constant)

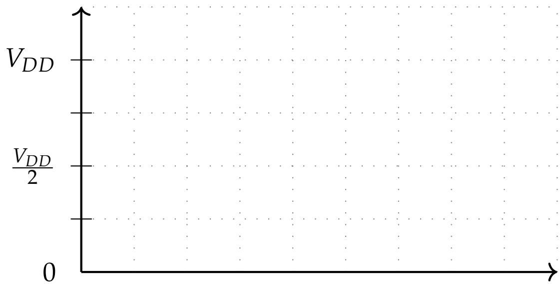
$$
\begin{aligned}
V_Y &= V_{DD}\, e^{-t/\tau} \\
V_{DD}/2 &= V_{DD}\, e^{-t/\tau} \\
1/2 &= e^{-t/\tau} \\
\ln(1/2) &= -t/\tau \\
-\tau \ln(1/2) &= t \\
t &= \tau \ln(2)
\end{aligned}
$$

- $t_{pd,1\rightarrow 0} = (3RC + RC_L) \cdot \ln(2)$
- We usually just assume effective resistance is scaled by ln(2)

$$\boxed{t_{pd,1\rightarrow 0} = 3RC + RC_L}$$







- Let t_{pd} be the time until $V_Y = V_{DD}/2$ (propagation delay)
- Let $\tau = R(3C + C_L) = 3RC + RC_L$ (time constant)

$$V_Y = V_{DD} \cdot (1 - e^{-t/\tau})$$
$$V_{DD}/2 = V_{DD} \cdot (1 - e^{-t/\tau})$$
$$V_{DD}/2 = 1 - e^{-t/\tau}$$
$$\ln(1/2) = -t/\tau$$
$$-\tau \ln(1/2) = t$$
$$t = \tau \ln(2)$$

- $t_{pd,0\rightarrow1} = (3RC + RC_L) \cdot \ln(2)$
- We usually just assume effective resistance is scaled by ln(2)

$$\boxed{t_{pd,0\rightarrow1} = 3RC + RC_L}$$

Front-End View

Cell Area	
A Input Cap	
Y Logic Function	
Y Propagation Delay	

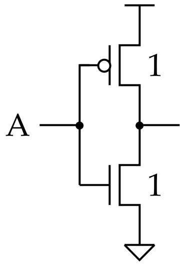
Back-End View

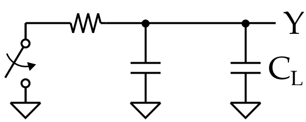
Cell Height	
Cell Width	
A Pin Location	
Y Pin Location	

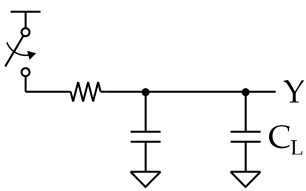
Aside: Abstract delay units

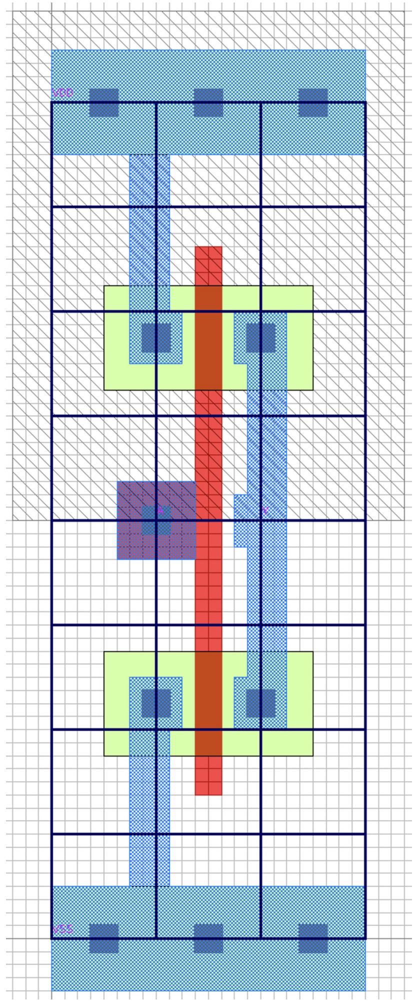
- We often want to analyze delay in "abstract delay units"
- Let τ be the propagation delay of an unloaded INVX1 standard cell
- $\tau = 3RC + RC_L = 3RC + R(0) = 3RC$

Aside: Inverter with non-equal rise and fall times

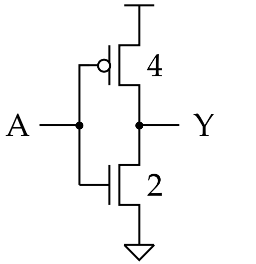


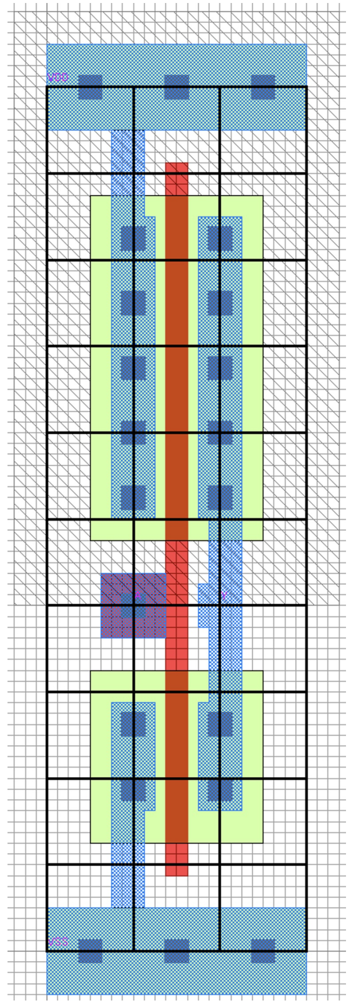


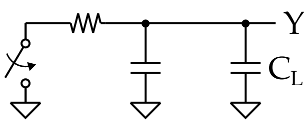


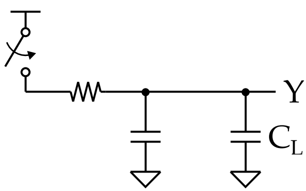


Aside: Inverter with 2× drive strength

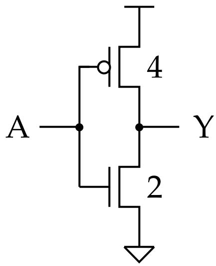


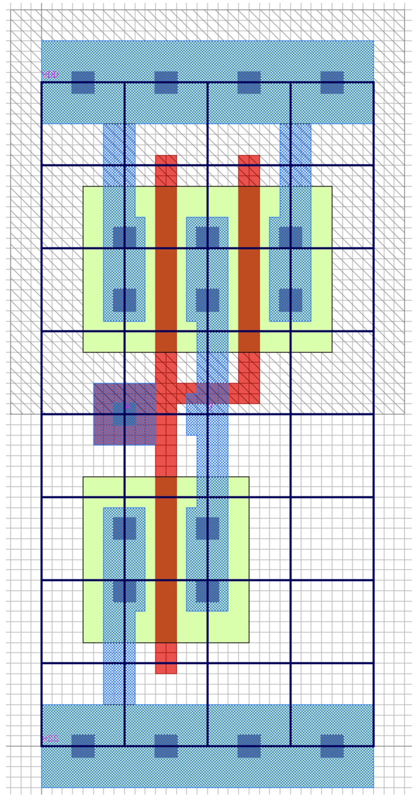


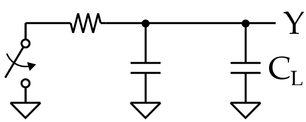


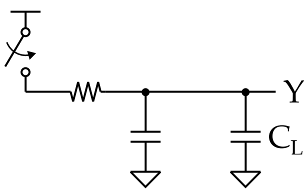


Aside: Inverter with 2× drive strength with fingers









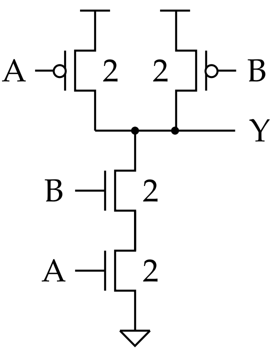
3.2. NAND2X1

Behavioral View

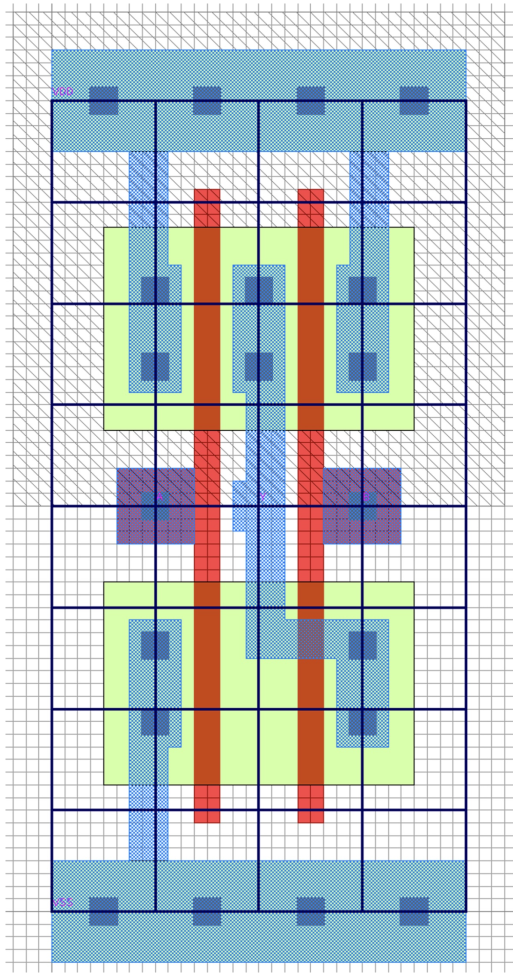
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$$Y = \overline{AB}$$

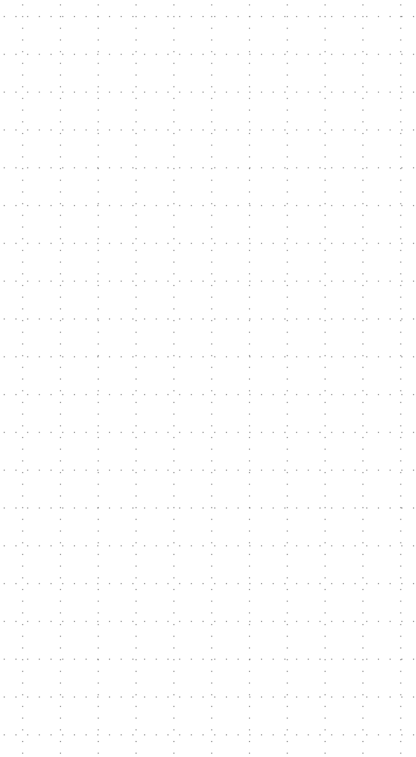
Schematic View

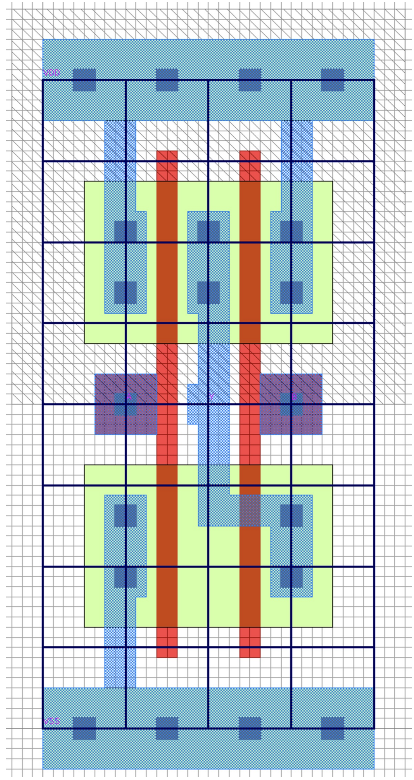


Layout View



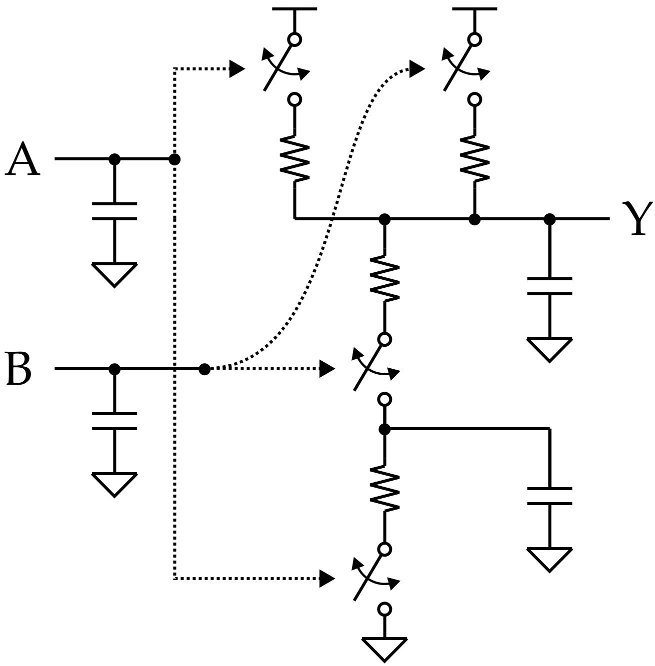
- Stick diagrams enable sketching a plan before detailed layout

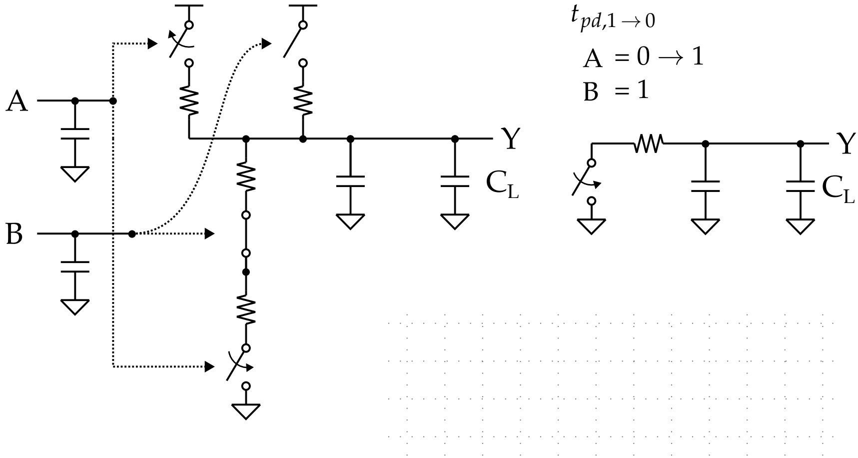


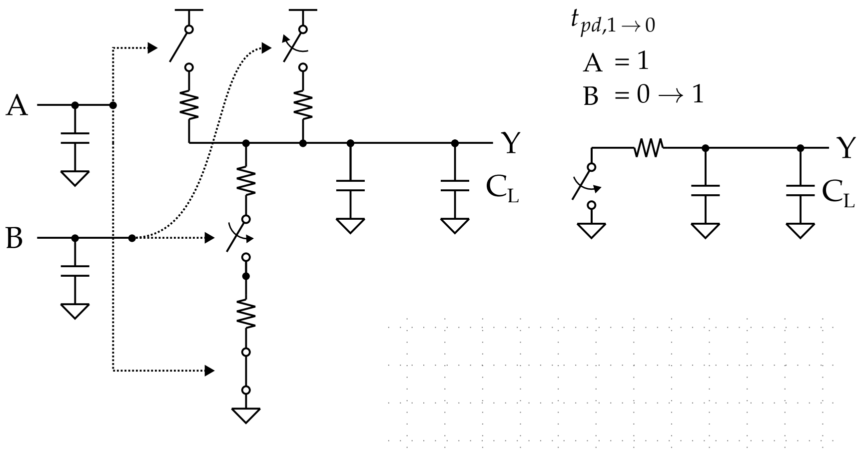


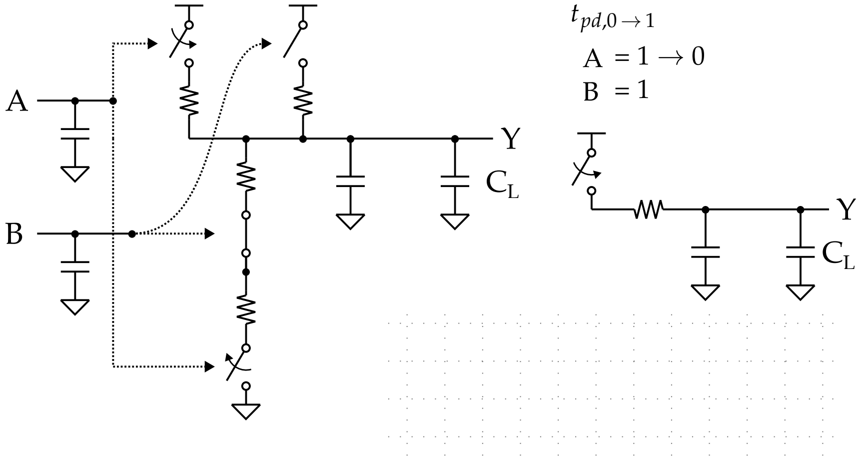
Extracted Schematic View

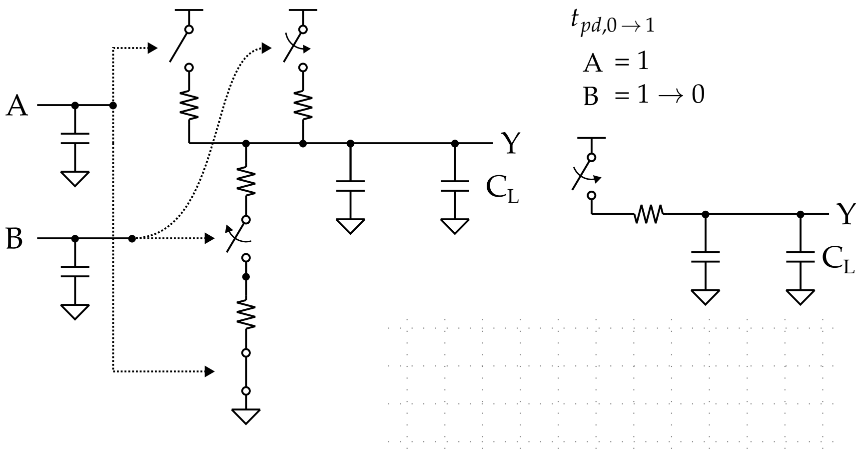
- Label the effective resistance and capacitance values to complete the extracted schematic model




$t_{pd,1\to 0}$
A = 0 → 1
B = 1
A
B
Y
C_L
Y
C_L


$t_{pd,1\to 0}$
A = 1
B = 0 → 1
A
B
Y
C_L
Y
C_L


A
B
Y
C_L
$t_{pd,0\to 1}$
A = 1 → 0
B = 1
Y
C_L


A
B
Y
C_L
$t_{pd,0\to 1}$
A = 1
B = 1 → 0
Y
C_L

Front-End View

Cell Area	
A Input Cap	
B Input Cap	
Y Logic Function	
Y Propagation Delay	

Back-End View

Cell Height	
Cell Width	
A Pin Location	
B Pin Location	
Y Pin Location	

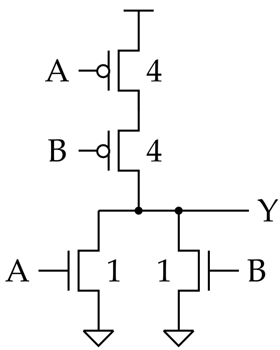
3.3. NOR2X1

Behavioral View

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$$Y = \overline{A + B}$$

Schematic View



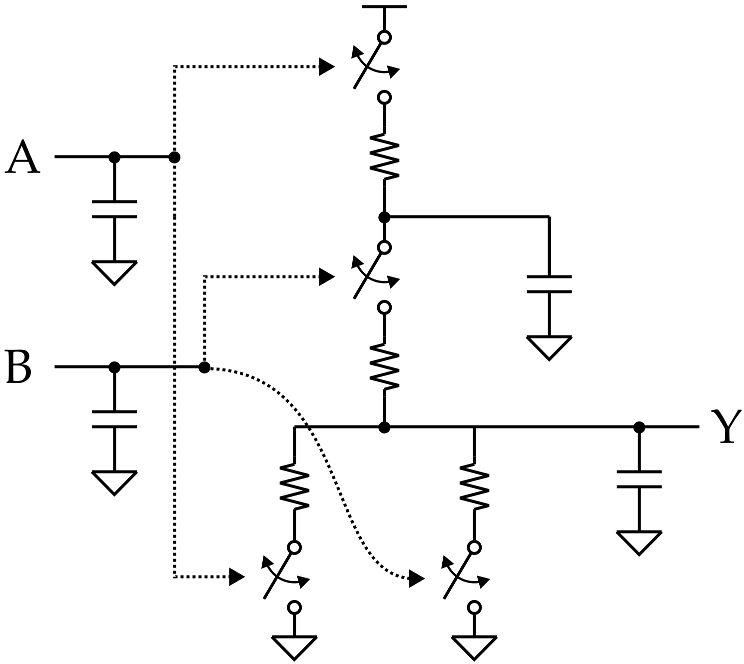
Layout View

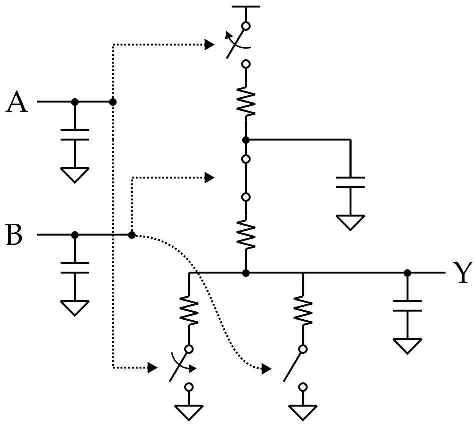
(Stick Diagram without Fingers)

(Stick Diagram with Fingers)

Extracted Schematic View

- Label the effective resistance and capacitance values to complete the extracted schematic model
  - Ignore internal capacitance
  - Assume layout-independent parasistic capacitance

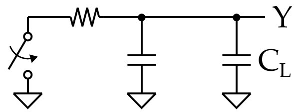


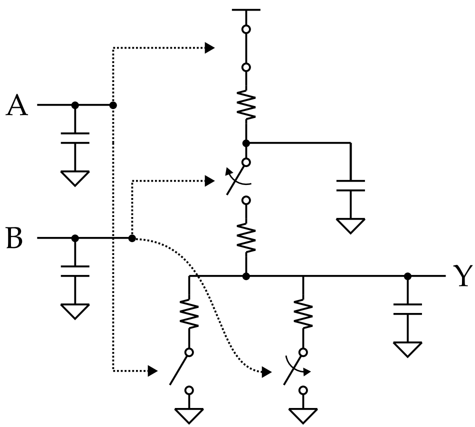


$t_{pd,1 \to 0}$

$A = 0 \to 1$

$B = 0$

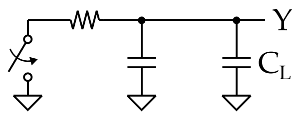


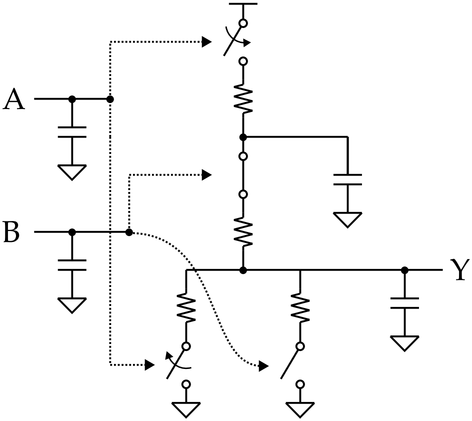


$t_{pd,1 \to 0}$

$A = 0$

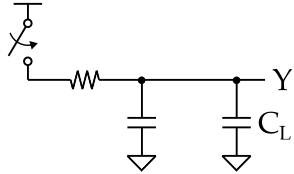
$B = 0 \to 1$

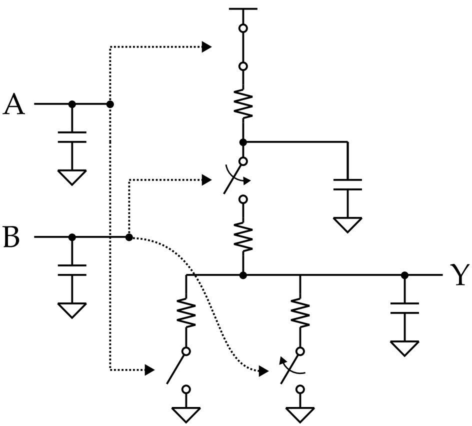




$t_{pd,0\rightarrow 1}$

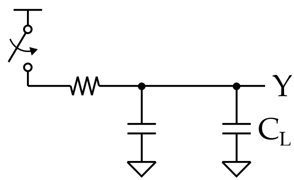
A $= 1 \rightarrow 0$
B $= 0$





$t_{pd,0\rightarrow 1}$

A $= 0$
B $= 1 \rightarrow 0$



Front-End View

Cell Area	
A Input Cap	
B Input Cap	
Y Logic Function	
Y Propagation Delay	

Back-End View

Cell Height	
Cell Width	
A Pin Location	
B Pin Location	
Y Pin Location	

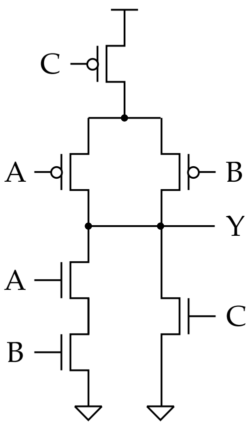
3.4. AOI21X1 *(to do on your own)*

Behavioral View

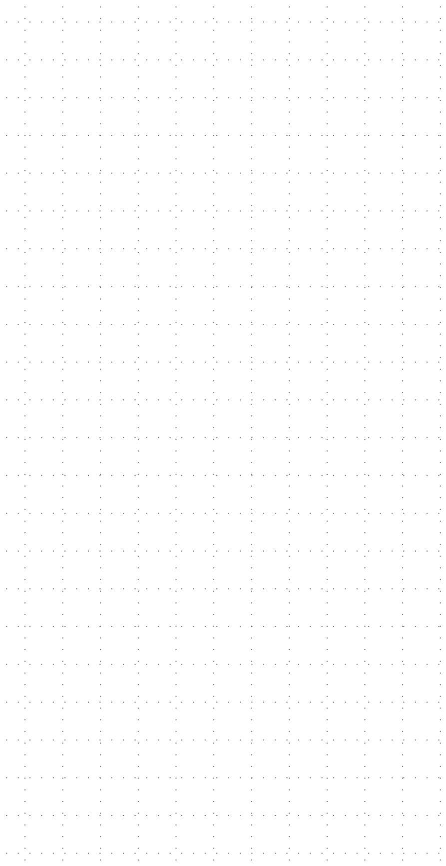
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$$Y = \overline{AB + C}$$

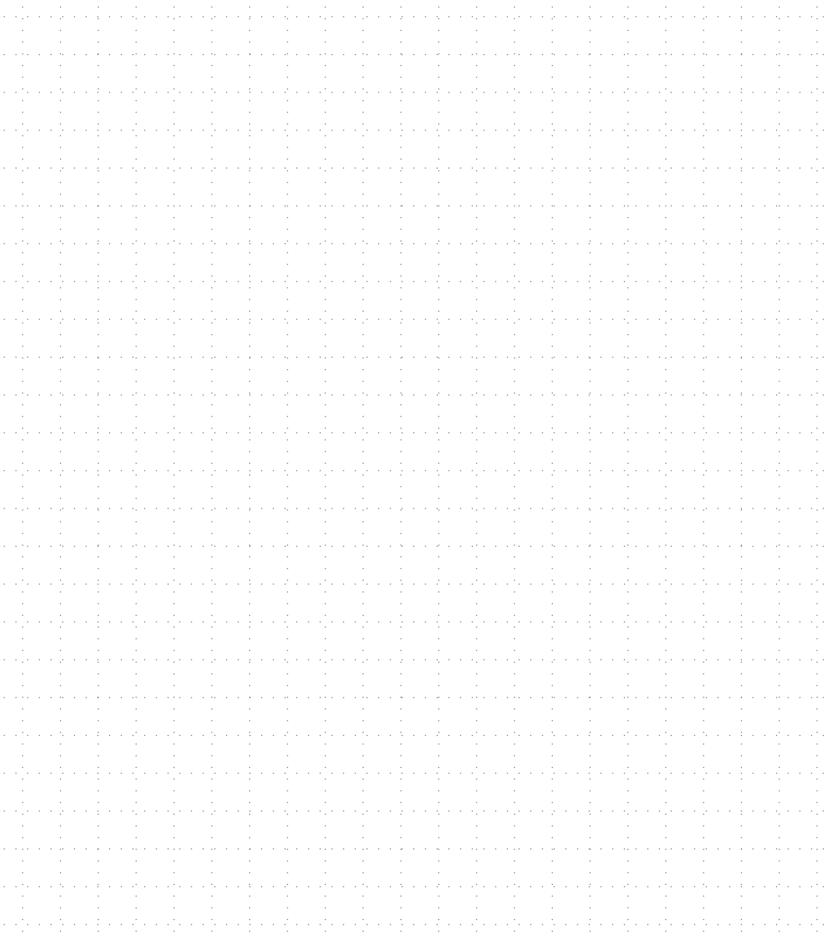
Schematic View



Layout View
(Stick Diagram)



Extracted Schematic View



Front-End View

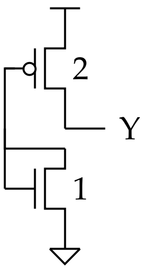
Cell Area	
A Input Cap	
B Input Cap	
C Input Cap	
Y Logic Function	
Y Propagation Delay	

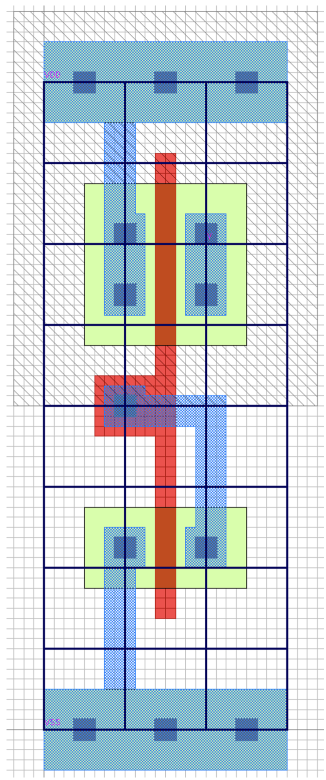
Back-End View

Cell Height	
Cell Width	
A Pin Location	
B Pin Location	
C Pin Location	
Y Pin Location	

3.5. TIEHI

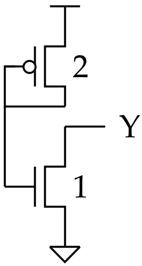
- Standard cell for connecting output to a constant logic one
- Do not directly connect a single net to the VDD supply rail
  - Power rails and signal nets can require different design rules
  - ESD on power rail can destroy fragile transistor gate
  - Power supply noise can cause signal to exceed noise margins

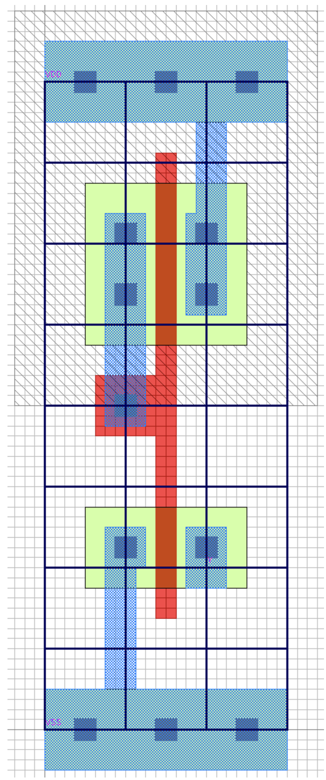




3.6. TIELO

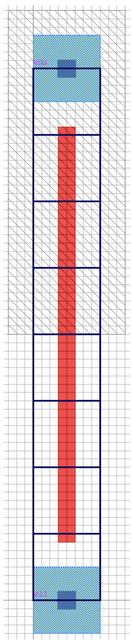
- Standard cell for connecting output to a constant logic zero
- Do not directly connect a single net to the ground rail
  - Ground rails and signal nets can require different design rules
  - ESD on ground rail can destroy fragile transistor gate
  - Ground noise can cause signal to exceed noise margins

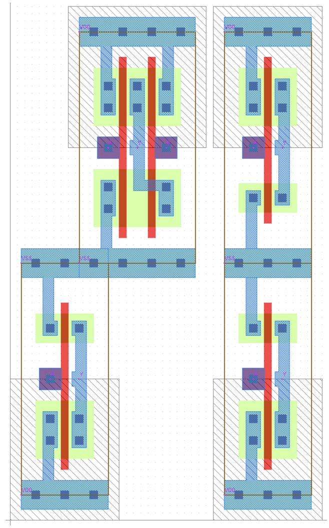


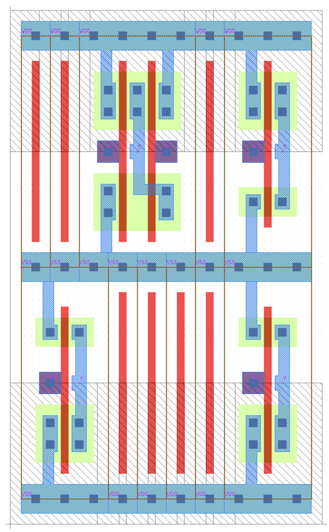


3.7. FILL

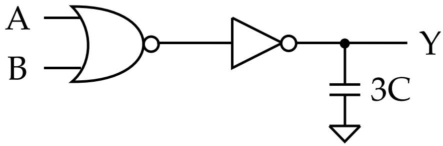
- Standard cell for filling in empty space along each row
- Needs to connect the power rail, ground rail, and n-well
- Neesd to include substrate and n-well contacts
- Needs polysilicon to satisfy polysilicon density design rules

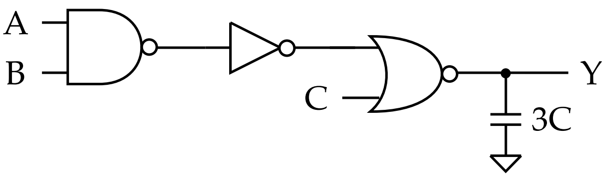






4. Gate-Level Networks





5. TinyFlow: Standard-Cell Design Flow

5.1. Files

Behavioral View	Verilog	`stdcells.v`
Schematic View	SPICE	`stdcells.sp`
Layout View	GDS	`stdcells.gds`
Extracted Schematic View	SPICE	`stdcells-rcx.sp`
Front-End View	YAML	`stdcells-fe.yml`
Back-End View	YAML	`stdcells-be.yml`

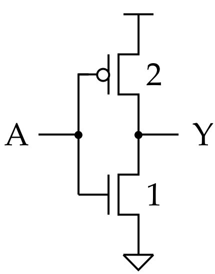
Behavioral View → Verilog

A	Y
0	1
1	0

$$Y = \overline{A}$$

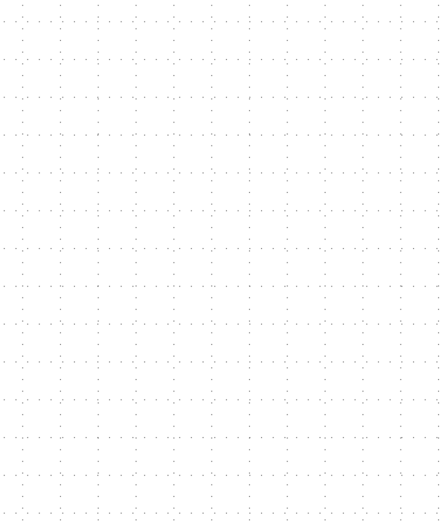
```
module INVX1
(
  input  A,
  output Y
);
  assign Y = ~A;
endmodule
```

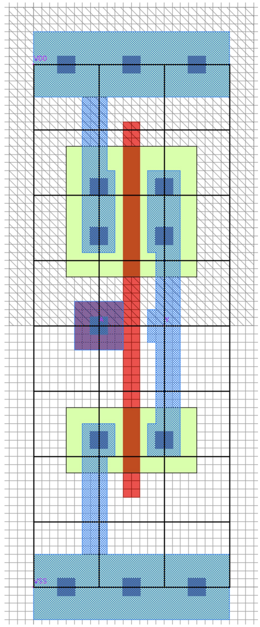
Schematic View → SPICE



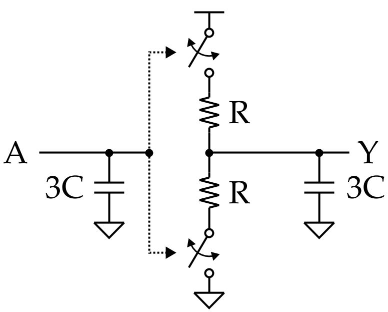

```
.SUBCKT INVX1 A Y VDD VSS

M_P Y A VDD VDD PMOS L=0.18U W=1.44U
M_N Y A VSS VSS NMOS L=0.18U W=0.72U

.ENDS INVX1
```

Layout View → GDS





Extracted Schematic View → SPICE




```
.SUBCKT INVX1 1 2 3 4

M$1 2 1 3 3 PMOS L=0.18U W=1.44U
  AS=0.9072P AD=0.9072P
  PS=4.14U PD=4.14U

M$2 2 1 4 4 NMOS L=0.18U W=0.72U
  AS=0.4536P AD=0.4536P
  PS=2.7U PD=2.7U

.ENDS INVX1
```

Front-End View → YAML

Cell Area	$1{,}536\,\lambda^2$
A Input Cap	3C
Y Logic Func	$Y = \overline{A}$
Y Prop Delay	$3RC + RC_L$

```
- name: INVX1
  area_cost: 1536 # lambda^2
  pins:

    - name: A
      type: input
      cgate: 3.6 # fF

    - name: Y
      type: output
      function: INV(A)

  parasitic_delay:   11.454 # ps
  load_delay_factor:  3.306 # ps/fF
```

Back-End View → YAML

Cell Height	$64\,\lambda$
Cell Width	$24\,\lambda$
A Pin Loc	$(8\,\lambda, 32\,\lambda)$
Y Pin Loc	$(16\,\lambda, 32\,\lambda)$

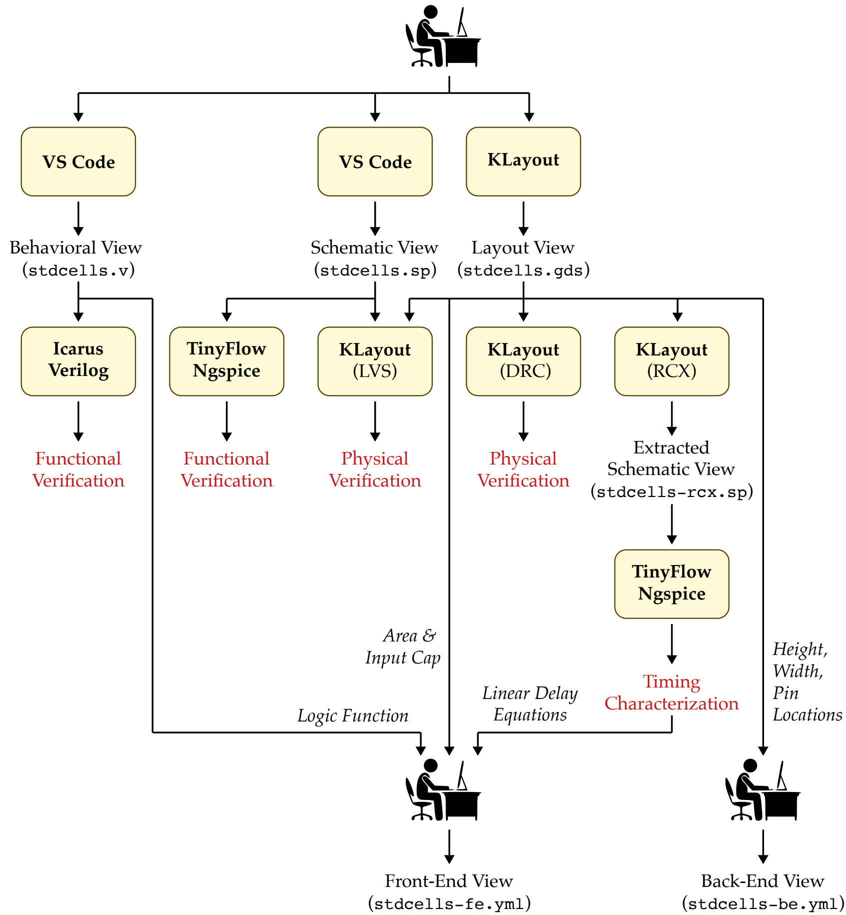
```
- name: INVX1
  size:
    width:  24
    height: 64
  pins:
    - name: A
      loc:  (8,32)
    - name: Y
      loc:  (16,32)
```

5.2. Tools

Icarus Verilog

TinyFlow-Ngspice

5.3. Flow


VS Code
VS Code
KLayout
Behavioral View
(stdcells.v)
Schematic View
(stdcells.sp)
Layout View
(stdcells.gds)
Icarus Verilog
TinyFlow Ngspice
KLayout (LVS)
KLayout (DRC)
KLayout (RCX)
Functional Verification
Functional Verification
Physical Verification
Physical Verification
Extracted Schematic View
(stdcells-rcx.sp)
TinyFlow Ngspice
Area & Input Cap
Timing Characterization
Height, Width, Pin Locations
Linear Delay Equations
Logic Function
Front-End View
(stdcells-fe.yml)
Back-End View
(stdcells-be.yml)