ECE 6745 Complex Digital ASIC Design
Topic 2: Basic Standard Cells

School of Electrical and Computer Engineering
Cornell University

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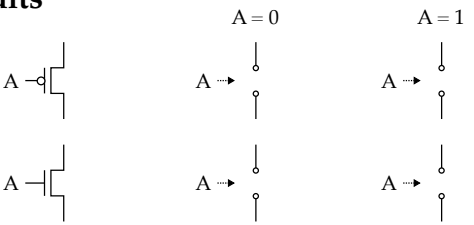
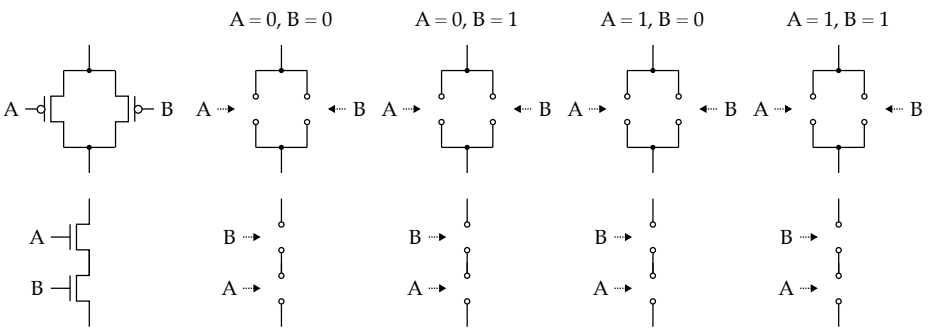
1. Static CMOS Circuits

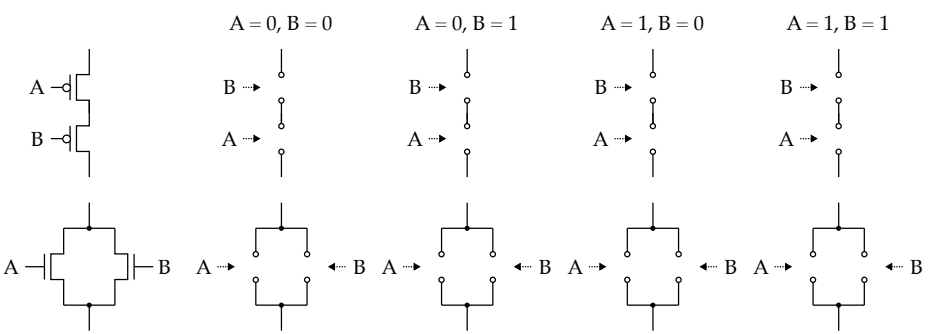
- A PMOS transistor is the complement of an NMOS transistor



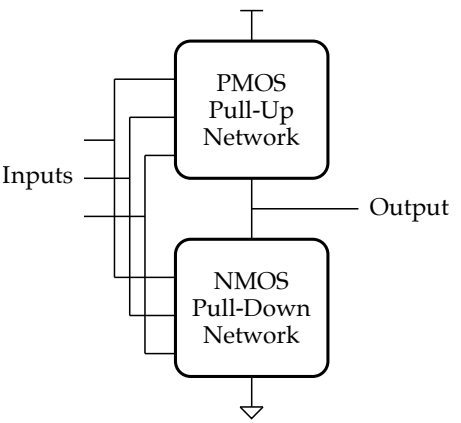
- PMOS in parallel are the complement of NMOS in series



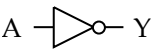
- PMOS in series are the complement of NMOS in parallel



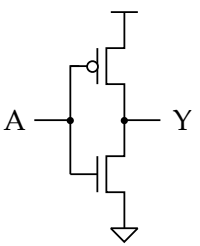
- Static CMOS circuits are divided into two parts:
  - Pull-up network exclusively uses PMOS transistors
  - Pull-down network exclusively uses NMOS transistors
- Pull-up network is the complement of the pull-down network
  - Every input is connected to exactly one PMOS and one NMOS
  - If one network is ON, the other network is OFF
  - Both networks are never ON at the same time
    (i.e., there is never a direct current path from VDD to ground)
  - Both networks are never OFF at the same time
    (i.e., the output should never be floating)



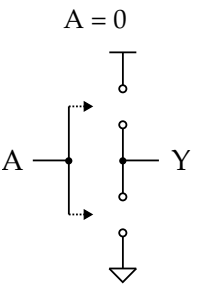
1.1. Inverter Circuit

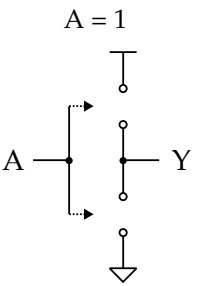


A	Y
0	1
1	0

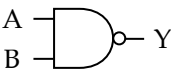


Switch-Level Model

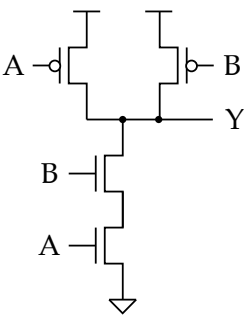




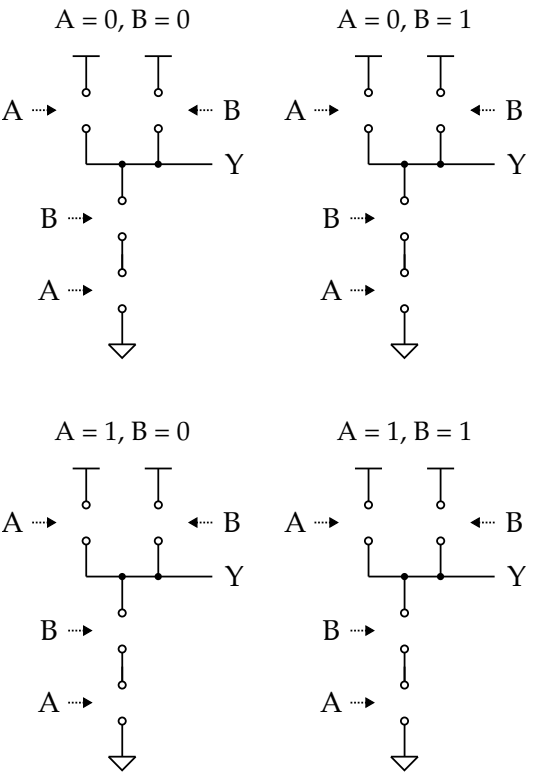
1.2. NAND2 Circuit



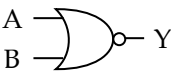
A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0



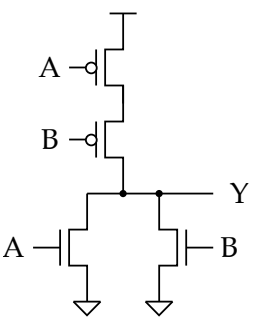
Switch-Level Model



1.3. NOR2 Circuit

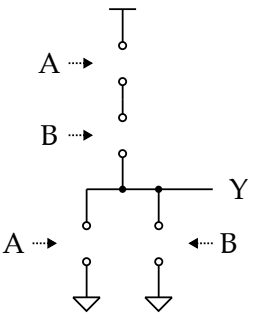


A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	0

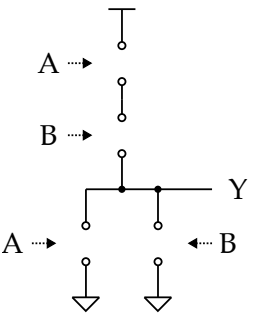


Switch-Level Model

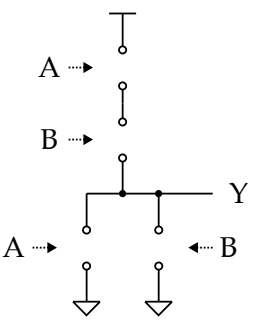
A = 0, B = 0



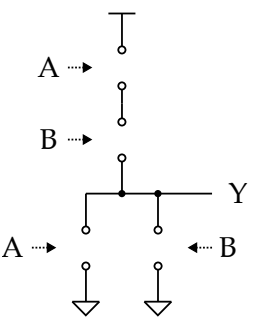
A = 0, B = 1



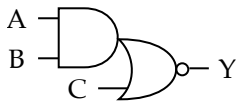
A = 1, B = 0



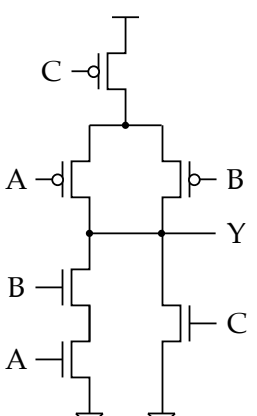
A = 1, B = 1



1.4. AOI21 Circuit

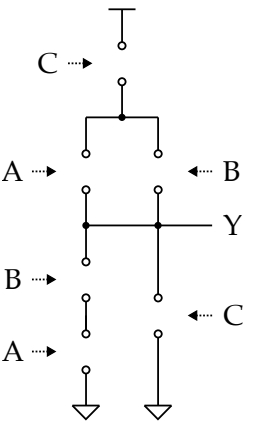


A	*B*	*C*	*Y*
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

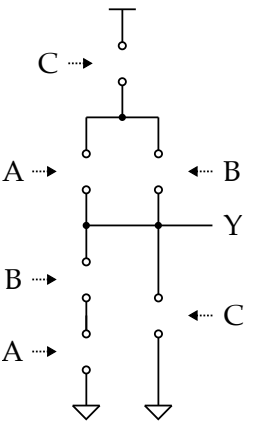


Switch-Level Model

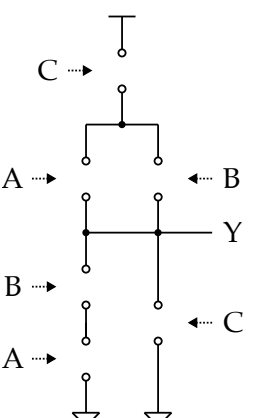
A = 0, B = 0, C = 0



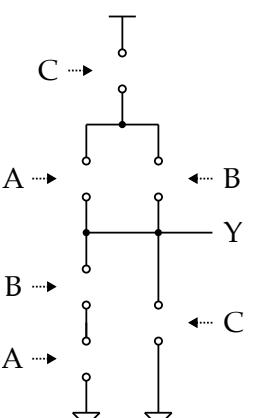
A = 0, B = 1, C = 0



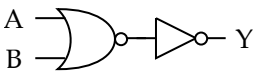
A = 1, B = 1, C = 0



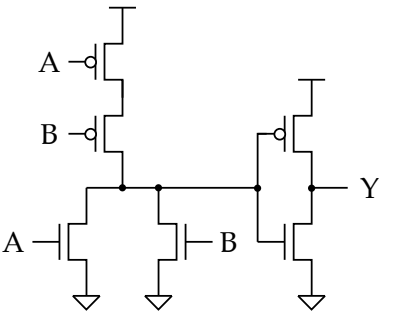
A = 1, B = 1, C = 1



1.5. Multi-Stage Circuits

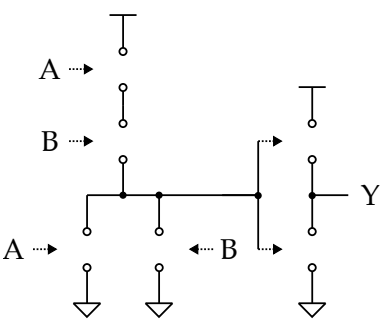


A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

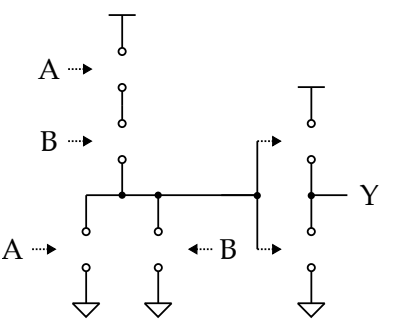


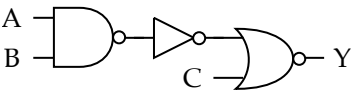
Switch-Level Model

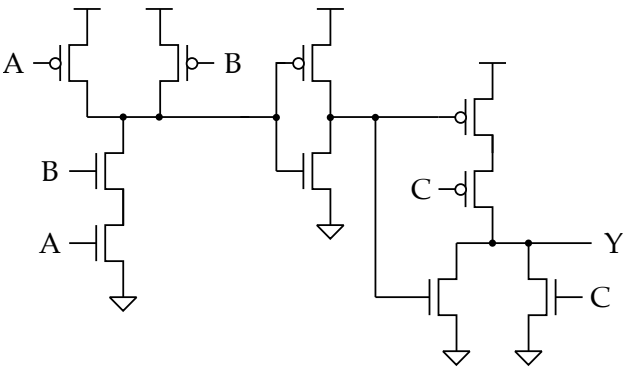
A = 0, B = 0



A = 0, B = 1

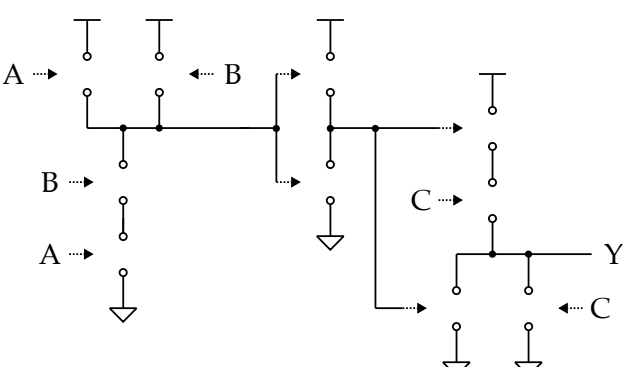




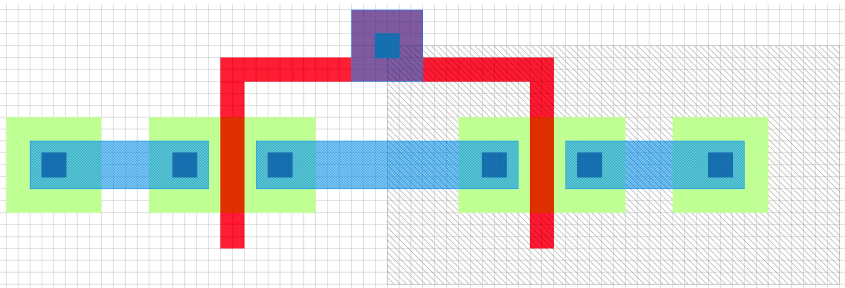


Switch-Level Model

A = 1, B = 1, C = 0

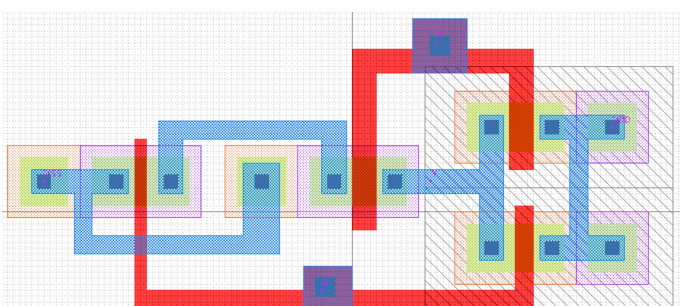


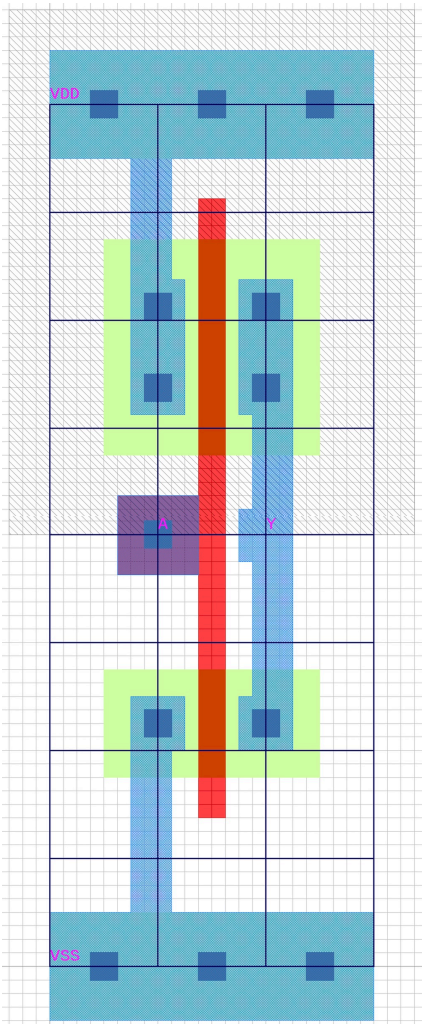
2. Full-Custom vs. Standard Cell Design



2.1. Full-Custom Design

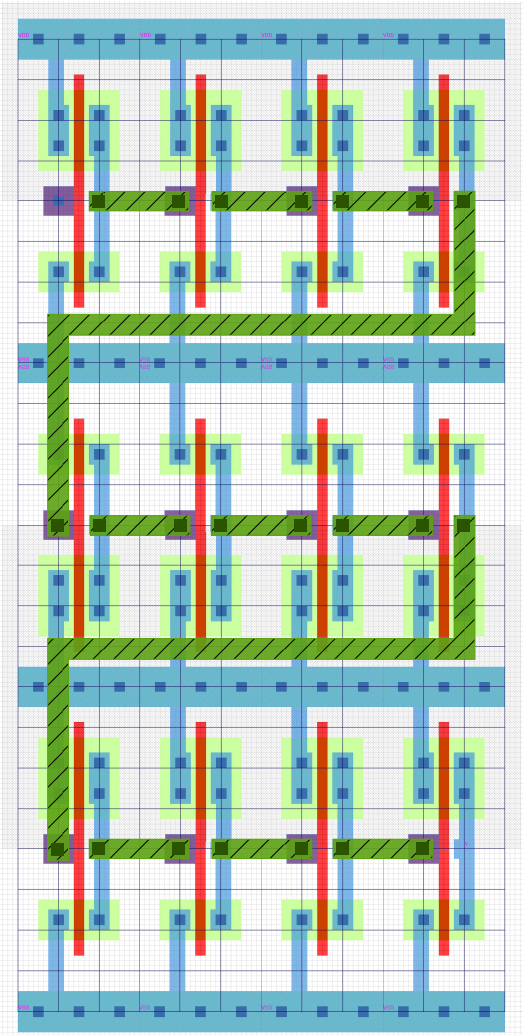
- Transistors can be in any position and any orientation
- N-well can be any size and in any location
- VDD and ground can use any metal layer and any location
- Substrate and n-well contacts can be in any location
- Metal 2+ routing is unconstrained
- Cells can be any height and any width
- Pins can be on any layer and in any location
- Cells can have any drive strengths with non-equal rise and fall times





2.2. Standard-Cell Design

- Standard transistor positions and orientation (PMOS at top, NMOS at bottom, vertical gates)
- Standard n-well size and location (n-well at top)
- Standard VDD and ground metal layer and locations (on metal 1, VDD rail 8λ tall at top, ground rail 8λ tall at bottom)
- Standard n-well and substrate contacts
- Standard boundry and extension of n-well, VDD, and ground rails beyond boundry (origin is in lower left)
- Standard metal 2+ routing grid (8λ track spacing)
- Standard cell height (64λ)
- Standard cell width (aligned to routing grid, i.e., 8λ, 16λ, 24λ, etc)
- Standard pin layer and locations (on metal 1 and on routing grid)
- Standard set of available drive strengths



- Standard cells are designed to be abutted in rows
  - n-wells align
  - VDD rails align
  - Ground rails align
  - N-well contacts align
  - Substrate contacts align
- Each row is flipped vertically with respect to previous row
  - Enables sharing VDD and ground rails
- Standard-cell design rules ensure composing standard cells will not create any DRC violations
- Metal 2+ always routed on the routing grid

2.3. Standard-Cell Views

Behavioral View	Logical function of the standard cell, used for gate-level simulation
Schematic View	Transistor-level representation of standard cell, used for functional verification and layout-vs-schematic (LVS)
Layout View	Layout of standard cell, used for design-rule checking (DRC), layout-vs-schematic (LVS), resistance/capacitance extraction (RCX), and fabrication
Extracted Schematic View	Transistor-level representation with extracted resistance and capacitances, used for layout-vs-schematic (LVS) and timing characterization
Front-End View	High-level information about standard cell including area, input capacitance, logical function, and delay model; used in synthesis
Back-End View	Low-level information about standard cell including height, width, and pin locations; used in placement and routing

3. Standard Cells

- We will initially focus on the following seven basic standard cells
  - INVX1 : NOT gate (inverter)
  - NAND2X1 : 2-input NAND gate
  - NOR2X1 : 2-input NOR gate
  - AOI21X1 : 3-input AND-OR-Inverting gate
  - TIEHI : Tie output to logic one
  - TIELO : Tie output to logic zero
  - FILL : Filler cell
- X1 suffix means these standard cells all have the same drive strength (i.e., approximately the same effective resistance)
- We will later discuss more advanced standard cells
  - More complex combinational logic cells
  - Sequential logic cells (i.e., flip-flops)
  - Cells with larger drive stengths

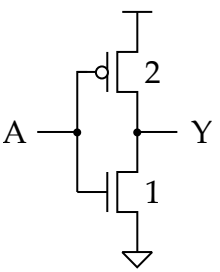
3.1. INVX1

Behavioral View

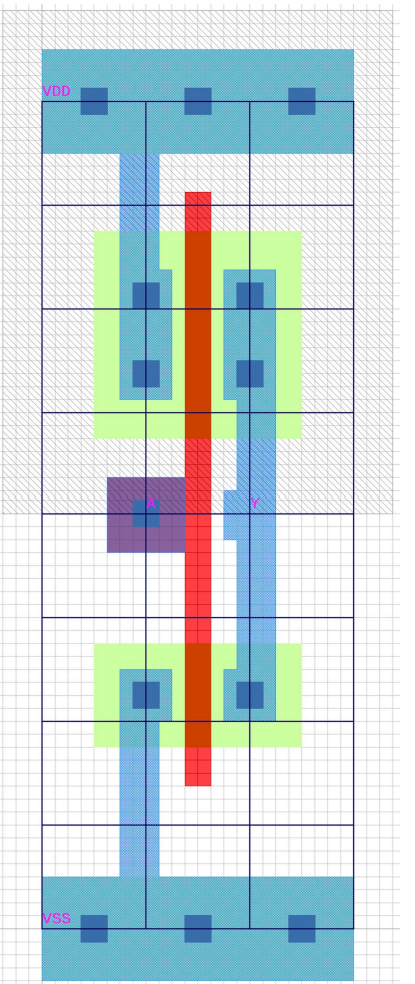
A	Y
0	1
1	0

$$Y = \overline{A}$$

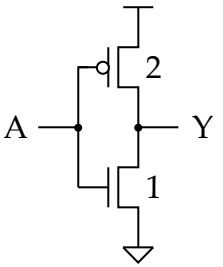
Schematic View

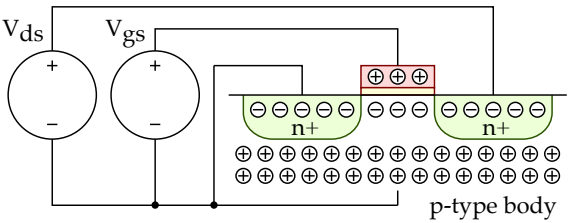


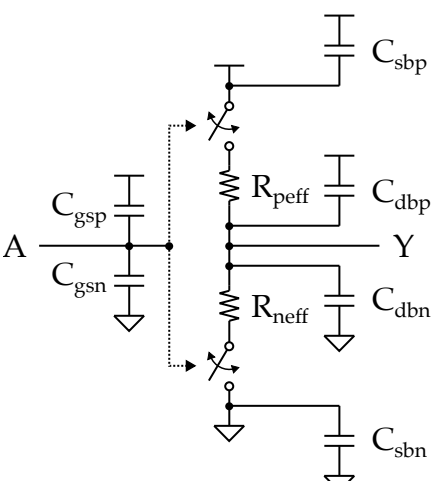
Layout View



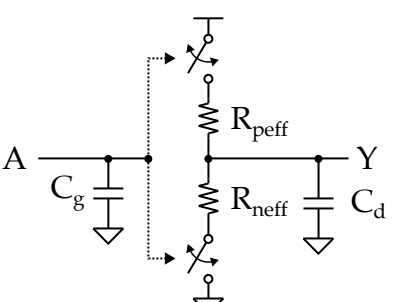
Extracted Schematic View



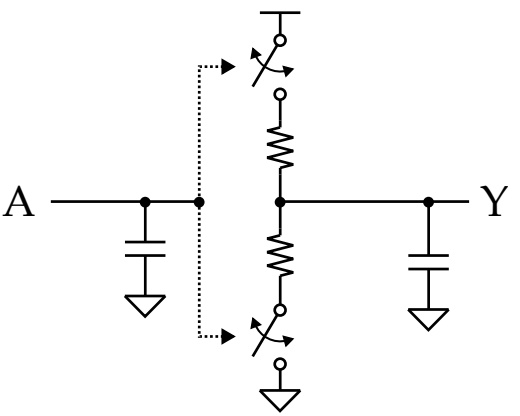


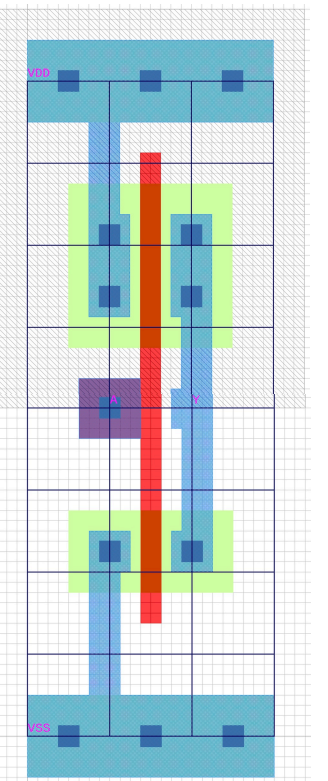


- C_{sb} capacitors do not actually switch, so ignore
- C_d and C_g capacitors tied to constant voltage sources so lump together



- Let R be the effective resistance of a minimum-sized NMOS
- Let C be the gate capacitance of a minimum-sized NMOS
- Let C be the diffusion capacitance of a minimum-sized NMOS
- Recall $R_{peff} = 2 \times R_{neff}$ for same transistor width





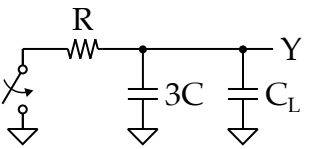
Front-End View

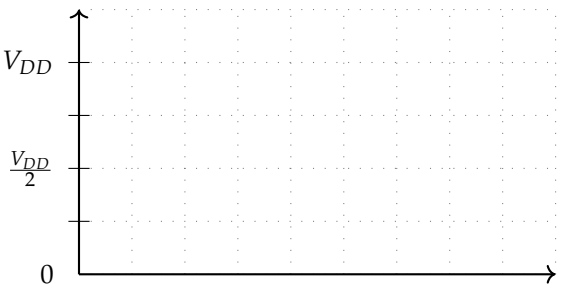
Cell Area
A Input Cap
Y Logic Function
Y Propagation Delay

Back-End View

Cell Height
Cell Width
A Pin Location
Y Pin Location

$t_{pd,1\to0}$
A $= 0 \to 1$





- Let t_{pd} be the time until $V_Y = V_{DD}/2$ (propagation delay)
- Let $\tau = R(3C + C_L) = 3RC + RC_L$ (time constant)

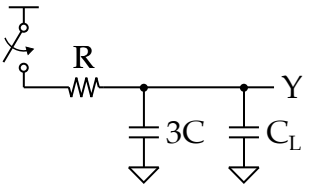
$$V_Y = V_{DD}\, e^{-t/\tau}$$
$$\frac{V_{DD}}{2} = V_{DD}\, e^{-t/\tau}$$
$$\frac{1}{V_{DD}}\frac{V_{DD}}{2} = e^{-t/\tau}$$
$$\ln\left(\frac{1}{2}\right) = \frac{-t}{\tau}$$
$$-\tau \ln\left(\frac{1}{2}\right) = t$$
$$t = \tau \ln(2)$$

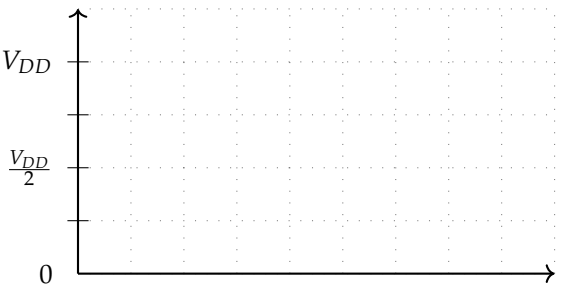
- $t_{pd,1\to0} = (3RC + RC_L) \cdot \ln(2)$
- We usually just assume effective resistance is scaled by ln(2)

$$\boxed{t_{pd,1\to0} = 3RC + RC_L}$$

$t_{pd,0\to1}$

A $= 1 \to 0$





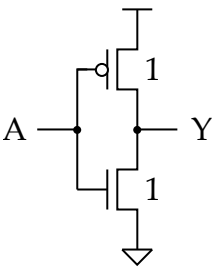
- Let t_{pd} be the time until $V_Y = V_{DD}/2$ (propagation delay)
- Let $\tau = R(3C + C_L) = 3RC + RC_L$ (time constant)

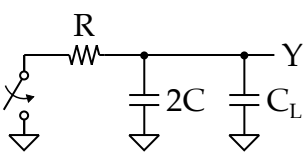
$$V_Y = V_{DD} \cdot (1 - e^{-t/\tau})$$
$$\frac{V_{DD}}{2} = V_{DD} \cdot (1 - e^{-t/\tau})$$
$$\frac{1}{V_{DD}} \frac{V_{DD}}{2} = 1 - e^{-t/\tau}$$
$$\ln\left(\frac{1}{2}\right) = \frac{-t}{\tau}$$
$$-\tau \ln\left(\frac{1}{2}\right) = t$$
$$t = \tau \ln(2)$$

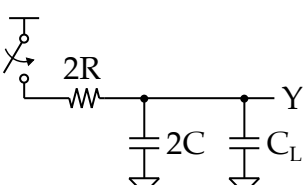
- $t_{pd,0\to1} = (3RC + RC_L) \cdot \ln(2)$
- We usually just assume effective resistance is scaled by ln(2)

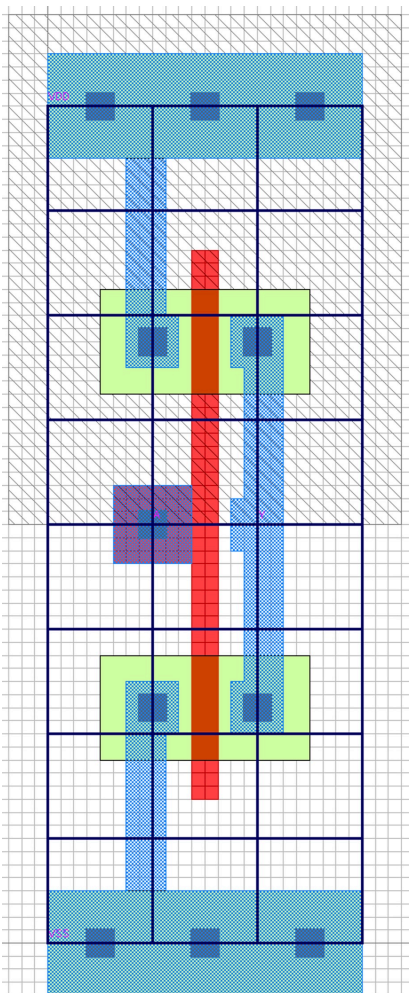
$$\boxed{t_{pd,0\to1} = 3RC + RC_L}$$

Aside: Inverter with non-equal rise and fall times

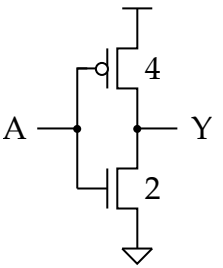


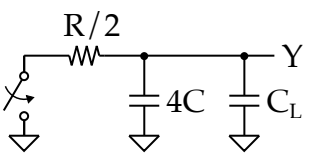


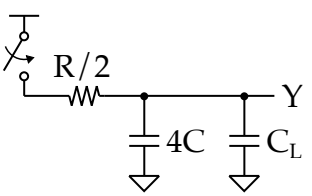


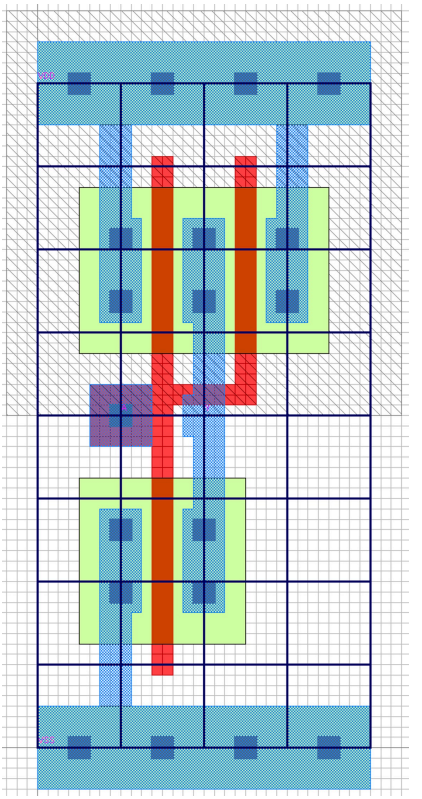


Aside: Inverter with twice the drive strength (INVX2)









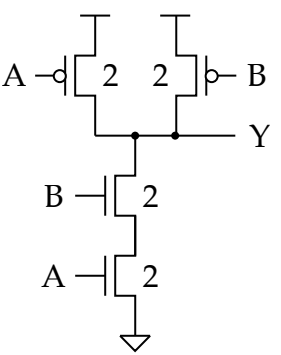
3.2. NAND2X1

Behavioral View

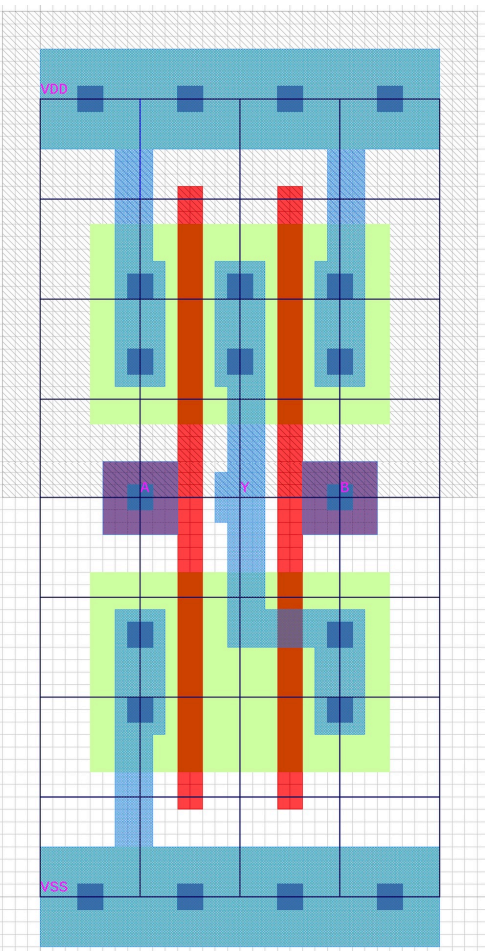
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$$Y = \overline{AB}$$

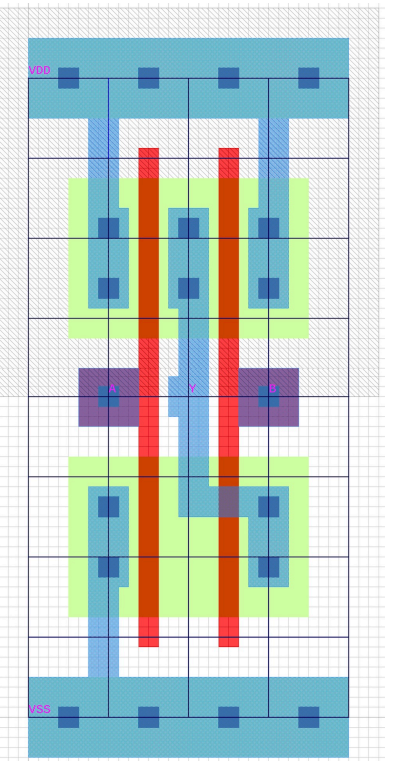
Schematic View



Layout View

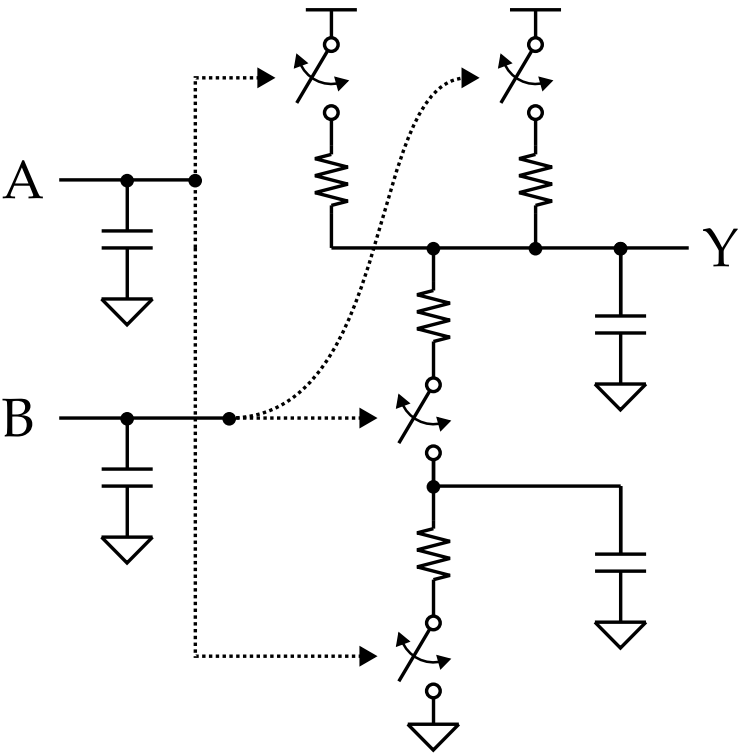


- Stick diagrams enable sketching a plan before detailed layout



Extracted Schematic View

- Label the effective resistance and capacitance values to complete the extracted schematic model



Front-End View

Cell Area
A Input Cap
B Input Cap
Y Logic Function
Y Propagation Delay

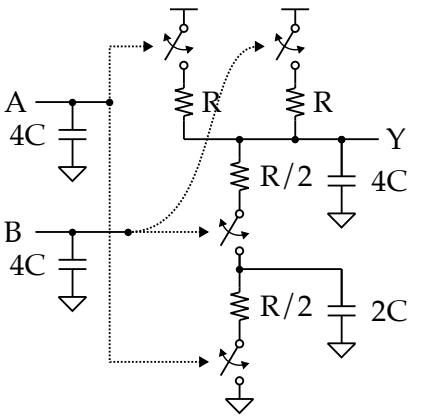
Back-End View

Cell Height
Cell Width
A Pin Location
B Pin Location
Y Pin Location

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

List all possible input conditions

A	B	Y
0	$0 \rightarrow 1$	
0	$1 \rightarrow 0$	
1	$0 \rightarrow 1$	
1	$1 \rightarrow 0$	
$0 \rightarrow 1$	0	
$1 \rightarrow 0$	0	
$0 \rightarrow 1$	1	
$1 \rightarrow 0$	1	

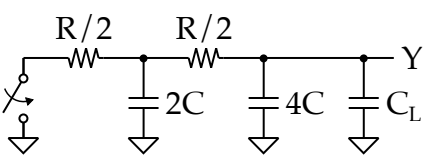


- Estimate propagation delay for all input conditions which result in an output transition

$t_{pd,1 \rightarrow 0}$

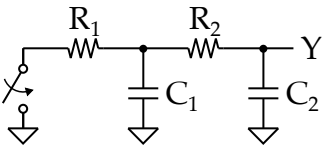
A $= 0 \rightarrow 1$

B $= 1$



Aside: Elmore's Delay

- Consider the following general RC circuit



- Requires complicated second-order model

$$V_Y(t) = V_{DD}\frac{\tau_1 e^{-t/\tau_1} - \tau_2 e^{-t/\tau_2}}{\tau_1 - \tau_2}$$

$$R^* = \frac{R_2}{R_1} \qquad C^* = \frac{C_2}{C_1}$$

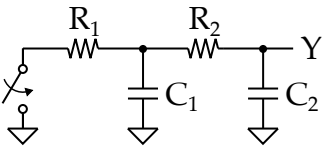
$$\tau_{1,2} = \frac{R_1C_1 + (R_1 + R_2)C_2}{2}\left(1 \pm \sqrt{1 - \frac{4R^*C^*}{[1 + (1 + R^*)C^*]^2}}\right)$$

- We do not want to determine the exact waveform for V_Y
- So we can use Elmore's delay to estimate the propagation delay
- Approximate this second-order model with a first-order model that preserves the propagation delay but not the full waveform shape

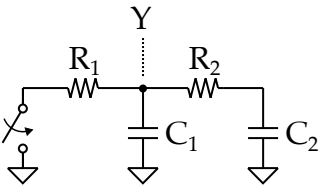
$$V_Y = V_{DD}\, e^{-t/\tau}$$

$$\tau = R_1C_1 + (R_1 + R_2)C_2$$

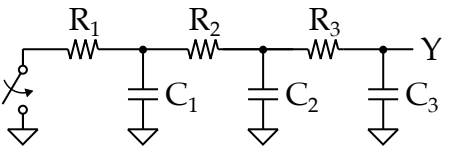
- Each capacitor contributes delay proportional to the resistance between it and the input
- Only useful for estimating propagation delay
- Best when one τ is much larger than the other τ
- Even if $\tau_1 = \tau_2$, error is $< 15\%$



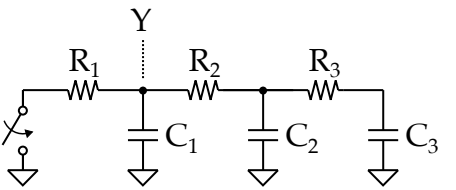
$$t_{pd} = R_1C_1 + (R_1 + R_2)C_2$$



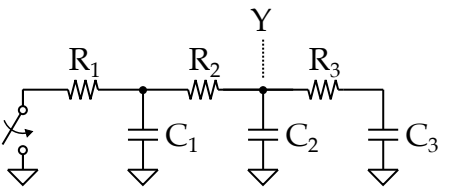
$$t_{pd} = R_1C_1 + R_1C_2$$



$$t_{pd} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3$$



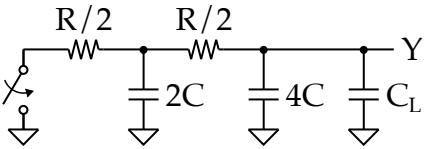
$$t_{pd} = R_1C_1 + R_1C_2 + R_1C_3$$



$$t_{pd} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2)C_3$$

Use Elmore's delay to estimate propagation delay of NAND2X1

$t_{pd,1\to0}$
A $= 0 \to 1$
B $= 1$



$$t_{pd,1\to0} = \frac{R}{2}(2C) + (\frac{R}{2} + \frac{R}{2})(4C + C_L)$$
$$= RC + R(4C + C_L) = 5RC + RC_L$$

$t_{pd,1\to0}$
A $= 1$
B $= 0 \to 1$

$t_{pd,0\to1}$
A $= 1$
B $= 1 \to 0$

$t_{pd,0\to1}$
A $= 1 \to 0$
B $= 1$

Aside: Delay Models

- Value-, Path-, and Load-Dependent Linear Delay Model

A	B	Y
1	$0 \to 1$	$t_{pd,1\to 0} = 4RC + RC_L$
1	$1 \to 0$	$t_{pd,0\to 1} = 4RC + RC_L$
$0 \to 1$	1	$t_{pd,1\to 0} = 5RC + RC_L$
$1 \to 0$	1	$t_{pd,0\to 1} = 6RC + RC_L$

- Path- and Load-Dependent Linear Delay Model

$$t_{pd,B\to Y} = 4RC + RC_L$$
$$t_{pd,A\to Y} = 6RC + RC_L$$

- Load-Dependent Linear Delay Model

$$t_{pd} = 6RC + RC_L$$

- Constant Delay Model

$$t_{pd} = 6RC + R(3C) = 9RC$$

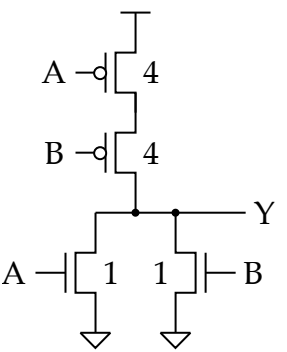
3.3. NOR2X1

Behavioral View

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$$Y = \overline{A + B}$$

Schematic View



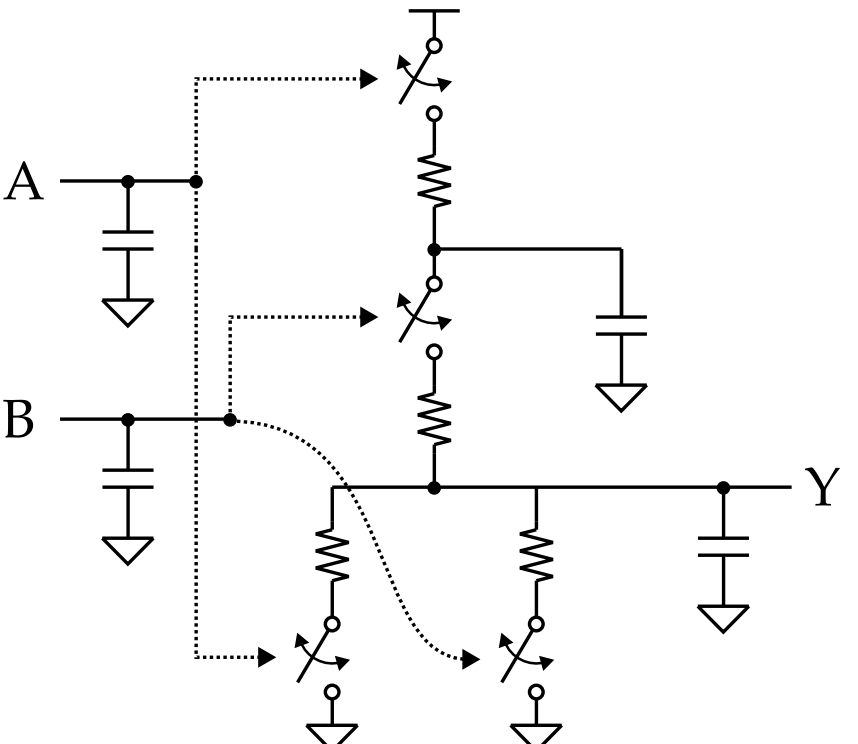
Layout View

(Stick Diagram without Fingers)

(Stick Diagram with Fingers)

Extracted Schematic View

- Label the effective resistance and capacitance values to complete the extracted schematic model
- Assume using fingers for equal rise and fall times



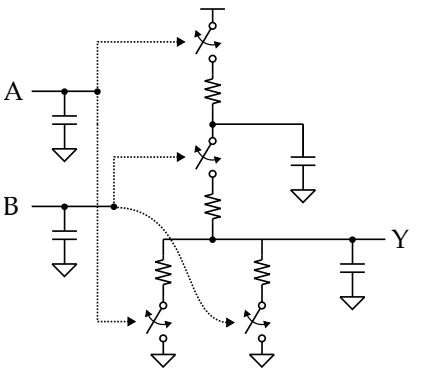
Front-End View

Cell Area
A Input Cap
B Input Cap
Y Logic Function
Y Propagation Delay

Back-End View

Cell Height
Cell Width
A Pin Location
B Pin Location
Y Pin Location

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



List all possible input conditions

A	B	Y
0	$0 \rightarrow 1$	
0	$1 \rightarrow 0$	
1	$0 \rightarrow 1$	
1	$1 \rightarrow 0$	
$0 \rightarrow 1$	0	
$1 \rightarrow 0$	0	
$0 \rightarrow 1$	1	
$1 \rightarrow 0$	1	

Use Elmore's delay to estimate propagation delay of NOR2X1

$t_{pd,1\to0}$

A $= 0$

B $= 0 \to 1$

$t_{pd,0\to1}$

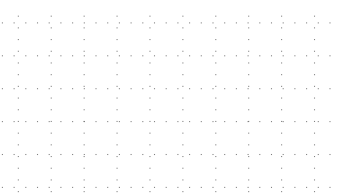
A $= 0$

B $= 1 \to 0$

$t_{pd,1\to1}$

A $= 0 \to 1$

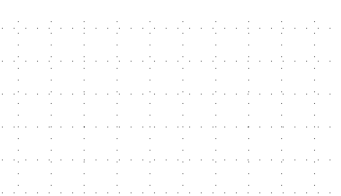
B $= 0$



$t_{pd,0\to1}$

A $= 1 \to 0$

B $= 0$



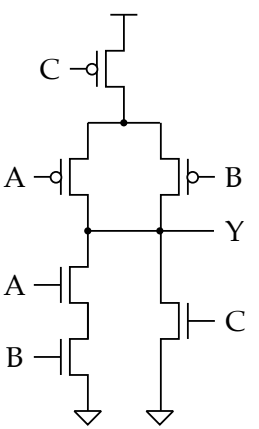
3.4. AOI21X1

Behavioral View

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

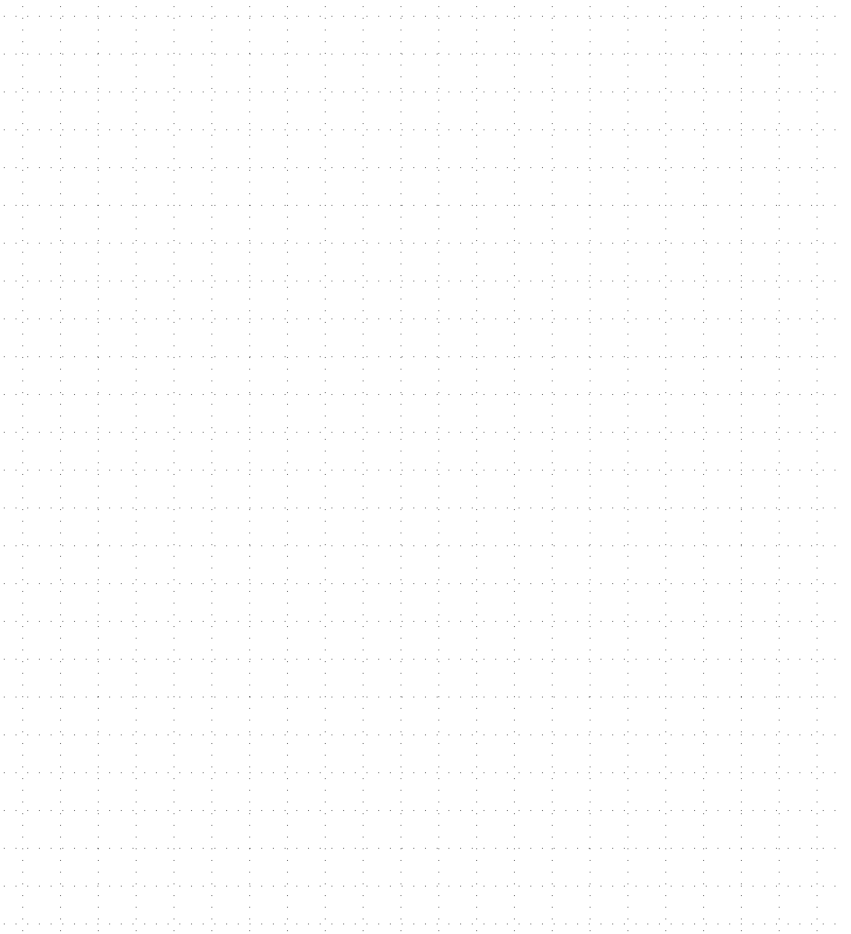
$$Y = \overline{AB + C}$$

Schematic View



Layout View
(Stick Diagram)

Extracted Schematic View



Front-End View

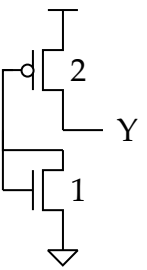
Cell Area
A Input Cap
B Input Cap
C Input Cap
Y Logic Function
Y Propagation Delay

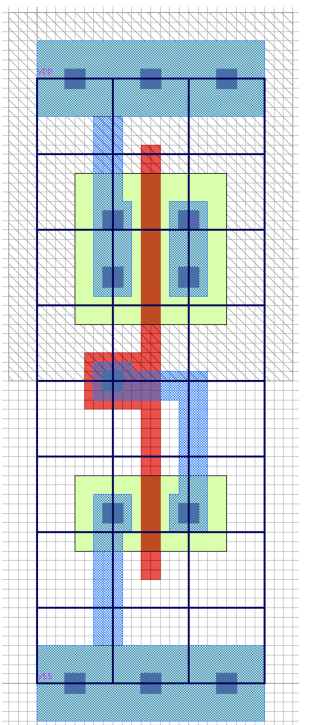
Back-End View

Cell Height
Cell Width
A Pin Location
B Pin Location
C Pin Location
Y Pin Location

3.5. TIEHI

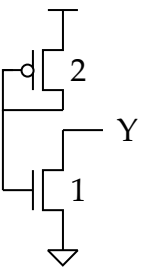
- Standard cell for connecting output to a constant logic one
- Do not directly connect a single net to the VDD supply rail
  - Power rails and signal nets can require different design rules
  - ESD on power rail can destroy fragile transistor gate
  - Power supply noise can cause signal to exceed noise margins
  - ... among other reasons ...

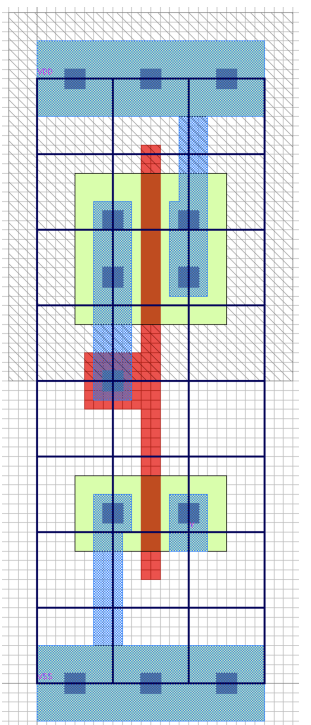




3.6. TIELO

- Standard cell for connecting output to a constant logic zero
- Do not directly connect a single net to the ground rail
  - Ground rails and signal nets can require different design rules
  - ESD on ground rail can destroy fragile transistor gate
  - Ground noise can cause signal to exceed noise margins
  - ... among other reasons ...





3.7. FILL

- Standard cell for “filling in empty space”
- Needs to connect the power rail, ground rail, and n-well
- Needs poly to satisfy poly density design rules