ECE 6745 Complex Digital ASIC Design
Topic 1: Basic CMOS Devices

School of Electrical and Computer Engineering
Cornell University

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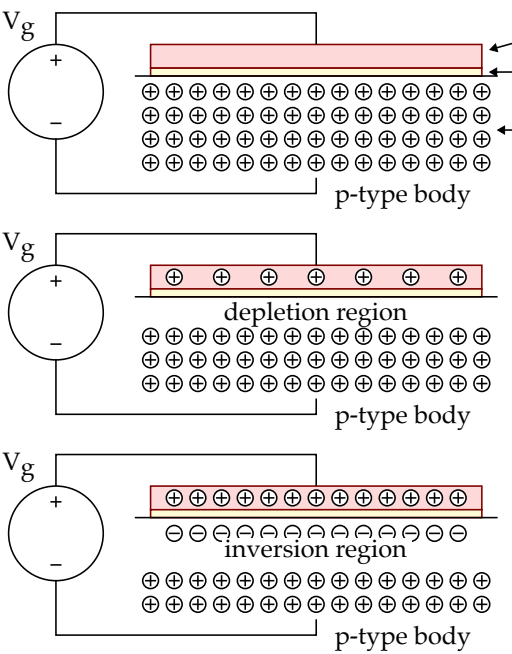
1. Transistors

- Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are the fundamnetal building block of every ASIC chip
- We will take an incremental approach:
  - Metal-Oxide-Semiconductor (MOS) Structure
  - NMOS Transistors
  - RC Model for an NMOS Transistor
  - PMOS Transistors

1.1. "Metal"-Oxide-Semiconductor Structure



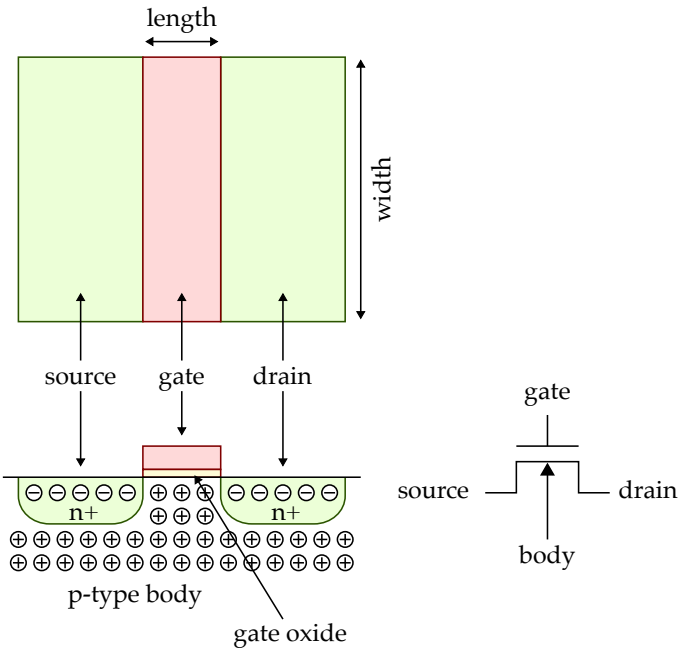
Depletion Mode

$V_g < V_t$ results in positive charge on the gate which repels holes in the p-type body

Inversion Mode

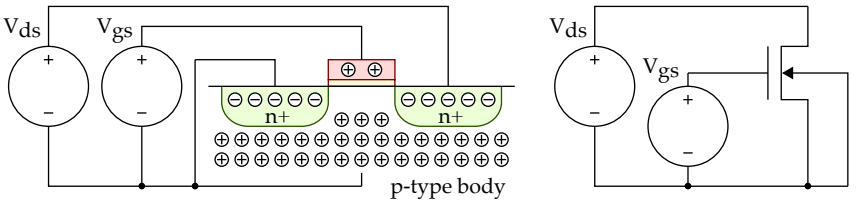
$V_g > V_t$ results in more positive charge on the gate which repels holes further and attracts free electrons (generated from thermal excitation)

1.2. NMOS Transistor

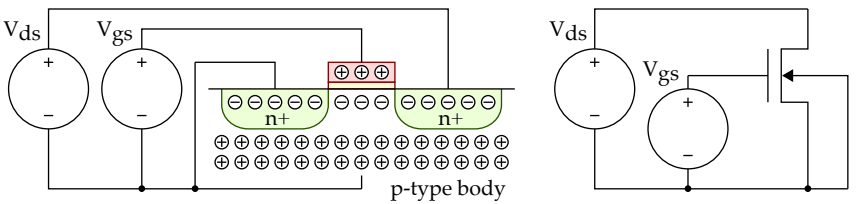


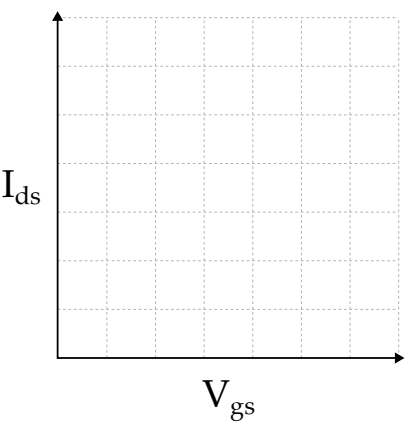
- An NMOS transistor uses n-type doped silicon to create a *source* and *drain* next to a MOS structure with a p-type body
- The voltage on the gate controls the inversion region which can create a *channel of electrons* between the source and drain
  - When the MOS structure is in *depletion mode*, the transistor is *off* and no current flows through the channel
  - When the MOS structure is in *inversion mode*, the transistor is *on* and current flows through the channel

NMOS Off when $0 < V_{gs} < V_t$

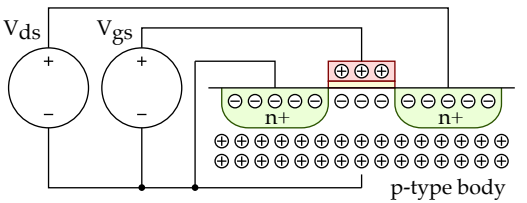


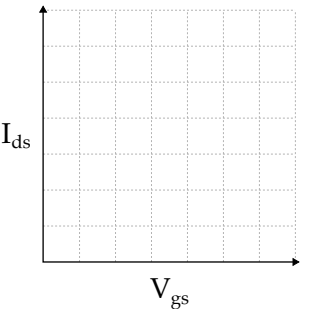
NMOS On when $V_t < V_{gs} < V_{DD}$



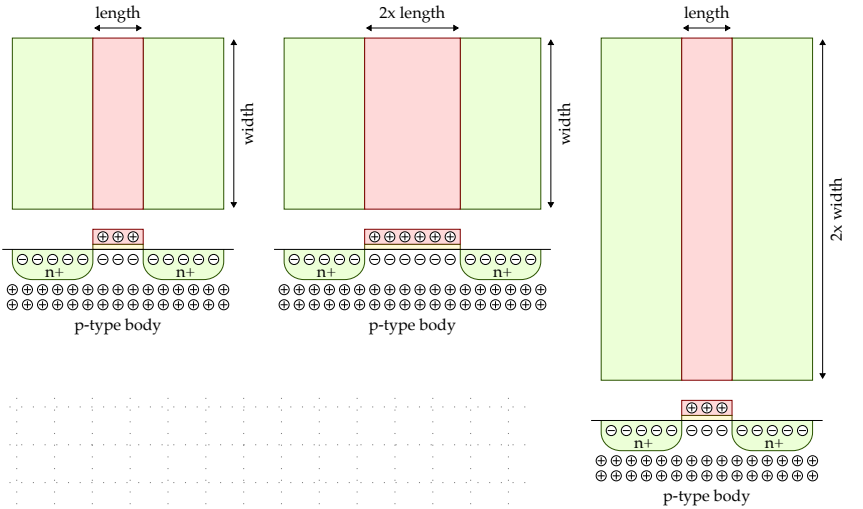


1.3. RC Model of an NMOS Transistor

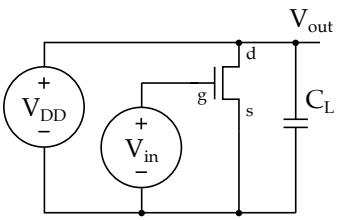


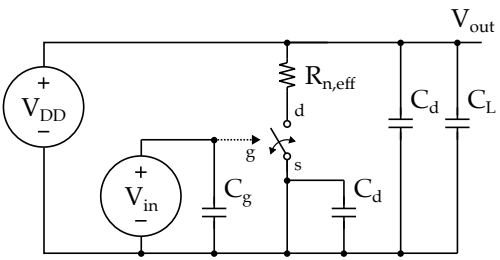


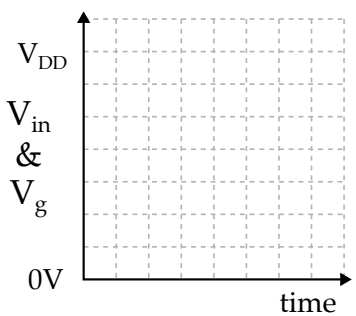
How does the RC model change with transistor length and width?

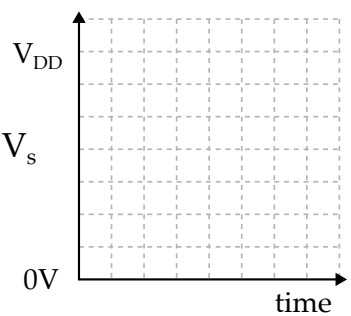


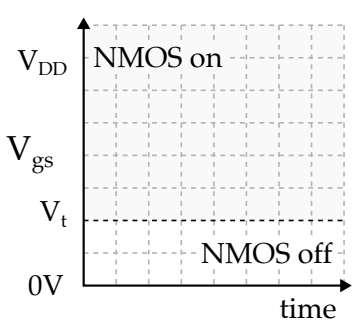
Consider discharging a load capacitance through an NMOS

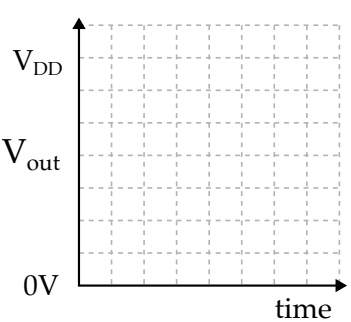




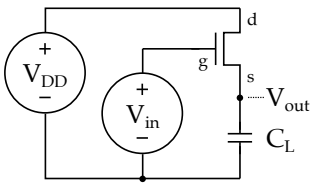


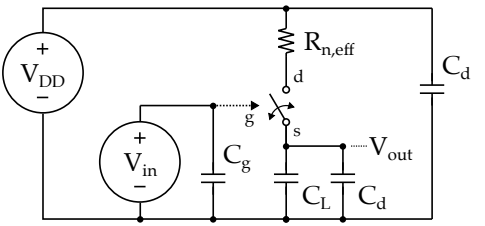


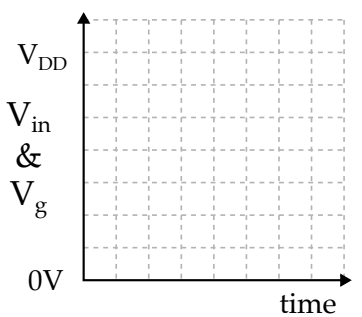


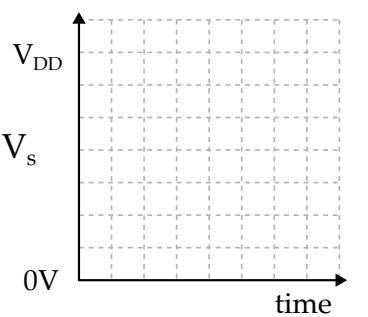


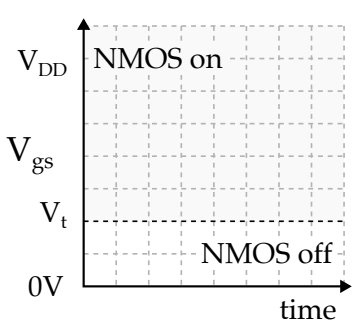
Consider charging a load capacitance through an NMOS

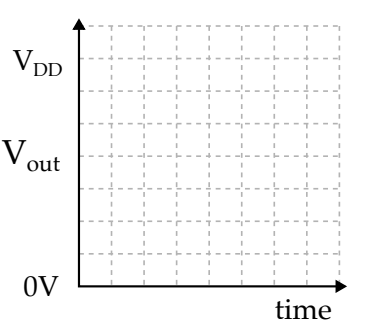




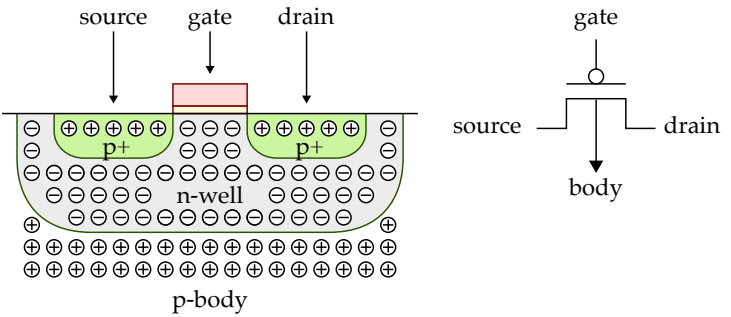




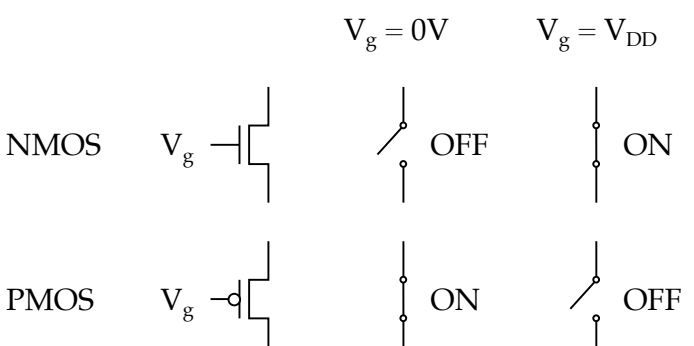




1.4. PMOS Transistors



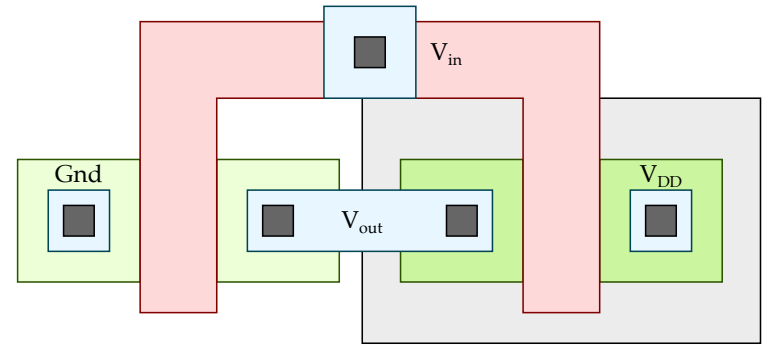
- A PMOS transistor uses p-type doped silicon to create a *source* and *drain* next to a MOS structure with a n-type body
- The voltage on the gate controls the inversion region which can create a *channel of holes* between the source and drain
  - When the MOS structure is in *depletion mode*, the transistor is *off* and no current flows through the channel
  - When the MOS structure is in *inversion mode*, the transistor is *on* and current flows through the channel

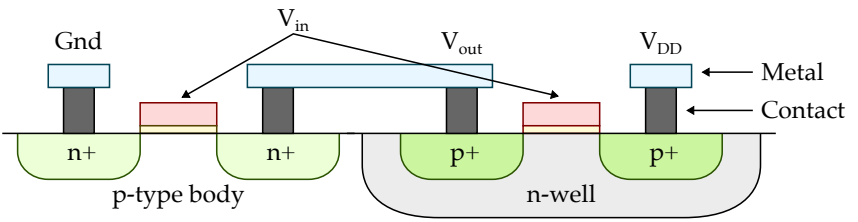


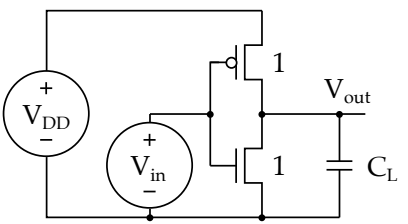
1.5. RC Model of an PMOS Transistor

- The *mobility* of holes is less than the *mobility* of electrons
- Consider an NMOS and PMOS of the same width and length
  - The effective resistance of the PMOS is higher than the NMOS
  - In this course, we will assume $R_{p,eff} = 2 \times R_{n,eff}$
- Assume the gate and diffusion capacitances are the same for both NMOS and PMOS transistors

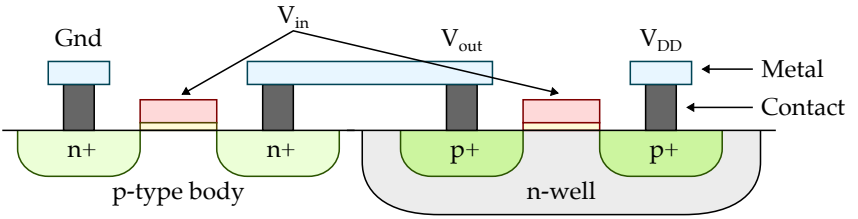
2. The Inverter

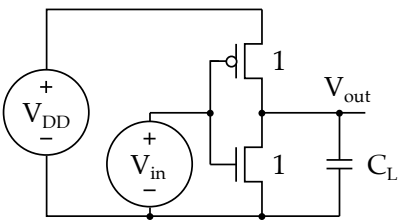




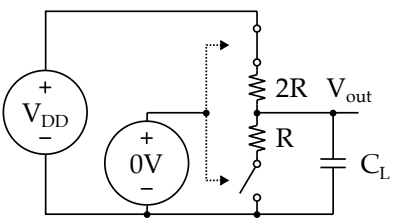


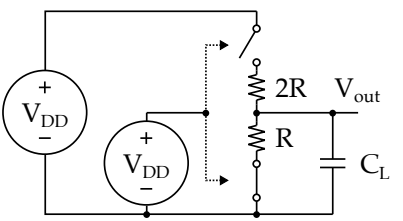
- Transistors are labeled with their size relative to a minimum width NMOS

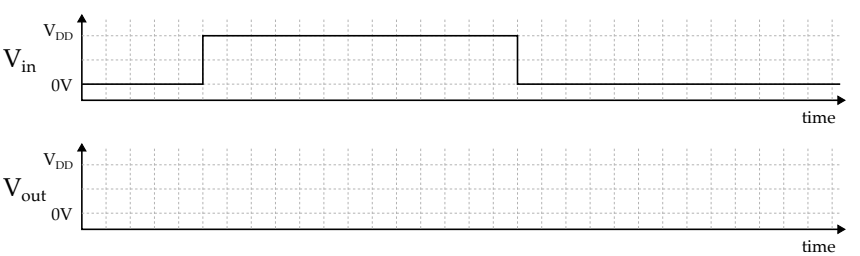


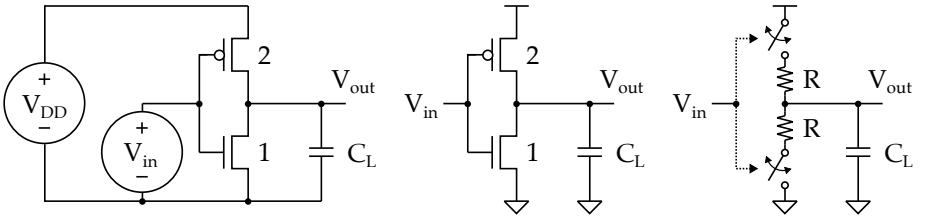


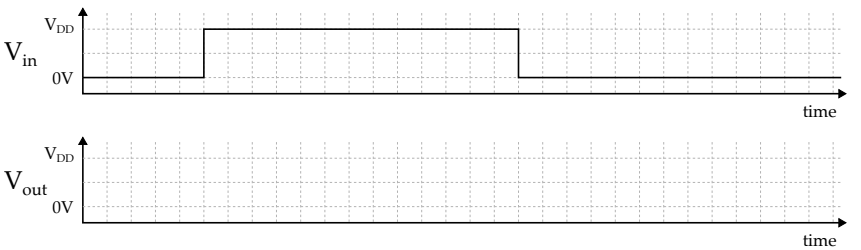
- For now ignore gate and diffusion capacitance
- Drive strength of an inverter is inversely proportional to the effective resistance

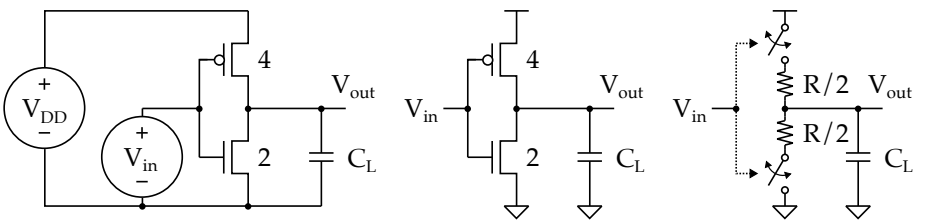


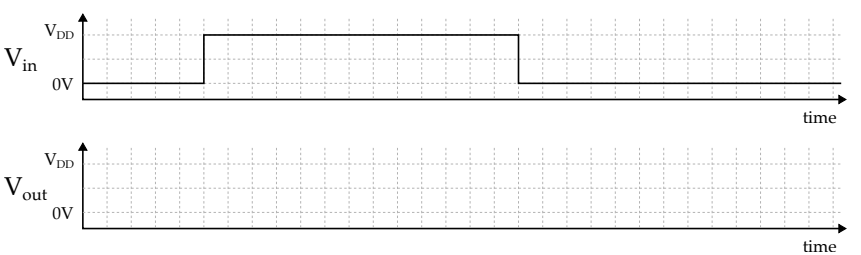




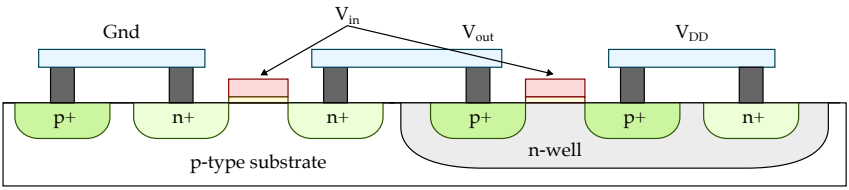

+
V_{DD}
−
+
V_{in}
−
2
1
V_{out}
C_L
V_{in}
2
1
V_{out}
C_L
V_{in}
R
R
V_{out}
C_L


V_{DD}
V_{in}
0V
time
V_{DD}
V_{out}
0V
time

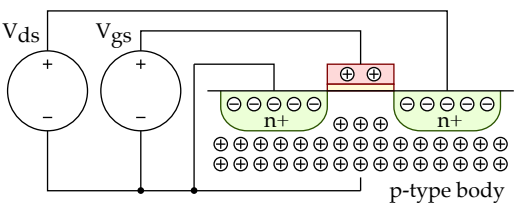

+
V_{DD}
−
+
V_{in}
−
4
2
V_{out}
C_L
V_{in}
4
2
V_{out}
C_L
V_{in}
R/2
R/2
V_{out}
C_L

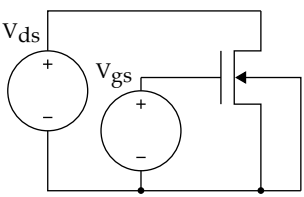

V_{DD}
V_{in}
0V
time
V_{DD}
V_{out}
0V
time

3. CMOS Fabrication



- Must connect the p-type body (substrate) to ground
- Must connect the n-well to VDD





Seven CMOS Fabrication Steps

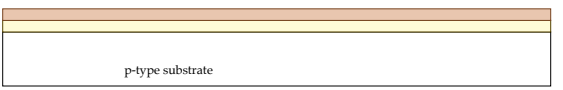
- Step 1: Fabricate n-well
- Step 2: Fabricate transistor gates
- Step 3: Fabricate n-type diffusion
- Step 4: Fabricate p-type diffusion
- Step 5: Fabricate contacts
- Step 6: Fabricate metal 1 wires
- Step 7: Fabricate rest of the metal stack

3.1. Step 1: Fabricate N-Well

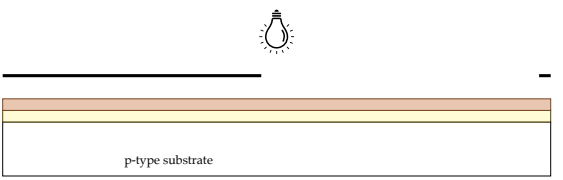
1.1: Bare Si wafer

1.2: Grow sacrificial SiO_2

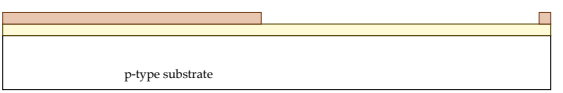
1.3: **Spin** on photoresist



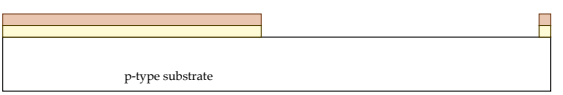
1.4: **Expose** photoresist



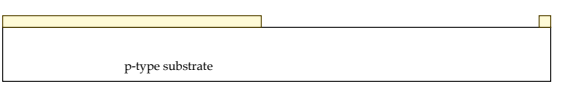
1.5: **Wash** photoresist



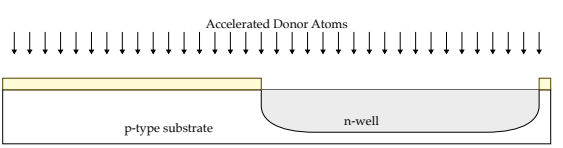
1.6: **Etch** SiO_2 with HF



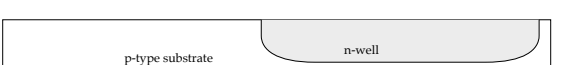
1.7: **Remove** photoresist



1.8: N-Type implant

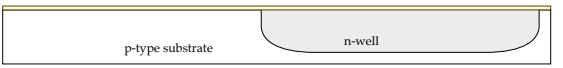


1.9: Remove SiO_2 with HF

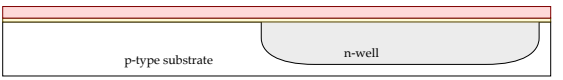


3.2. Step 2: Fabricate Transistor Gates

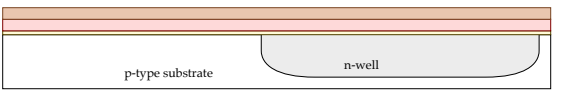
2.1: Grow thin SiO_2



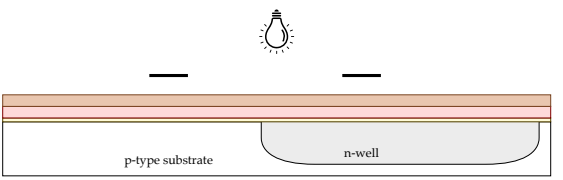
2.2: Deposit Polysilicon



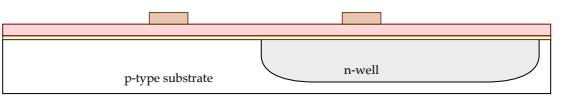
2.3: **Spin** on photoresist



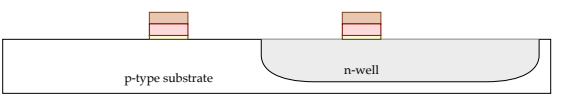
2.4: **Expose** photoresist



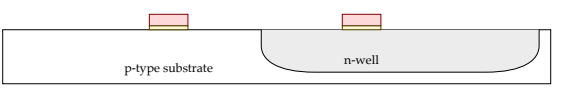
2.5: **Wash** photoresist



2.6: **Etch** Polysilicon & SiO_2

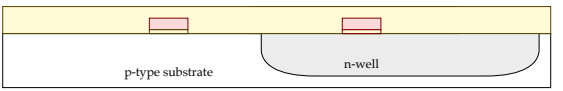


2.7: **Remove** photoresist

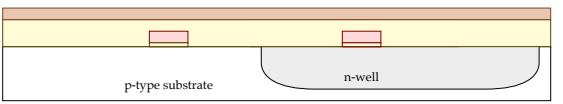


3.3. Step 3: Fabricate N-Type Diffusion

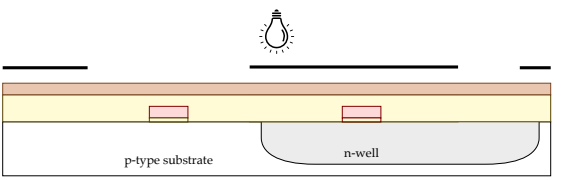
3.1: Grow sacrificial SiO_2



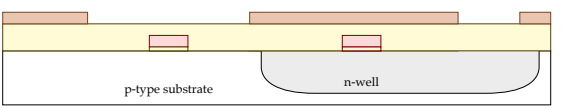
3.2: **Spin** on photoresist



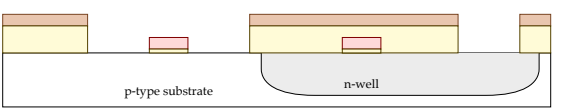
3.3: **Expose** photoresist



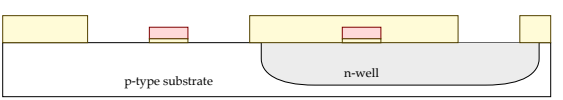
3.4: **Wash** photoresist



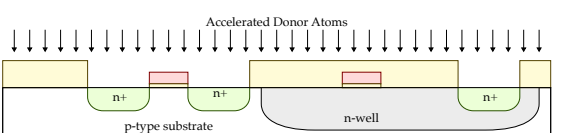
3.5: **Etch** SiO_2



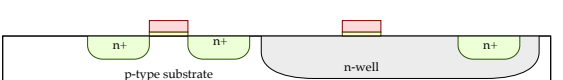
3.6: **Remove** photoresist



3.7: N-Type Implant

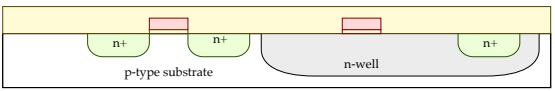


3.8: Remove SiO_2 with HF

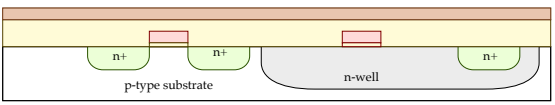


3.4. Step 4: Fabricate P-Type Diffusion

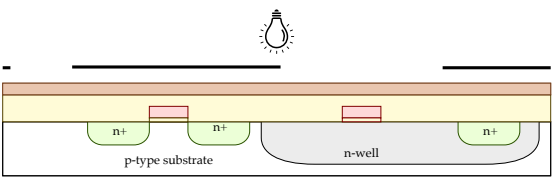
4.1: Grow sacrificial SiO_2



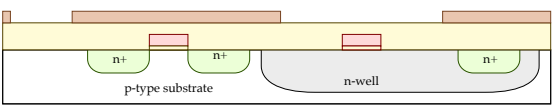
4.2: **Spin** on photoresist



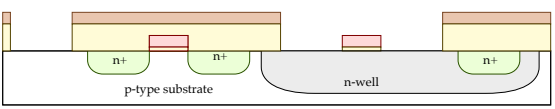
4.3: **Expose** photoresist



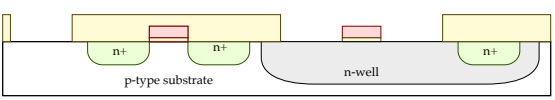
4.4: **Wash** photoresist



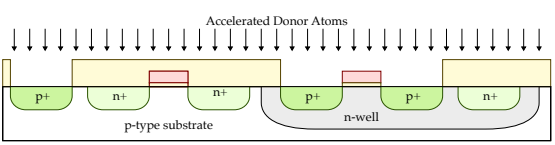
4.5: **Etch** SiO_2



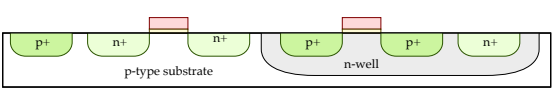
4.6: **Remove** photoresist



4.7: P-Type Implant

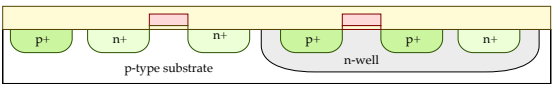


4.8: Remove SiO_2 with HF

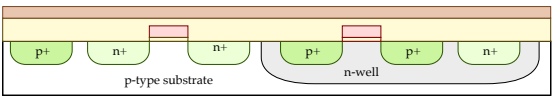


3.5. Step 5: Fabricate Contacts

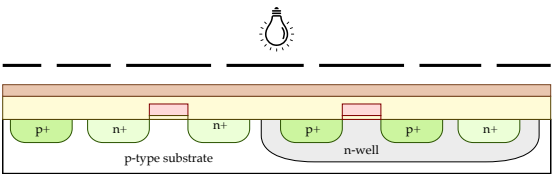
5.1: Grow thick SiO_2



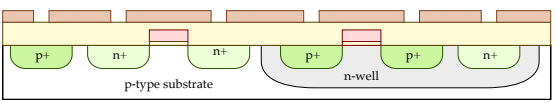
5.2: **Spin** on photoresist



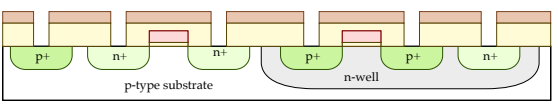
5.3: **Expose** photoresist



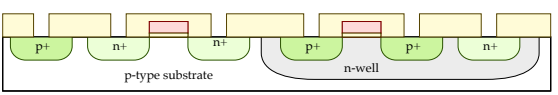
5.4: **Wash** photoresist



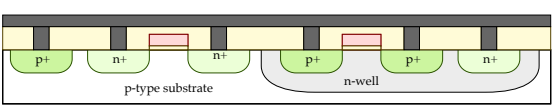
5.5: **Etch** SiO_2



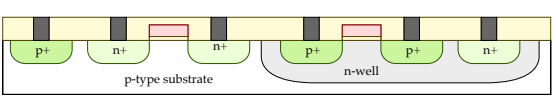
5.6: **Remove** photoresist



5.7: Deposit Tungsten

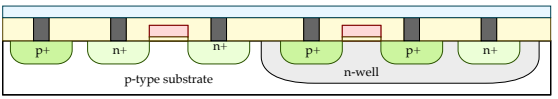


5.8: Chemical Mechanical Polishing

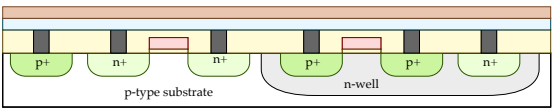


3.6. Step 6: Fabricate Metal 1 Wires

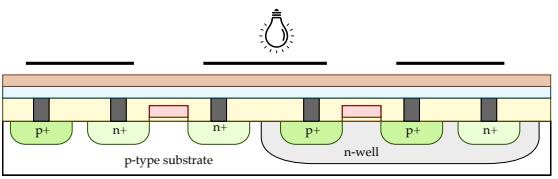
6.1: Deposit Aluminum



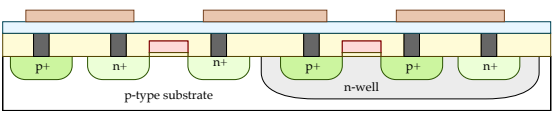
6.2: **Spin** on photoresist



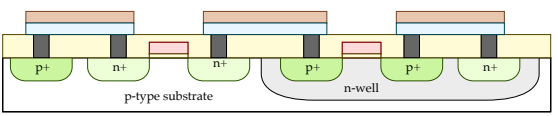
6.3: **Expose** photoresist



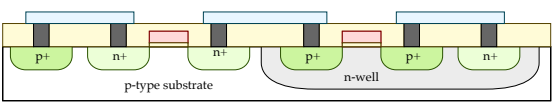
6.4: **Wash** photoresist



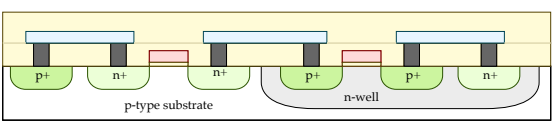
6.5: **Etch** Aluminum



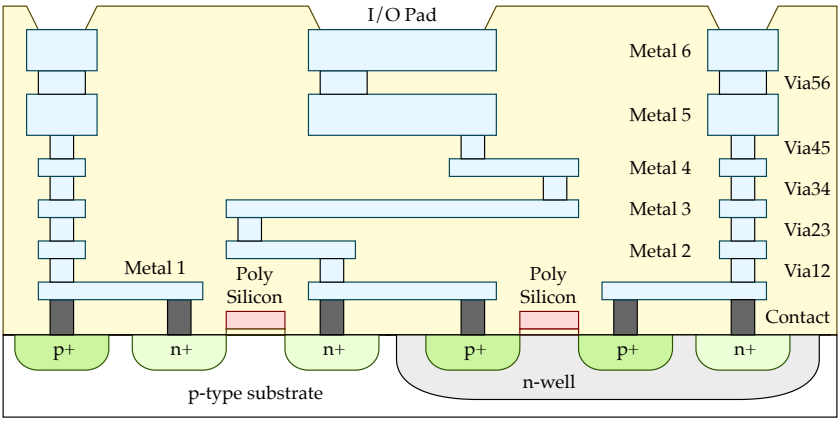
6.6: **Remove** photoresist



6.7: Grow thick SiO_2

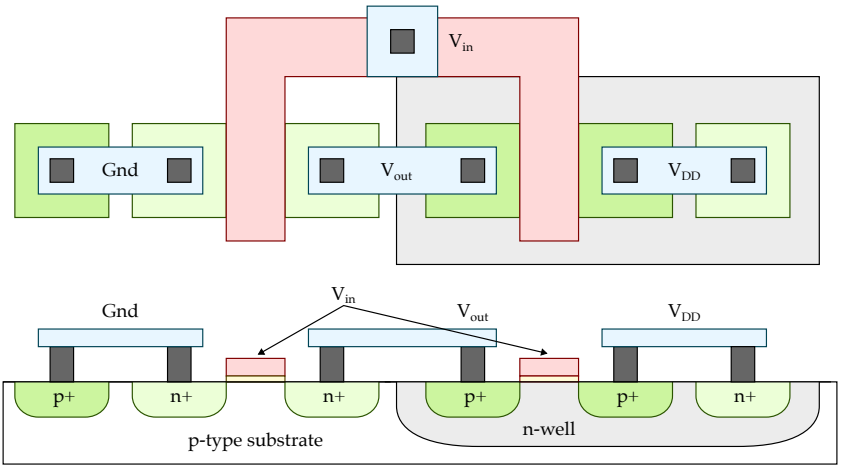


3.7. Step 7: Fabricate Rest of the Metal Stack

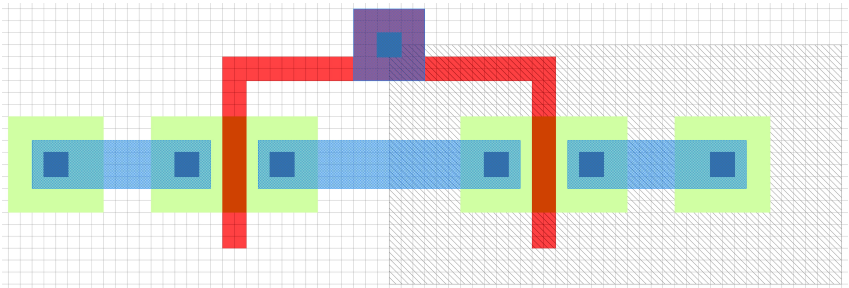


- Use same spin, expose, wash, etch, remove substems to create via connections between metal layers and metal wires
- Often need intermediate chemical mechanical polishing steps to ensure metal layers are planar
- Upper metal layers are often taller and wider to reduce wire resistance
- Openings in the SiO_2 at the very top of the stack create I/O pads which can be used to connect the package to the chip

4. Layout Design Rules

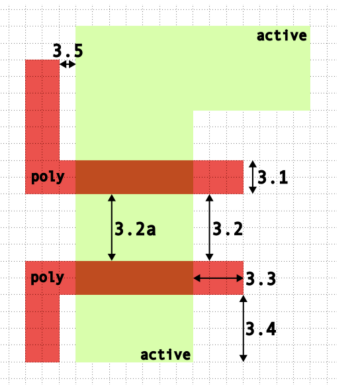


- Design rules specify constraints on layout that ensure feasible fabrication and correct transistor operation
- Micron-based design rules are specified in units of µm and are usually confidential
- Lambda-based design rules are specified in units of λ (i.e., half the minimum transistor length) and ideally are scalable across technologies
- Since Lambda-based design rules are generic they can be public



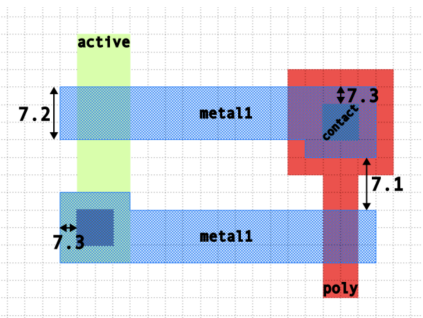
poly

Rule	Description	λ
3.1	Minimum width	2
3.2	Minimum spacing over field	3
3.2a	Minimum spacing over active	4
3.3	Minimum gate extension of active	3
3.4	Minimum active extension of poly	4
3.5	Minimum field poly to active	1



metal1

Rule	Description	λ
7.1	Minimum width	3
7.2	Minimum spacing	3
7.3	Minimum overlap of contact or via	1
7.4	Minimum spacing when either metal line is wider than 10 lambda	6
7.5	Minimum area	25 λ^2



5. TinyFlow: Full-Custom Design Flow

5.1. Files

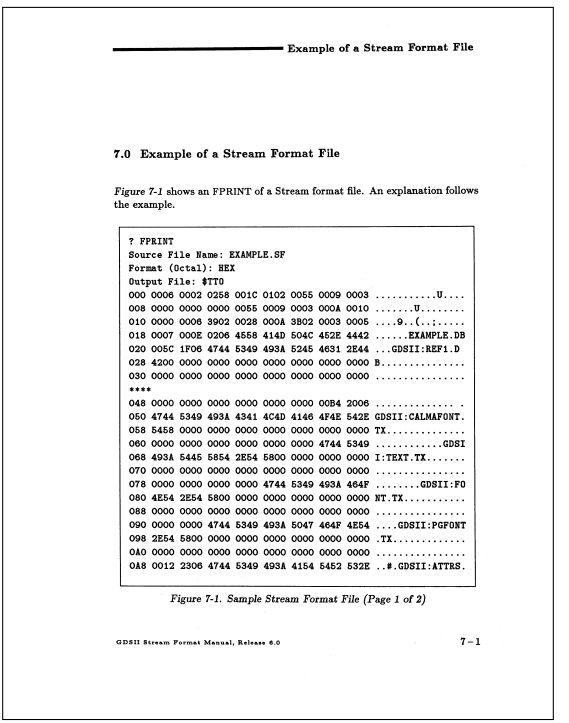
SPICE Format for Transisitor-Level Schematics (`.sp`)

```
* MMOS Discharging Capacitor
.param SUPPLY=1.8
.lib ...
.temp 125

VDD   vdd gnd SUPPLY

M1    out in gnd gnd NMOS L=0.18U W=0.72U

CLoad out gnd 12fF

VIN_  in gnd pwl( 0ns 0V 0.5ns 0V 0.7ns SUPPLY )

.ic   V(out)=SUPPLY
.tran 0.01ns 2.5ns

.control
run
plot V(in) V(out)
.endc
.end
```

```
* Inverter

.SUBCKT INV A Y VDD VSS

M_P Y A VDD VDD PMOS L=0.18U W=0.72U

M_N Y A VSS VSS NMOS L=0.18U W=0.72U

.ENDS INV
```

GDS Format for Layout Files (`.gds`)

- Layout used to be done on dedicated workstations, with all of the shape and layer information stored in the binary GDSII format
- When the layout was finished it would be stored on magnetic tape and shipped to the foundry
  - Tape-In: Creating a final GDS file
  - Tape-Out: Sending the final GDS file for fabrication



Example of a Stream Format File

7.0 Example of a Stream Format File

Figure 7-1 shows an FPRINT of a Stream format file. An explanation follows the example.

```
? FPRINT
Source File Name: EXAMPLE.SF
Format (Octal): HEX
Output File: $TTO
000 0006 0002 0258 001C 0102 0055 0009 0003 ..........U....
008 0000 0000 0000 0055 0009 0003 000A 0010 .......U........
010 0000 0006 3902 0028 000A 3B02 0003 0005 ....9..(..;.....
018 0007 000E 0206 4558 414D 504C 452E 4442 ......EXAMPLE.DB
020 005C 1F06 4744 5349 493A 5245 4631 2E44 ...GDSII:REF1.D
028 4200 0000 0000 0000 0000 0000 0000 0000 B...............
030 0000 0000 0000 0000 0000 0000 0000 0000 ................
****
048 0000 0000 0000 0000 0000 0000 00B4 2006 ..............  .
050 4744 5349 493A 4341 4C4D 4146 4F4E 542E GDSII:CALMAFONT.
058 5458 0000 0000 0000 0000 0000 0000 0000 TX..............
060 0000 0000 0000 0000 0000 0000 4744 5349 ............GDSI
068 493A 5445 5854 2E54 5800 0000 0000 0000 I:TEXT.TX.......
070 0000 0000 0000 0000 0000 0000 0000 0000 ................
078 0000 0000 0000 0000 0000 4744 5349 493A ........GDSII:
080 4F54 2E54 5800 0000 0000 0000 0000 0000 FO.TX..........
088 0000 0000 0000 0000 0000 0000 0000 0000 ................
090 0000 0000 0000 4744 5349 493A 5047 464F ....GDSII:PGFONT
098 2E54 5800 0000 0000 0000 0000 0000 0000 .TX............
0A0 0000 0000 0000 0000 0000 0000 0000 0000 ................
0A8 0012 2306 4744 5349 493A 4154 5452 532E ..#.GDSII:ATTRS.
```

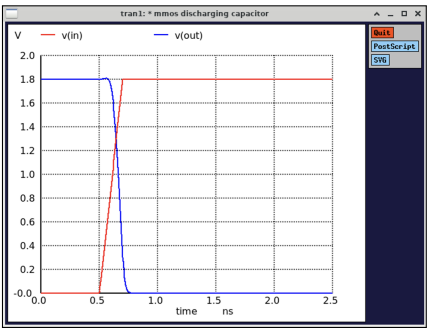
Figure 7-1. Sample Stream Format File (Page 1 of 2)

GDSII Stream Format Manual, Release 6.0 7 – 1

5.2. Tools

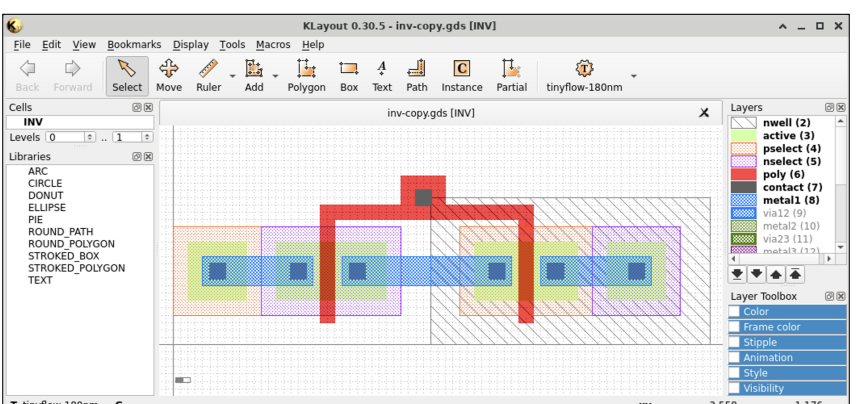
Ngspice

- Simulate transistor-level schematics
- Analyze and plot the results

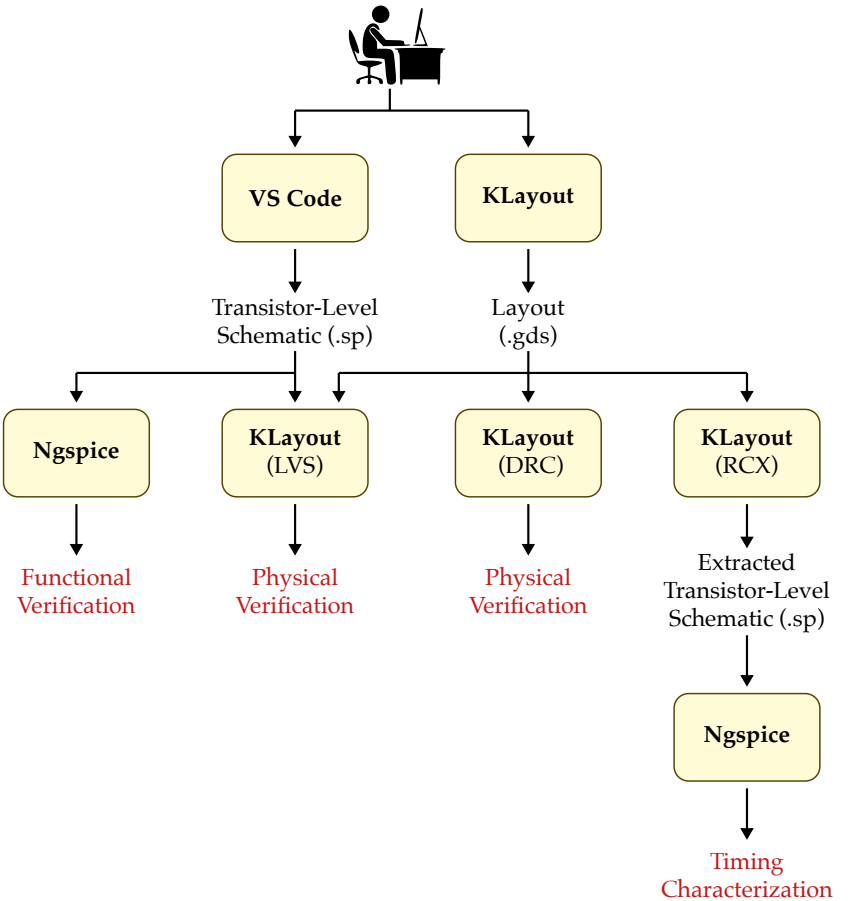


Klayout

- Open, edit, save GDS files
- Compare layout-vs-schematic (LVS)
- Design rule checking (DRC)
- Resistance and capacitance extraction (RCX)



5.3. Flow


VS Code
KLayout
Transistor-Level Schematic (.sp)
Layout (.gds)
Ngspice
KLayout (LVS)
KLayout (DRC)
KLayout (RCX)
Functional Verification
Physical Verification
Physical Verification
Extracted Transistor-Level Schematic (.sp)
Ngspice
Timing Characterization