ECE 5745 Complex Digital ASIC Design, Spring 2023
Next Steps

School of Electrical and Computer Engineering
Cornell University

revision: 2023-01-24-12-19

Only complete these next steps if you are officially enrolled in the course, or have spoken with the instructor and anticipate enrolling in the course right away.

1. Verify you can view the Canvas course site and Ed discussion forum

We will be using Canvas for distributing course materials, collecting assignments, and distributing grades. Please make sure that if you are officially enrolled in the course you can view this course in Canvas. We will be using Ed for all announcements, online discussion, and most student/instructor communication. Students officially enrolled should already be automatically added to the Ed discussion forum for this course. Please use the link in Canvas to make sure you can view the Ed discussion forum.

2. Read the course syllabus

The course syllabus contains essential information about the course motivation, structure, procedures, and policies. It will be assumed that all students have read and understand all of the material in the course syllabus.

3. Read Chapter 1 of Weste and Harris

The course textbook is *"CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed."* by Neil Weste and David Harris. For your convenience, the first chapter is available as a PDF on the Canvas course page in the readings section.

4. Review background material as necessary

Students which are less confident of their mastery of the material covered in ECE 4750 might consider reviewing the material on the ECE 4750 public course website. Students which are new to Verilog might find it useful to review a text on this hardware-description language, such as "Verilog HDL, 2nd ed." by Samir Palnitkar. Students which have never used Python before may want to spend additional time reviewing the textbook titled "Think Python: How to Think Like a Computer Scientist" by A. B. Downey (Green Tea Press, 2012) (which is also available as a PDF on the Canvas course page in the resources section).

5. Work through lab tutorials

Various lab tutorials will be posted on the public course website to help you familiarize yourself with the Verilog hardware modeling framework, Python testing framework, and the ASIC CAD toolflow. We have already posted tutorials on remote access to ecelinux, Linux, git, and Verilog. These first four tutorials are the same as used in ECE 4750, but students may still find it useful to

review them to refresh their understanding of important tools, techniques, and guidelines. Additional tutorials will be posted soon.

6. Fill out online form with your GitHub username

If you do not already have a GitHub account, go to `https://github.com/join`. Make sure you use your `netid@cornell.edu` email address if you are creating a new account. Your NetID makes a good GitHub username. Then go to `http://www.csl.cornell.edu/courses/ece5745/signup` and fill out the sign-up form with your NetID and GitHub username. This will allow the instructors to add your GitHub account to the GitHub organization created for this course.

7. Begin selecting a partner for the lab assignments and project

The lab assignments are specifically designed to be a reasonable amount of work for a pair of two students working together. Students should begin the process of selecting a partner, since this choice can often make a significant difference in succeeding on the lab assignments.

8. Attend the discussion section on Friday in 225 Upson Hall

Students are expected to attend the weekly discussion section. This week will be the front-end portion of the ASIC toolflow. The discussion section is on Fridays from 3:45–4:35pm in 225 Upson Hall.