**ECE 5745 Complex Digital ASIC Design, Spring 2021**

**Next Steps**

School of Electrical and Computer Engineering  
Cornell University

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Only complete these next steps if you are officially enrolled in the course, or have spoken with the instructor and anticipate enrolling in the course right away.

1. **Read the course syllabus**

   The course syllabus contains essential information about the course motivation, structure, procedures, and policies. It will be assumed that all students have read and understand all of the material in the course syllabus.

2. **Fill out online form with your GitHub username**

   If you do not already have a GitHub account, go to [https://github.com/join](https://github.com/join). Make sure you use your `netid@cornell.edu` email address if you are creating a new account. Your NetID makes a good GitHub username. Then go to [http://www.csl.cornell.edu/courses/ece5745/signup](http://www.csl.cornell.edu/courses/ece5745/signup) and fill out the sign-up form with your NetID and GitHub username. This will allow the instructors to add your GitHub account to the GitHub organization created for this course.

3. **Log into Ed Discussions**

   We will be using Ed Discussions for online discussion and most student/instructor communication. All students officially enrolled will be automatically added to the Ed Discussions page for this course. Please verify that you can access Ed Discussions using the link on Canvas.

4. **Work through lab tutorials**

   Various lab tutorials will be posted on the public course website to help you familiarize yourself with the Python/Verilog-based hardware modeling framework and the ASIC CAD toolflow. We have already posted five tutorials on remote access to ecelinux, Linux, git, PyMTL3, and Verilog. **Students must complete tutorial 0 before the discussion section on Friday!** Students should start working on all tutorials, especially if they are new to Linux, Git, PyMTL3, or Verilog.

5. **Attend extra lab/office hours on Friday if necessary**

   Jack Brzozowksi will be holding extra lab/office hours on Friday from 1:30-3:30pm via the standard course Zoom link to help any student with tutorial 0 so they can have remote access setup before the discussion section. **If you are having trouble with tutorial 0, please visit Jack on Friday before the discussion section!**
6. **Attend the virtual discussion section on Friday**

Attendance at the weekly discussion sections are optional but strongly encouraged. This week we will be discussing the front-end portion of the ASIC toolflow. This week’s discussion section will be on Friday via the standard Zoom course link from 3:45–4:35pm. **Again, students must complete tutorial 0 before the discussion section on Friday!**

7. **Read Chapter 1 of Weste and Harris**

The course textbook is “CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed.” by Neil Weste and David Harris. For your convenience, the first chapter is available as a PDF on the Canvas course page in the readings section.

8. **Review background material as necessary**

Students which are less confident of their mastery of the material covered in ECE 4750 might consider reviewing the material on the ECE 4750 public course website. Students which are new to Verilog might find it useful to review a text on this hardware-description language, such as “Verilog HDL, 2nd ed.” by Samir Palnitkar. Students which have never used Python before may want to spend additional time reviewing the textbook titled “Think Python: How to Think Like a Computer Scientist” by A. B. Downey (Green Tea Press, 2012) (which is also available as a PDF on the Canvas course page in the resources section).

9. **Begin selecting a partner for the lab assignments and project**

The lab assignments are specifically designed to be a reasonable amount of work for a pair of two students working together. Students should begin the process of selecting a partner, since this choice can often make a significant difference in succeeding on the lab assignments.