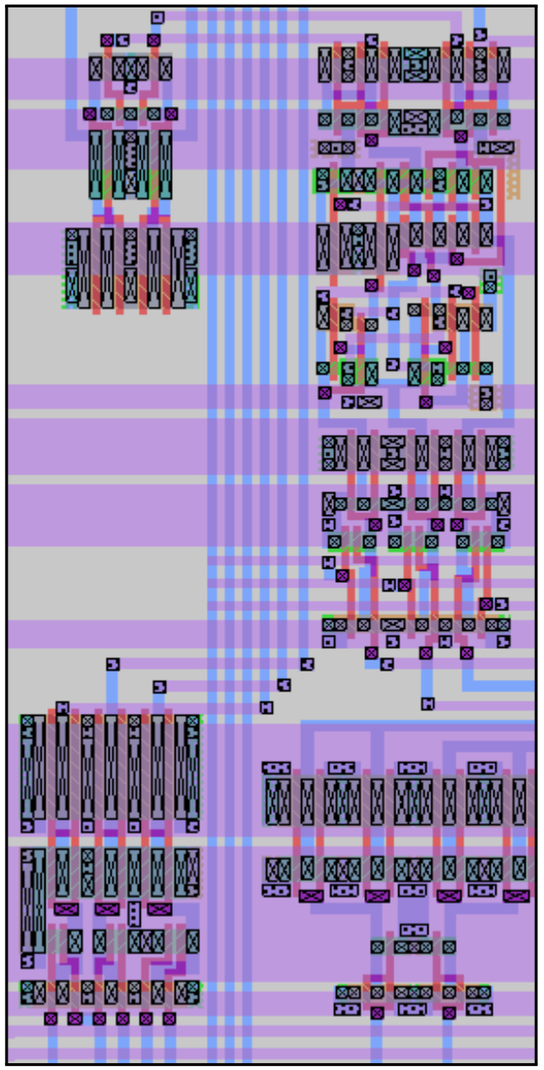
Using ASIC Flow to Quantify Cycle Time

ECE 4750 Computer Architecture
Discussion Section

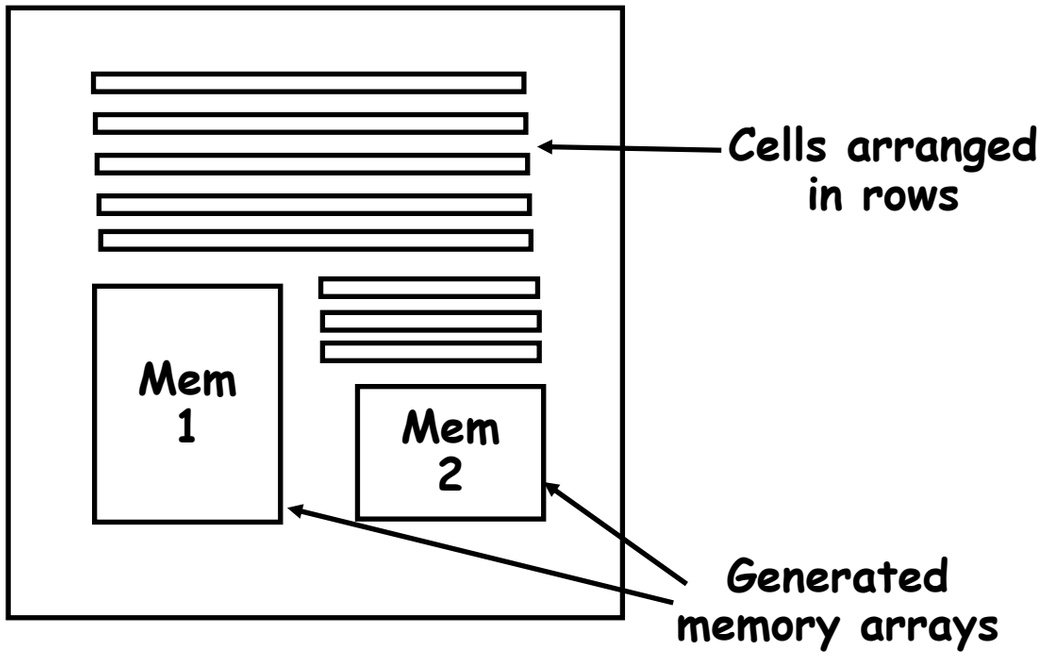
Full Custom Design vs. Standard-Cell Design

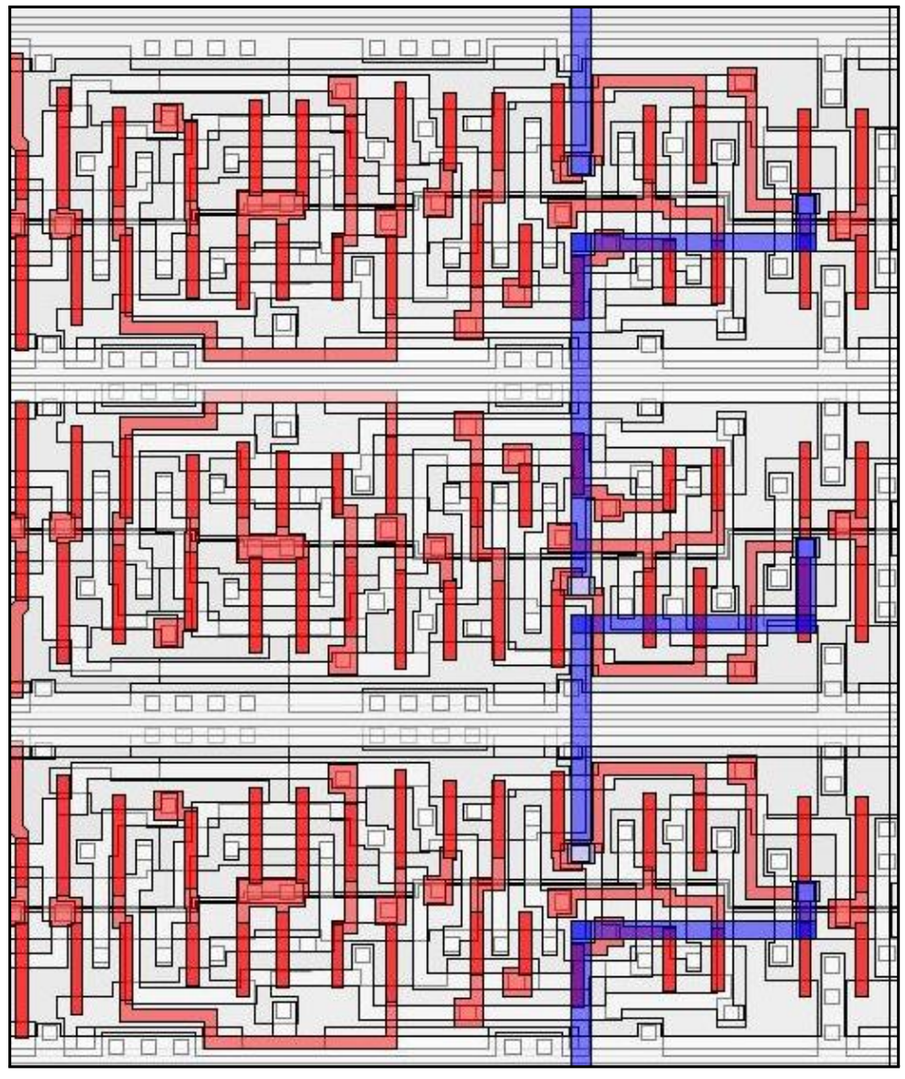


Full-custom layout in 1.0µm w/ 2 metal layers

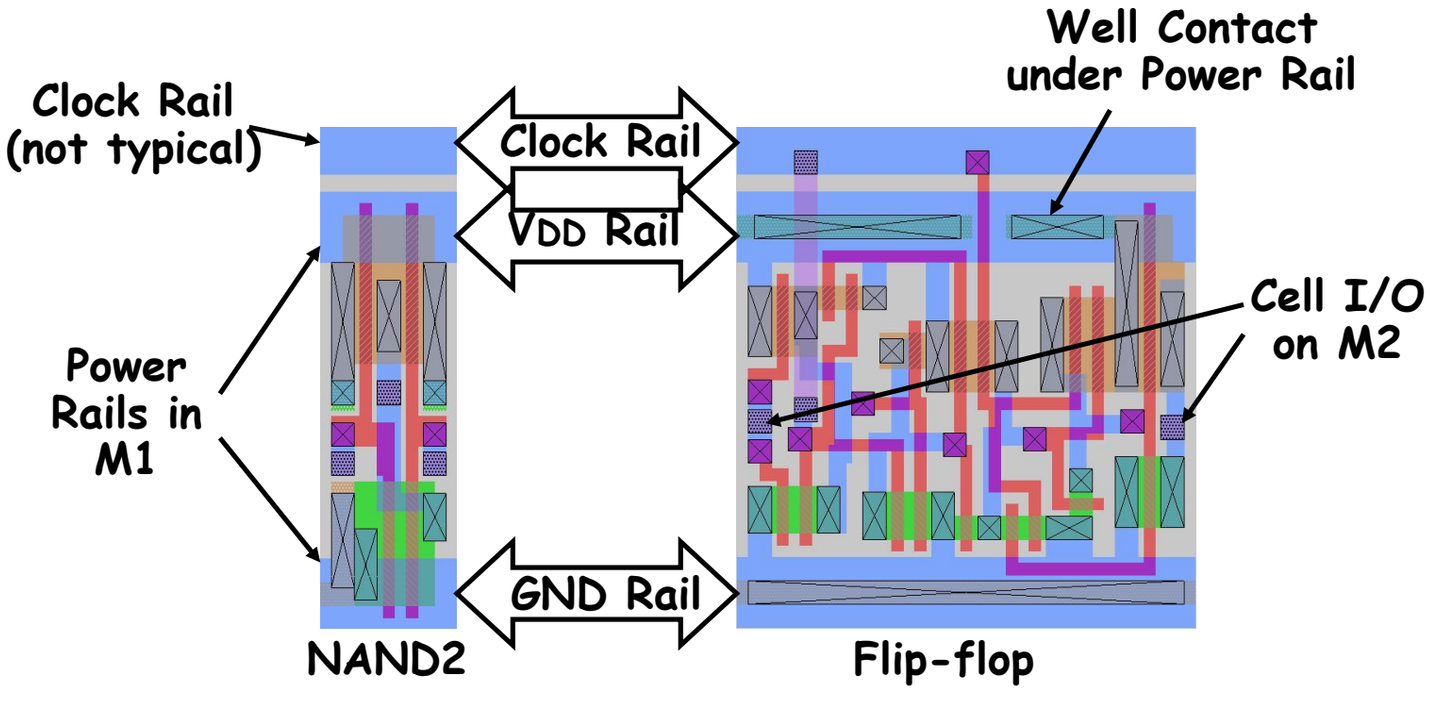
- Full-Custom Design
  - Designer is free to do anything, anywhere; though team usually imposes some design discipline
  - Most time consuming design style; reserved for very high performance or very high volume chips (Intel microprocessors, RF power amps for cellphones)
- Standard-Cell Design
  - Fixed library of “standard cells” and SRAM memory generators
  - Register-transfer-level description is automatically mapped to this library of standard cells, then these cells are placed and routed automatically
  - Enables agile hardware design methodology

Standard-Cell Design Methodology

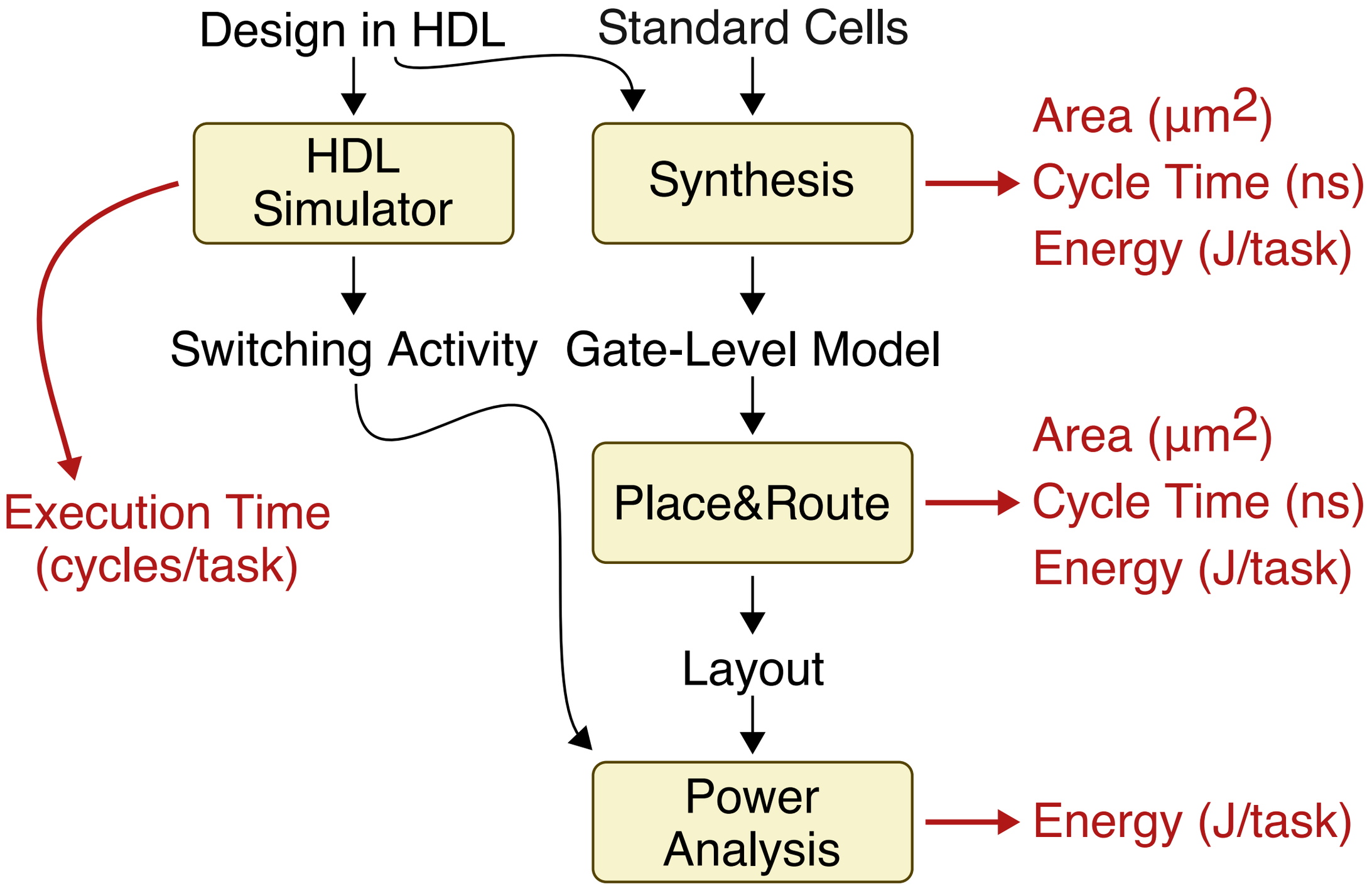




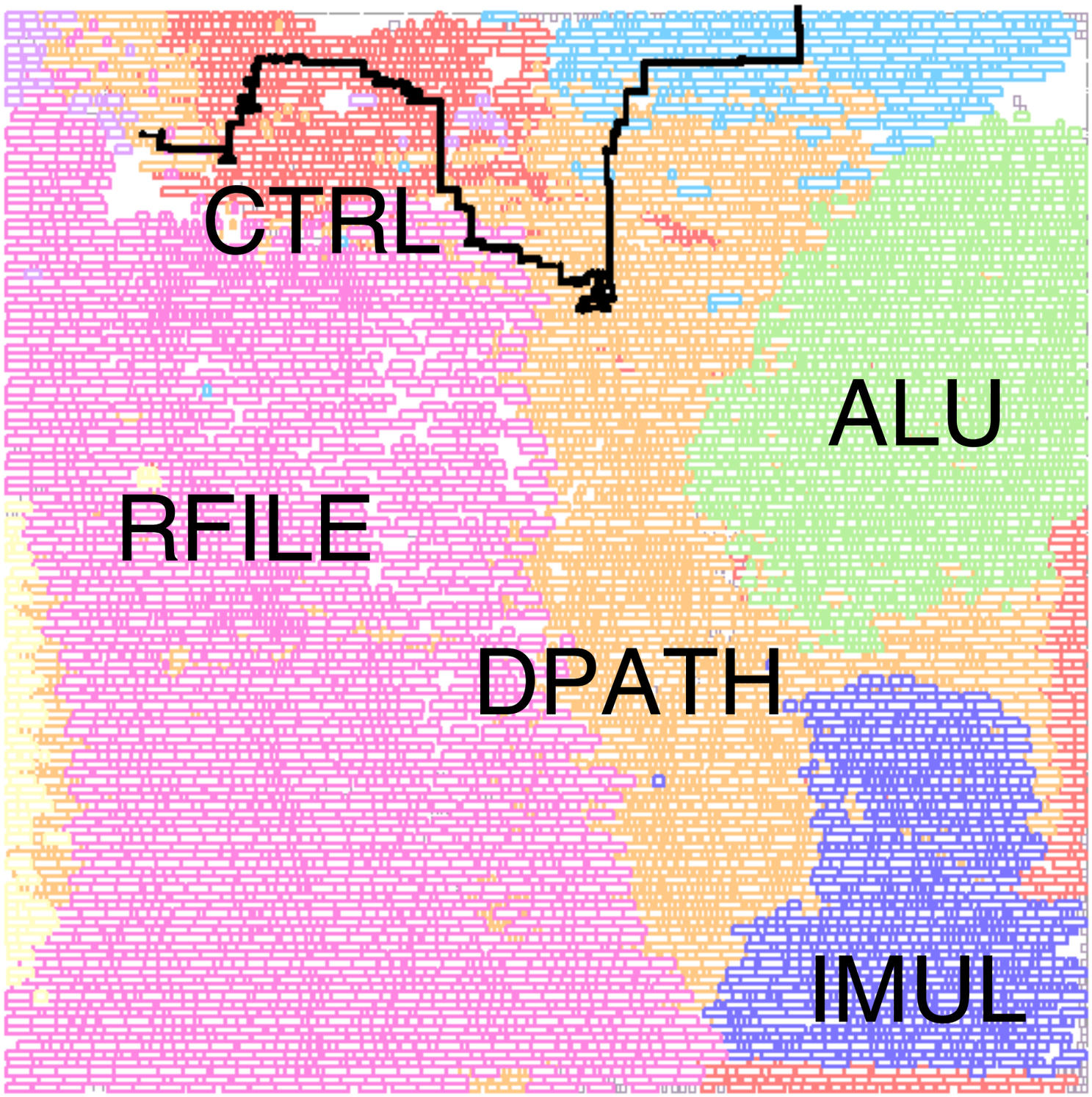
Ripple carry adder with carry chain highlighted

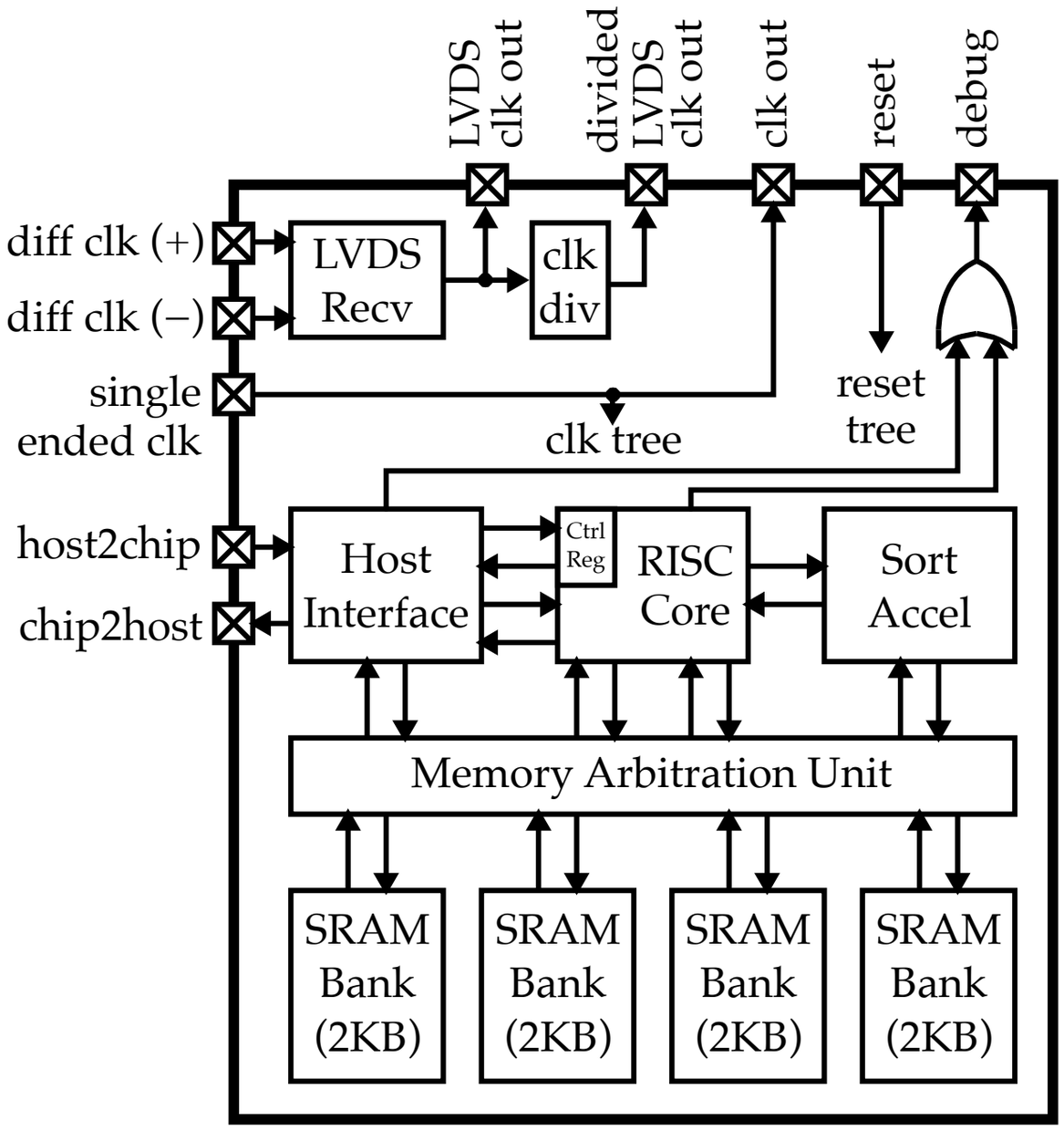


Standard-Cell Design Methodology



TinyRV2 Stalling Processor · 90nm Tech

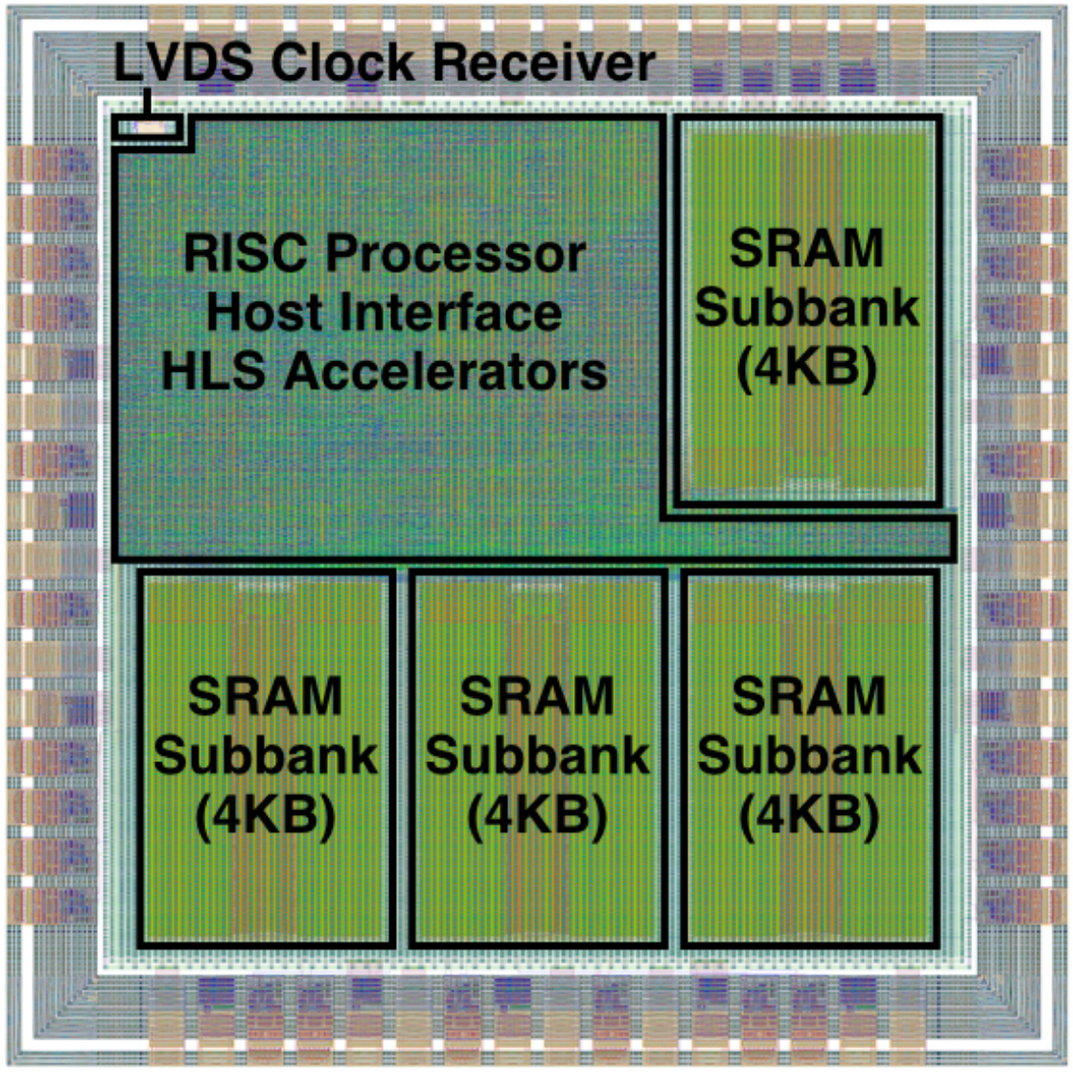




Testing Plans After Fabrication

The testing platform enables running small test programs on BRGTC1 to compare the performance and energy of pure-software kernels versus the HLS-generated sorting accelerator

Taped out in March 2016
Expected return in Fall 2016



Taped-out Layout for BRGTC1

2x2mm 1.3M transistors in IBM 130nm
RISC processor, 16KB SRAM
HLS-generated accelerators
Static Timing Analysis Freq. @ 246 MHz

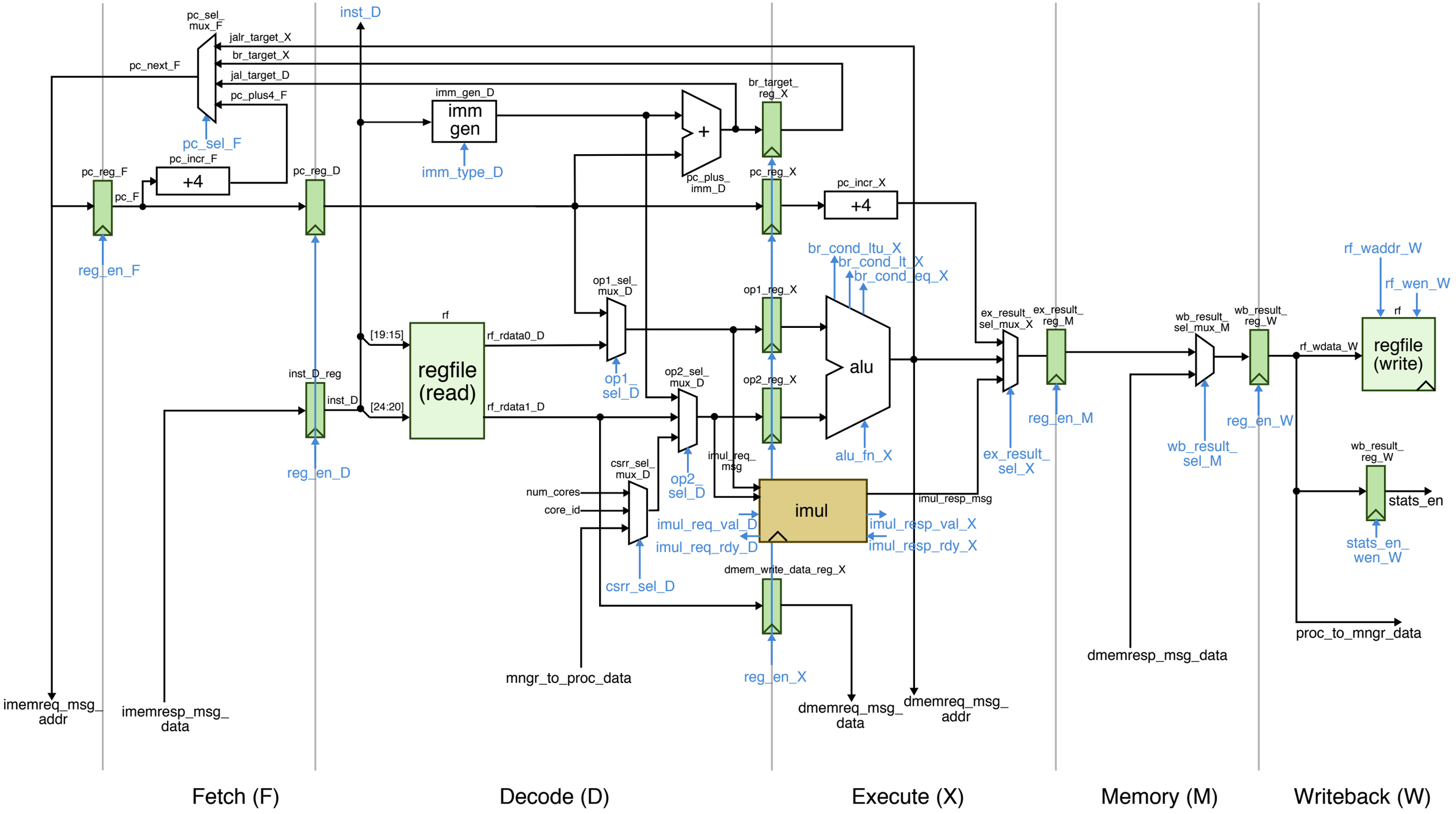
All numbers here are generate from …

- Synopsys Design Compiler / IC compiler
- Synopsys **90nm** Generic Library for **Teaching IC Design**

Quote: Intel's Pentium D (Smithfield) – 90 nm process technology (2.66–3.2 GHz)

- Introduced May 26, 2005
- 2.66–3.2 GHz (model numbers 805–840)
- Number of transistors 230 million
- 1 MB × 2 (non-shared, 2 MB total) L2 cache
- Cache coherency between cores requires communication over the FSB
- Performance increase of 60% over similarly clocked Prescott
- 2.66 GHz (533 MHz FSB) Pentium D 805 introduced December 2005
- Contains 2x **Prescott** dies in one package
- Family 15 Model 4

TinyRV2 Stalling Processor Datapath



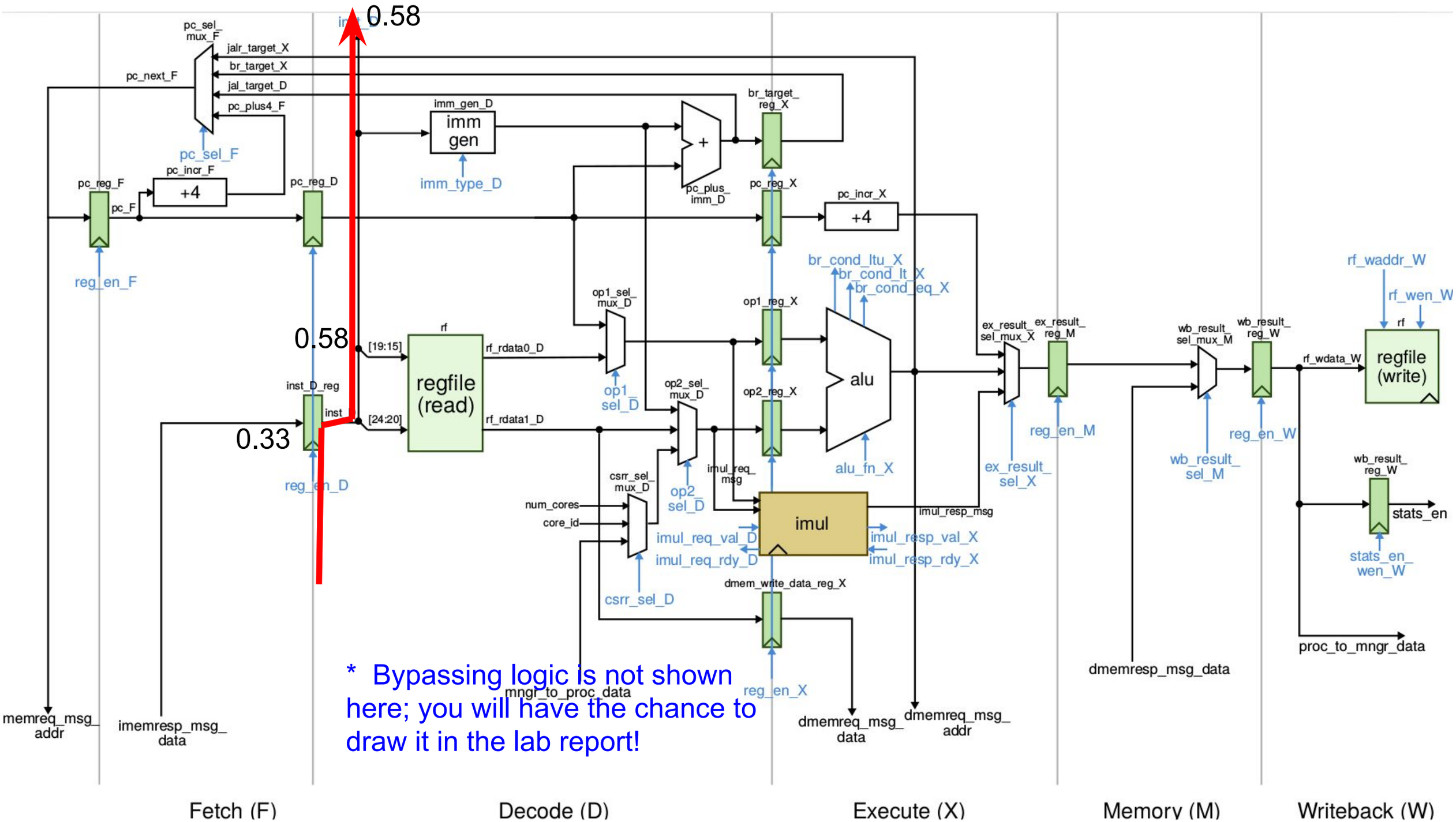
Fetch (F) | Decode (D) | Execute (X) | Memory (M) | Writeback (W)

Tracing the Critical Path

```
clock ideal_clock1 (rise edge)                          0.0000  0.0000
clock network delay (propagated)                        0.3343  0.3343
dpath/inst_D_reg/out_reg_24_/CLK (DFFX1)                0.0000  0.3343 r
dpath/inst_D_reg/out_reg_24_/Q (DFFX1)                  0.2441  0.5784 f
dpath/inst_D_reg/out[24] (RegEnRst)                     0.0000  0.5784 f
  dpath/inst_D[24] (ProcAltDpathPRTL)                   0.0000  0.5784 f
  ctrl/IN5 (ProcAltCtrlPRTL)                            0.0000  0.5784 f
```

Clock propagation + CLK-to-Q = 0.58ns!

Tracing the Critical Path

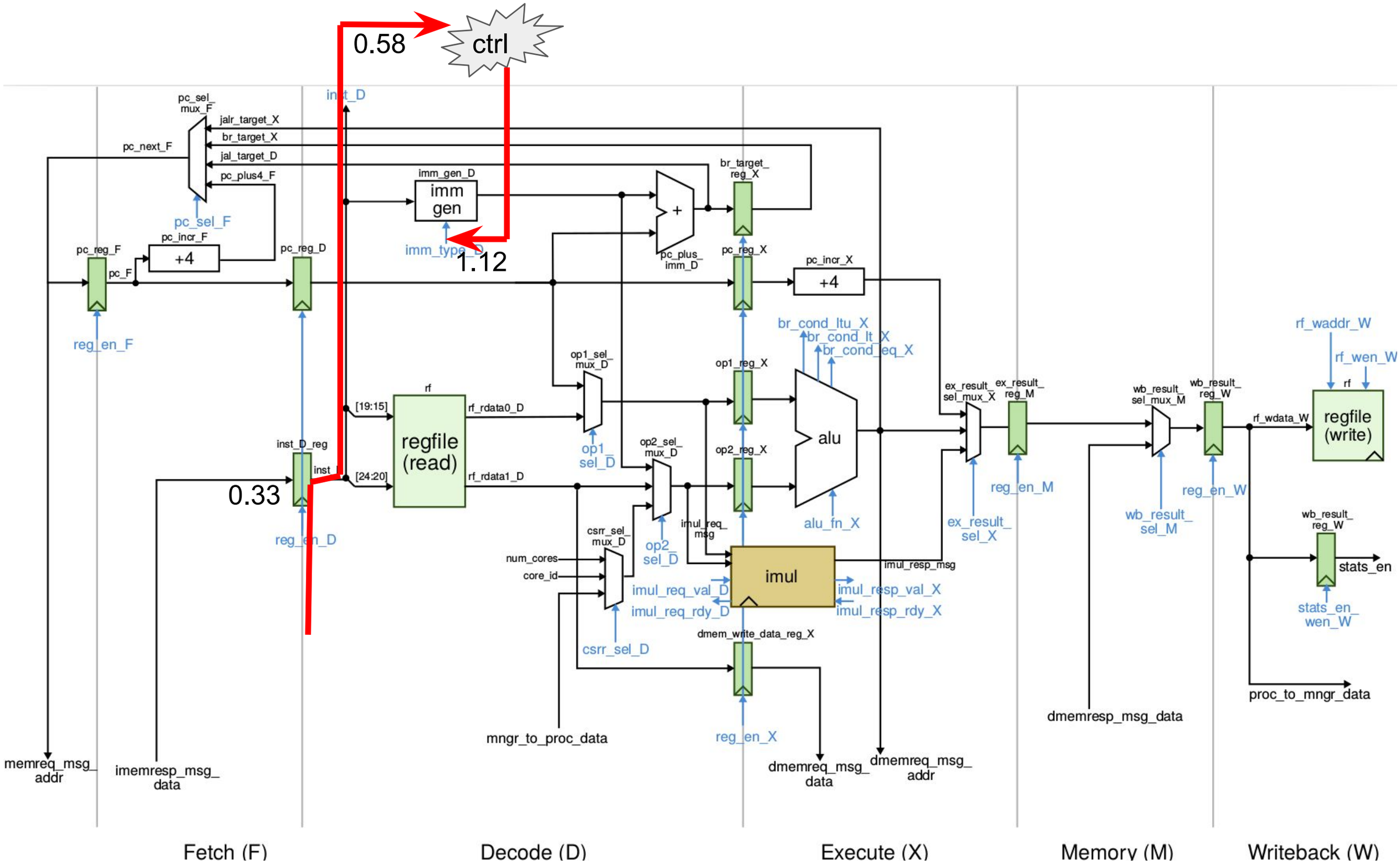


Tracing the Critical Path

```
ctrl/inst_type_decoder_D/in_[24] (DecodeInstType)                    0.0000  0.5784 f
...
ctrl/inst_type_decoder_D/dp_ipo3/Q (OR4X2)                           0.0961  0.9872 f
ctrl/inst_type_decoder_D/out[0] (DecodeInstType)                     0.0000  0.9872 f
...
  ctrl/imm_type_D[0] (ProcAltCtrlPRTL)                               0.0000  1.1241 r
  dpath/imm_type_D[0] (ProcAltDpathPRTL)                             0.0000  1.1241 r
```

Decode an instruction = 0.54ns!

Tracing the Critical Path

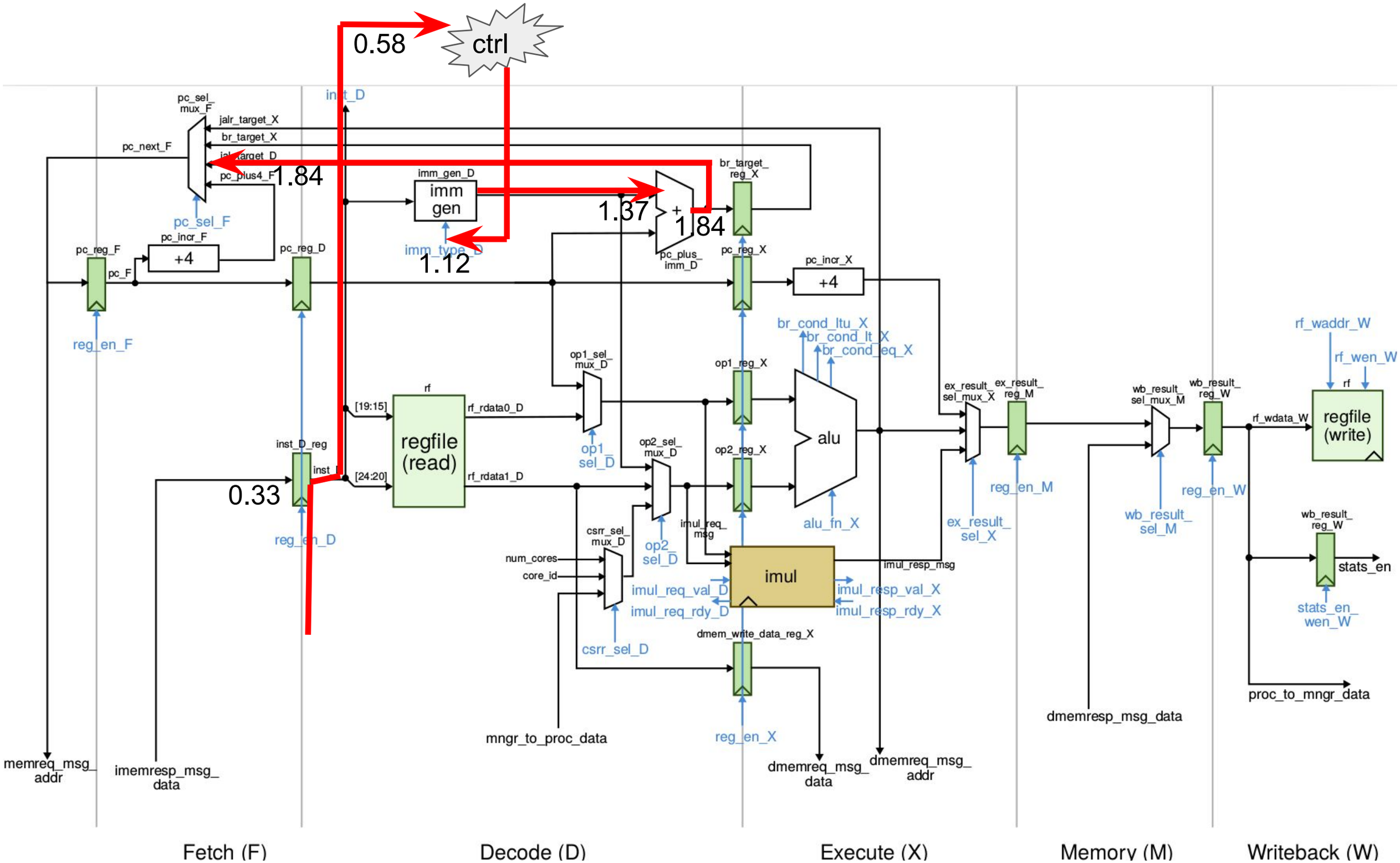


Tracing the Critical Path

```
dpath/imm_type_D[0] (ProcAltDpathPRTL)                    0.0000  1.1241 r
dpath/imm_gen_D/imm_type[0] (ImmGenPRTL)                  0.0000  1.1241 r
dpath/imm_gen_D/U2/IN2 (NOR2X4)                           0.0011  1.1253 r
...
dpath/imm_gen_D/U63/Q (AO21X1)                            0.1116  1.3726 f
  dpath/imm_gen_D/imm[13] (ImmGenPRTL)                    0.0000  1.3726 f
  dpath/pc_plus_imm_D/in1[13] (Adder)                     0.0000  1.3726 f
  ...
  dpath/pc_plus_imm_D/out[19] (Adder)                     0.0000  1.8441 r
```

Generating imm = 0.25ns, addition = 0.47ns!

Tracing the Critical Path



Tracing the Critical Path

```
dpath/pc_sel_mux_F/in__002[19] (Mux)                          0.0000  1.8441 r
...
dpath/pc_sel_mux_F/out[19] (Mux)                              0.0000  1.9050 r
dpath/imemreq_msg[53] (ProcAltDpathPRTL)                      0.0000  1.9050 r
  imemreq_queue/q1/dpath/bypass_mux/out[53] (Mux)             0.0000  2.0747 r
  ...
  imemreq_msg[53] (out)                                       0.0001  2.0748 r
```

Bypass queue = 0.17ns!

Tracing the Critical Path