ECE 4750 Computer Architecture, Fall 2016
Next Steps

School of Electrical and Computer Engineering
Cornell University

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Regardless of whether or not your are officially enrolled in this course, if you are interested in taking this course for either credit or as an auditor you must go through the following steps.

1. Read the course syllabus

The course syllabus contains essential information about the course motivation, structure, procedures, and policies. It will be assumed that all students have read and understand all of the material in the course syllabus. We will not waste lecture time repeating what is in the syllabus, so it is difficult to stress how important it is to read the entire syllabus!

2. Log into Piazza

We will be using Piazza for online discussion and most student/instructor communication. Both students officially enrolled and on the waitlist will be automatically added to the Piazza page for this course on Thursday, August 25th. As soon as you receive the welcome email, please log into Piazza to ensure that it is working.

3. Prepare for first quiz

There will be a short five-minute quiz at the very beginning of lecture on Monday, August 29th on the ECE 4750 collaboration policy as described in the course syllabus. You should read the course syllabus to prepare.

4. Work through lab tutorials

We are preparing four tutorials covering the Linux development environment, Git version control, the PyMTL Hardware Modeling Framework, and the Verilog Hardware Description Language. The tutorials have critical information on how to access the ECE computing resources, how to use GitHub/TravisCI, and how to manage your lab group. Please complete these tutorials as soon as they are posted on the public course website.

5. Attend discussion section on Friday in 203 Phillips Hall

Attendance at the weekly discussion sections is optional but strongly encouraged. This week we will be reviewing the basics of the PyMTL Hardware Modeling Framework we will be using in the lab assignments. Next week we will review the basics of the Verilog Hardware Modeling Language. The discussion section is on Friday from 2:30–3:20pm in 203 Phillips Hall.

6. Read Chapter 1 of Hennessy and Patterson

The course textbook is *"Computer Architecture: A Quantitative Approach, 5th Edition,"* by J. L. Hennessy and D. A. Patterson (Morgan Kaufmann, 2012). For your convenience, the first chapter is available at `http://www.csl.cornell.edu/courses/ece4750/readings/hennessy-ch1-book2012.pdf` (username and password given out in lecture).

7. Review background material as necessary

Students which are less confident of their mastery of the material covered in the pre-requisite courses should probably begin reviewing the material in *"Digital Design and Computer Architecture, 2nd Edition,"* by D. Harris and S. Harris (Morgan Kaufmann, 2012). Students who have never used Python before may want to spend additional time reviewing the optional textbook titled *"Think Python: How to Think Like a Computer Scientist"* by A. B. Downey (Green Tea Press, 2014). Students are not required to use Verilog hardware description language for the lab assignments. If a student has less experience working with Verilog but still wants to use this language, then they are strongly encouraged to read Chapter 4 in Harris and Harris on digital design with Verilog and/or to review the optional text *"Verilog HDL: A Guide to Digital Design and Synthesis, 2nd edition"* by S. Palnitkar (Prentice Hall, 2003). These materials are available on reserve at Uris Library, available on the public course webpage, or available for free to Cornell students as an e-book. See public course webpage for links.

8. Begin selecting a group for the lab assignments

The lab assignments are specifically designed to be a reasonable amount of work for three students working together. Students can either form their own group or have the instructor form a group for them. If you would like the instructor to form a group for you, then please submit a request using the online form located here `http://www.csl.cornell.edu/courses/ece4750/labgroup`. All requests must be submitted by 11:59pm on Wednesday, August 31st. Groups will be announced the following day. Only submit a request if you are formally enrolled in the course. You should complete the tutorials *and* you should start working on the first lab assignment even before groups are assigned!