ECE 2300
Digital Logic & Computer Organization
Spring 2018

Timing Analysis
Announcements

• Lab report guidelines are uploaded on CMS
  – As part of the assignment for Lab 3 report

• Lab 4(A) prelab due tomorrow
Synchronous Circuits

- The changes in the state of the memory elements are synchronized by a clock signal
  - All flip-flops (FFs) are synchronized to capture the inputs “simultaneously” on the clock tick

- Must ensure the output of the combinational logic has settled before the next clock tick
Review: Glitches in Synchronous Circuits

\[
\begin{align*}
X & \\
Y & \\
S & \\
S' & \\
S \cdot Y & \\
S' \cdot X & \\
F & \\
CLOCK & \\
\end{align*}
\]
Stable FF Situation

Flip-flop propagation delay (or clock-to-Q delay): the time it takes for the FF output to be stable after the clock edge
What if This Happens?

D2 input still transitioning

May capture neither HIGH nor LOW
Metastable State

- $Q$ stuck in the undefined region between 0 and 1
- Eventually moves to a stable state, but may take a while (metastable resolution time)
But What About This Situation?

Wrong value captured
Avoiding Timing Failure

• **Possible causes of metastability and wrong value capture**
  – Clock pulse that is too narrow
  – Input changes too soon before a clock edge
  – Input changes too soon after a clock edge

• **Avoid by meeting setup time, hold time, and minimum clock pulse width specifications**
Sequential Circuit Timing Analysis

• **Timing analysis** involves calculating the time delays between all FF pairs within the circuit.

• To determine the maximum operating frequency and ensure that setup time requirements are met:
  – The clock cannot be too fast.

• To ensure that hold time requirements are met:
  – The minimum propagation delay of the combinational logic (contamination delay) cannot be too small.
    – Independent of clock frequency.
Important Timing Parameters

CLOCK

- $t_{\text{setup}}$
- $t_{\text{hold}}$
- $t_{\text{clk}}$
- $t_{\text{HI}}$
- $t_{\text{L}}$
- $t_{\text{ffpd}}$
- $t_{\text{comb}}$

Combination logic
Setup Time Constraint

- $t_{\text{setup}}$ is the minimum amount of time before the triggering edge during which FF input must be stable.
Determining Clock Cycle Time

Every circuit path between every pair of FFs must satisfy the above equation to run the circuit at a frequency of $1/t_{\text{clk}}$

- **$t_{\text{ffpd(max)}} + t_{\text{comb(max)}} + t_{\text{setup}} \leq t_{\text{clk}}$**

- **The longest timing path (worst case) determines the maximum clock frequency**
  - Worst case temperature and voltage
  - Worst case manufacturing variations
Example: Setup Time Calculations

<table>
<thead>
<tr>
<th></th>
<th>Prop Delay (ns)</th>
<th>Setup Time (ns)</th>
<th>Hold Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>min  max</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF</td>
<td>1 7</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>Comb</td>
<td>3 9</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

- What’s the best achievable cycle time?
Example: Setup Time Calculations

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</tr>
<tr>
<td>FF</td>
<td>1</td>
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<td>3</td>
</tr>
<tr>
<td>Comb</td>
<td>3</td>
<td>9</td>
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- \( t_{\text{clk}} \geq t_{\text{ffpd(max)}} + t_{\text{comb(max)}} + t_{\text{setup}} = 7 + 9 + 3 = 19 \text{ns} \)
Hold Time Constraint

- \( t_{\text{hold}} \) is the minimum amount of time after the triggering edge during which FF input must remain stable
  - Otherwise, the receiving flip-flop may be contaminated with an unexpected value

- Need to consider minimum propagation delays (contamination delays) for hold time calculations
  \[
  t_{\text{ffpd}(\text{min})} + t_{\text{comb}(\text{min})} \geq t_{\text{hold}}
  \]
Example: Hold Time Constraint

Hold time windows ($t_{hold}$)
D2 must be held stable for FF2

$t_{ffpd}(\text{min}) + t_{comb}(\text{min}) = t_{ffpd}(\text{min}) + 0 \geq t_{hold}$
Example: Hold Time Calculations

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<td>FF</td>
<td>1 min, 7 max</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>Comb</td>
<td>3 min, 9 max</td>
<td>-</td>
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</table>

- Hold time at FF2 met?
Clock Skew Complicates Matters Further

- Clock may not reach all flip-flops simultaneously

\[
\text{CLK1} \quad \text{CLK2} \\
\text{FF1} \quad \text{combinational logic} \quad \text{FF2}
\]

\[\text{CLK1} \quad \text{CLK2} \quad \text{CLCOK} \]

\(t_{\text{skew}}\) : Maximum clock skew
\(t_{\text{skew(min)}}\) : Minimum clock skew
Cycle Time With Clock Skew

IN  FF1  Q1  Combinalional logic  FF2  D2  CLOCK
CLK1 [long wire]  CLK2

IN
CLK1 (delayed)
Q1 (delayed)
D2 (delayed)
CLK2

\(t_{skew}\)
\(t_{setup}\)
Negative Clock Skew

Sending FF receives clock later than receiving FF

$t_{ffpd(max)} + t_{comb(max)} + t_{setup} \leq t_{clk} - t_{skew(max)}$

Harmful skew for meeting setup time constraint
Positive Clock Skew

Receiving FF receives clock later than sending FF

\[ t_{ffpd(\text{max})} + t_{\text{comb(\text{max})}} + t_{\text{setup}} \leq t_{\text{clk}} + t_{\text{skew(min)}} \]

Beneficial skew for meeting setup time constraint
Hold Time With Positive Clock Skew

Receiving FF receives clock later than sending FF

\[ t_{ffpd(min)} + t_{comb(min)} \geq t_{hold} + t_{skew(max)} \]

Harmful skew for meeting hold time constraint
Hold Time With Negative Clock Skew

What if sending FF receives clock later than receiving FF?

\[ t_{ffpd(min)} + t_{comb(min)} \geq t_{hold} - t_{skew(min)} \]

Beneficial skew for meeting hold time constraint
Example: Setup Analysis with Clock Skew

Clock may arrive at FF1 up to 1ns later than FF2

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- What’s the best achievable cycle time?

\[
t_{\text{ffpd(max)}} + t_{\text{comb(max)}} + t_{\text{setup}} \leq t_{\text{clk}} - t_{\text{skew(max)}}
\]

\[
t_{\text{clk}} \geq 7 + 9 + 3 + 1 = 20\text{ns}
\]
Before Next Class

- H&H 5.1-5.2.3, 5.5

Next Time

Binary Arithmetic