

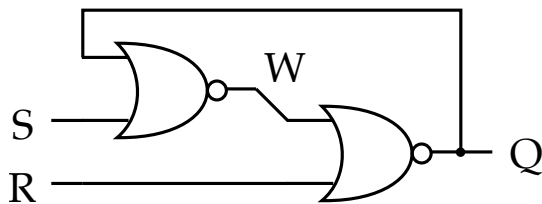
ECE 2300 Digital Logic and Computer Organization, Fall 2026

Lab 3B: Worksheet

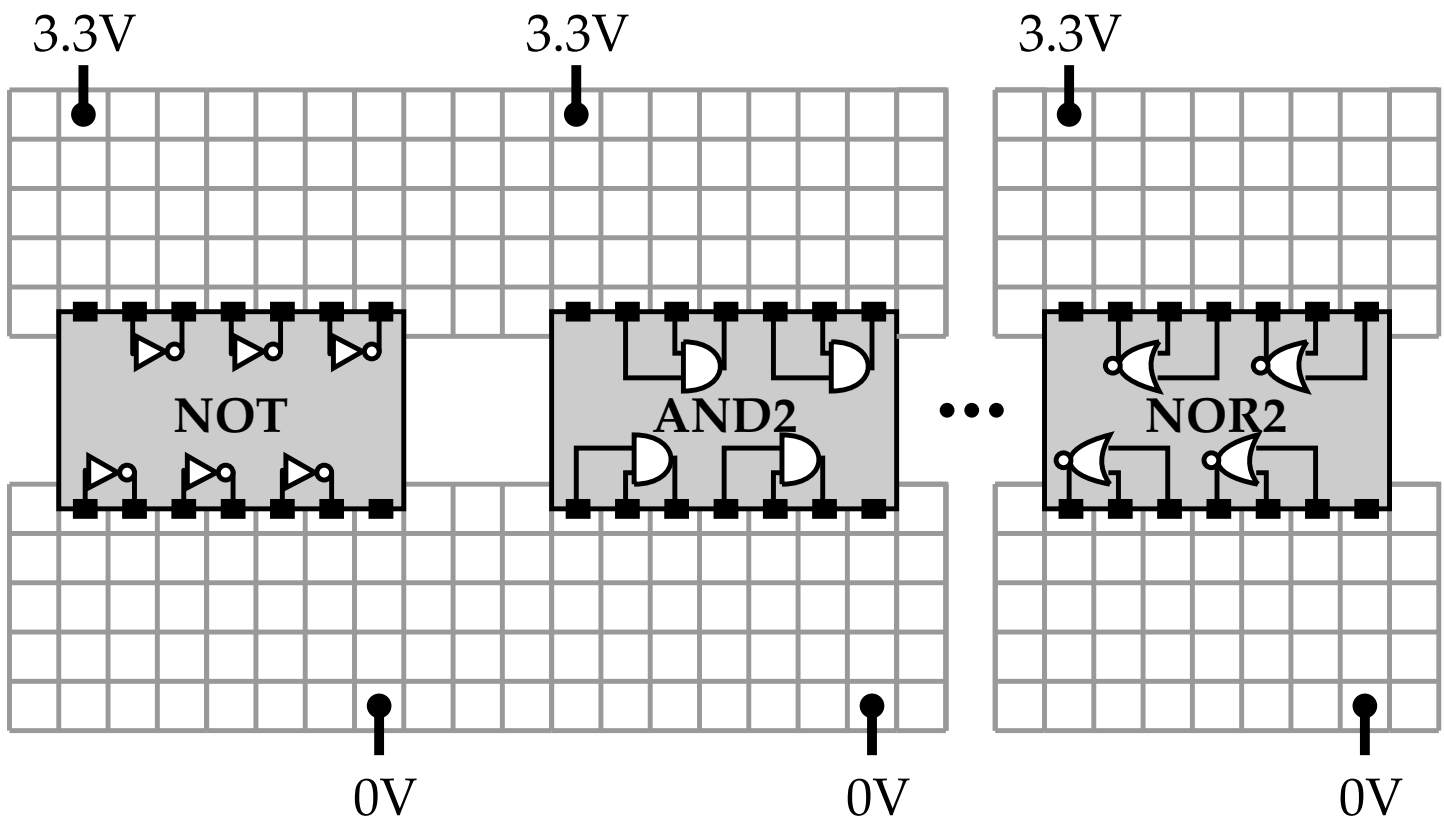
Please use one worksheet per group! You only need the worksheet to complete the lab check-off tasks. You do not need to turn the worksheet in, nor save it for your report.

SR Latch

The implementation for a SR latch is shown below. Fill in the truth table for a SR latch.

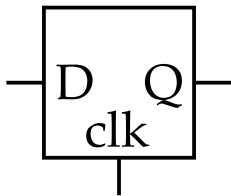
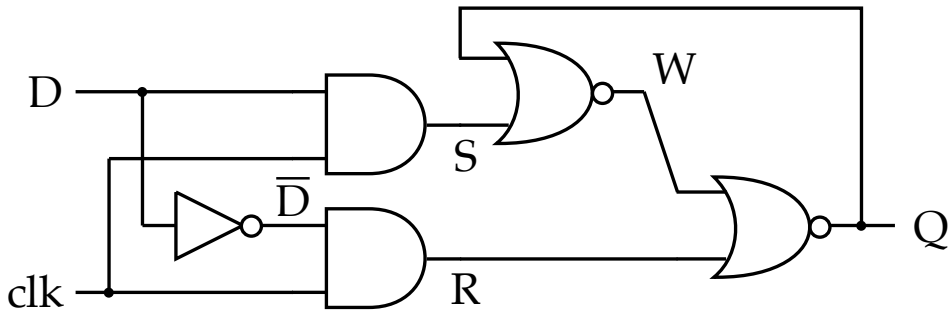


S	R	W	Q
0	0		
0	1		
1	0		
1	1		

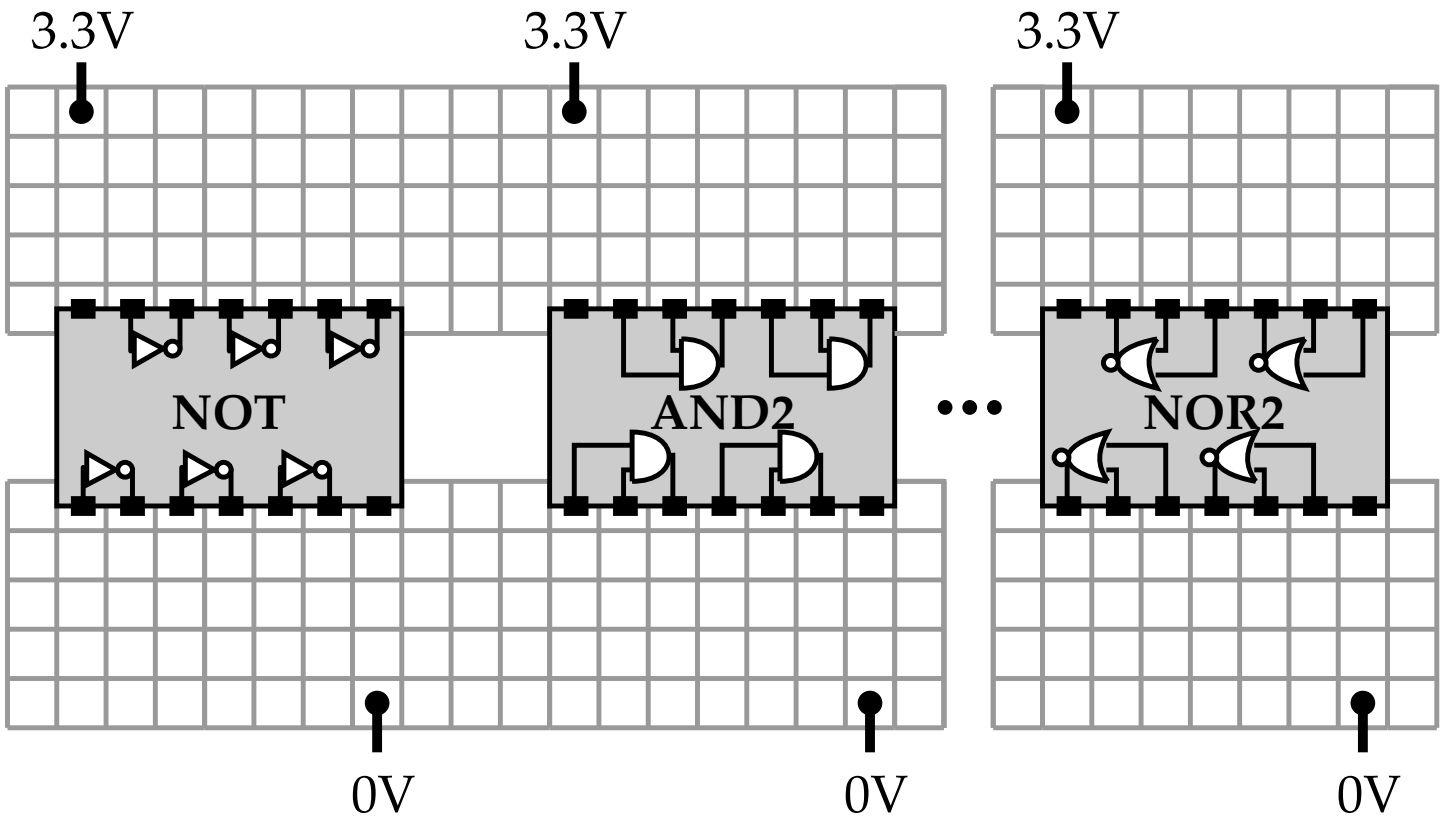


D Latch

The implementation for a D latch is shown below. Fill in the truth table for a D latch.



clk	D	$\overline{D}$	S	R	W	Q
0	0					
0	1					
1	0					
1	1					



Sequential Pair/Triple Detector

Annotate the block diagram for the sequential pair/triple detector with the actual delays in nanoseconds for the clock-to-q propagation delay, combinational logic propagation delay, and the setup time.

