

ECE 2300 Digital Logic and Computer Organization, Fall 2026

Lab 2D: Worksheet

Please use one worksheet per group! You will need to include the annotated actual critical path diagrams in your datasheets!

Predicted Critical Path for Ripple-Carry Adder

Draw your prediction of the critical path for the ripple-carry adder.

Predicted Critical Path for Carry-Select Adder

Draw your prediction of the critical path for the carry-select adder.

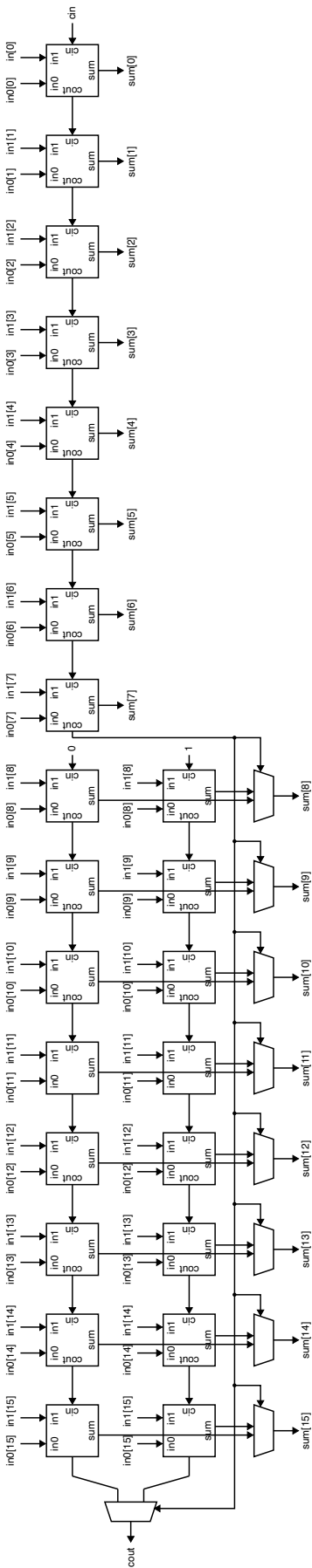
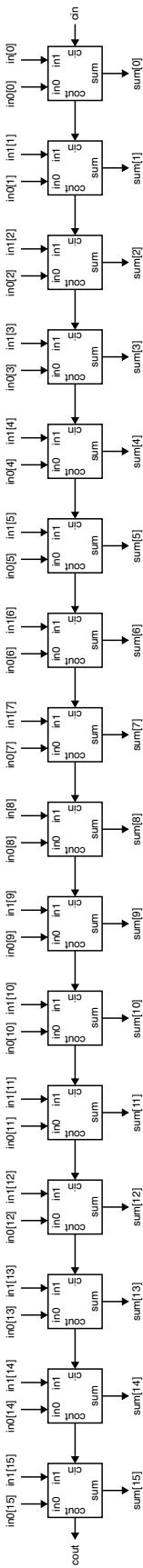
Actual Critical Path for Ripple-Carry Adder

Draw the actual critical path for the ripple-carry adder. Label the first four of the full adders along the critical path with their corresponding delay using the timing report (you do not need to label all of the full adders!). You can use SHIFT-select to highlight multiple *Incr* cells in the timing report and then hover over these highlighted cells to determine the sum of the delay through the corresponding elements. So you can highlight the *Incr* cells from a full adder's carry in to its carry out to get the total delay through that full adder. Include buffering delay between full adders as part of the delay of the full adder. Label the delay to get from the FPGA input pin to the ripple-carry adder and the delay to get from the ripple-carry adder to the FPGA output pin.

Actual Critical Path for Carry-Select Adder

Draw the actual critical path for the carry-select adder. Label the first four of the full adders and the 1-bit multiplexers along the critical path with their corresponding delay using the timing report (you do not need to label every full adder along the path!). You can use SHIFT-select to highlight multiple *Incr* cells in the timing report and then hover over these highlighted cells to determine the sum of the delay through the corresponding elements. So you can highlight the *Incr* cells from a full adder's carry in to its carry out to get the total delay through that full adder. Include buffering delay between full adders as part of the delay of the full adder. Label the delay to get from the FPGA input pin to the carry-select adder and the delay to get from the carry-select adder to the FPGA output pin.

Predicted Critical Paths



Actual Critical Paths

