ECE 2300 Digital Logic and Computer Organization, Fall 2026
Lab 1B: Worksheet

NAME: _____ NetID: _____

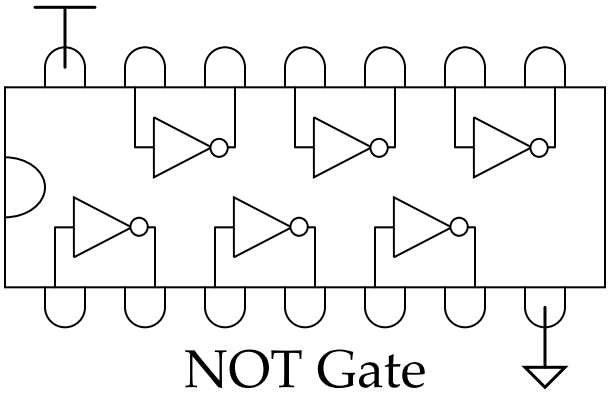
Combinational Logic IC Delays

Fill in the following table using the combinational logic IC datasheets.

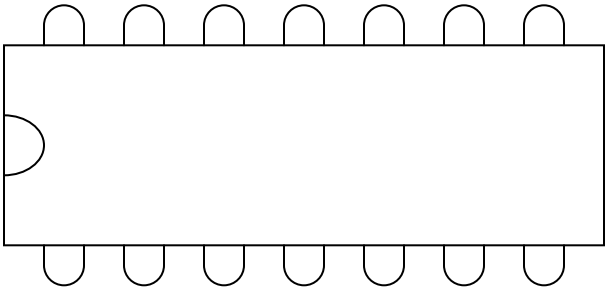
Logic Gate	Propagation Delay (ns)	Contamination Delay (ns)
NOT		
AND		
OR		
XOR		
NOR		

Combinational Logic IC Pin Outs

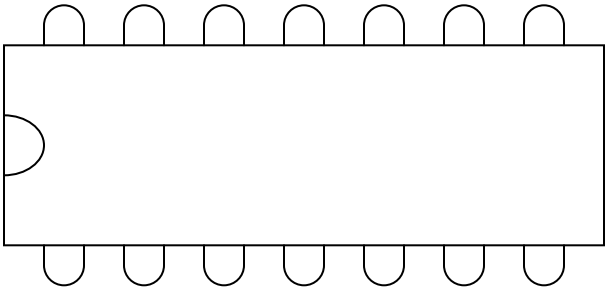
Draw how the logic gates in each combinational logic IC connect to the pins. We have completed the NOT IC for you. Notice how we are using the symbols for VDD and ground to indicate which pins serve these purposes.a



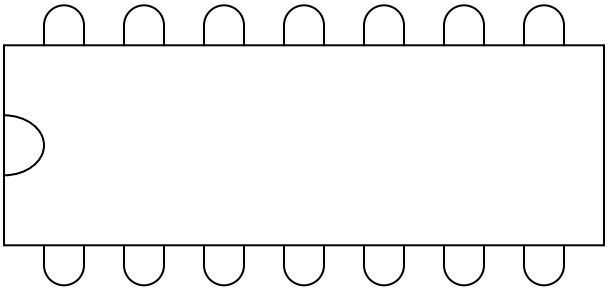
NOT Gate



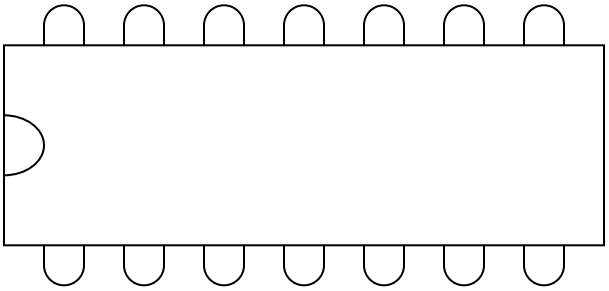
AND2 Gate



OR2 Gate



XOR2 Gate



NOR2 Gate

Pair/Triple Detector Truth Table

Complete the truth table for the pair/triple detector including all intermedaite signals.

in0	in1	in2	W	X	y	out
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

Pair/Triple Detector Breadboard Planning

Draw lines to plan how you want to wire up the pair/triple on the breadboard. Think carefully about how to avoid too many crossing wires and wires too close together.