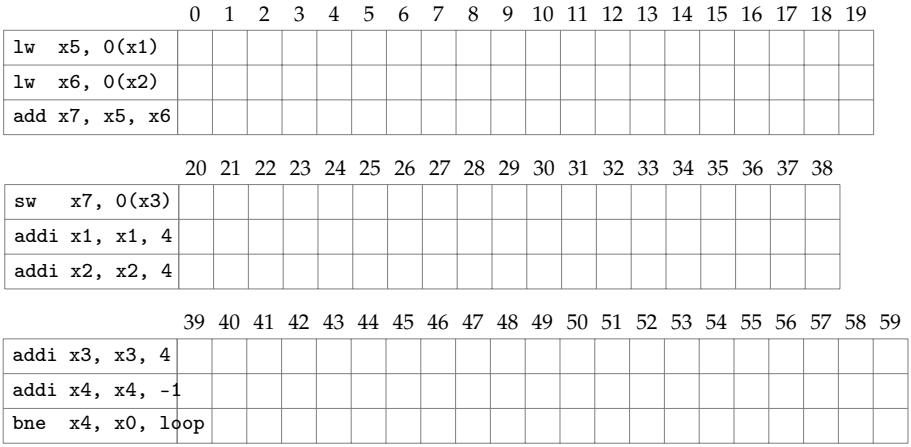
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
`lw  x5, 0(x1)`																		
`lw  x6, 0(x2)`																		
`add x7, x5, x6`																		
`sw  x7, 0(x3)`																		

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
`addi x1, x1, 4`																				
`addi x2, x2, 4`																				
`addi x3, x3, 4`																				
`addi x4, x4, -1`																				
`bne  x4, x0, loop`																				

Results for vector-vector-add micro-benchmark

Microarchitecture	Inst/Prog	Cycle/Inst	Time/Cycle	Exec Time
Single-Cycle	576	1.0	366 τ	211 kτ
15-State Multi-Cycle				



Results for vector-vector-add micro-benchmark

Microarchitecture	Inst/Prog	Cycle/Inst	Time/Cycle	Exec Time
Single-Cycle	576	1.0	366 τ	211 kτ
15-State Multi-Cycle	576	4.2	151 τ	367 kτ
63-State Multi-Cycle				

4. TinyRV1 Embedded System

- Memory-mapped input/output enables multi-cycle processor to external devices by reading/writing memory addresses
- Supporting the memory wait signal simply involves staying in specific stages if the memory is waiting
  - Need to integrate memory wait signal into specific control signals creating a Mealy FSM (i.e., reg en, rf wen)
- Now possible to support physical memory with sequential read