ECE 2300 Digital Logic and Computer Organization Fall 2026

Topic 8: Sequential Building Blocks

School of Electrical and Computer Engineering
Cornell University

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1 Counters **3**

2 Clock Dividers **5**

3 Shift Registers **7**

4 Synchronizers **8**

5 Sequential Arithmetic **9**

5.1. Single-Cycle Quad Adder 14

5.2. Multi-Cycle Quad Adder 15

5.3. Pipelined Quad Adder 16

5.4. Tree-Based Quad Adders 17

6 Memory Arrays **19**

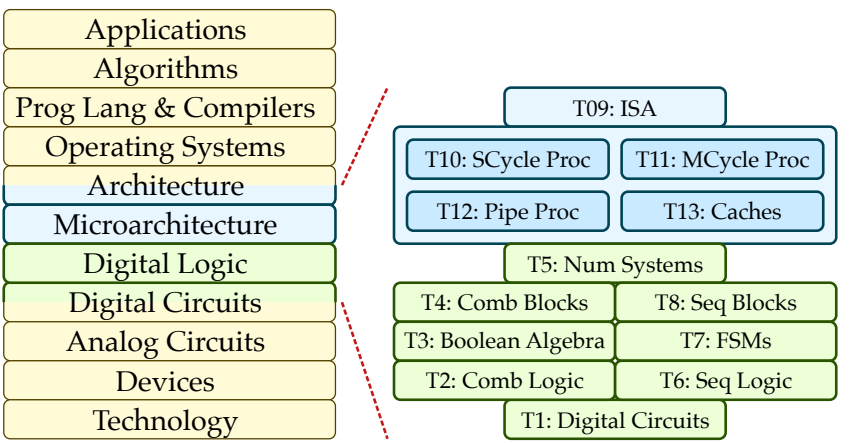
6.1. Read-Only Memories 20

6.2. Register Files 21

6.3. Static Random Access Memories (SRAM) 23
6.4. Dynamic Random Access Memories (DRAM) 24
6.5. Comparing Memory Arrays 25

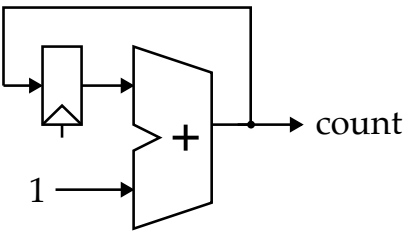
7 Programmable Logic **26**

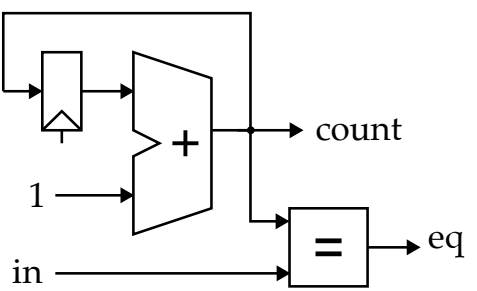
7.1. Programmable Truth Tables 26
7.2. Field Programmable Gate Arrays 28



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1. Counters





Summay of Kinds of Counters

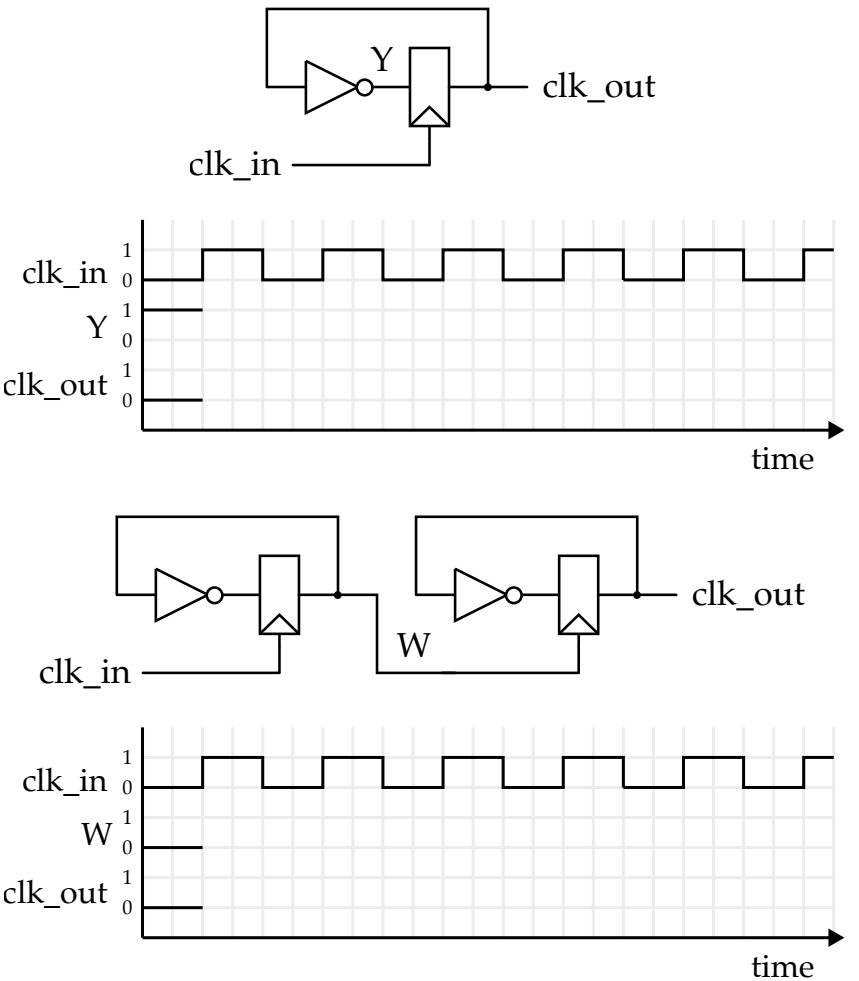
- Counters with enable and/or clear
- Up, down, up/down counters
- Variable increment counters (count by more than one)
- Variable start counters (control starting value)
- Decade counters (counts to ten then wraps around)
- Saturating counters (does not wrap around)

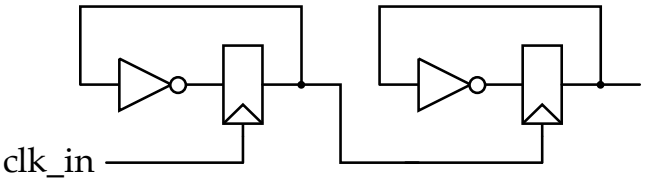
Implement an increment-by-one clearable up/down counter.

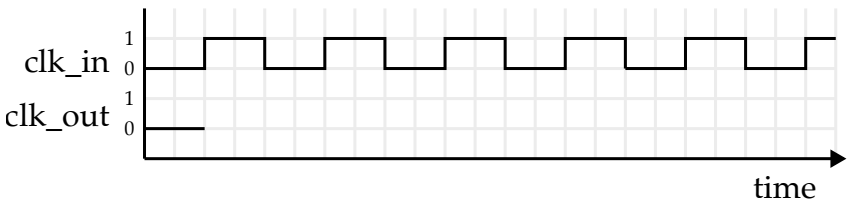
- clear: if 1 then clear counter, counter outputs zero following cycle
- updown: if 1 then count up by one, if 0 then count down by 1
- done: should be 1 if counter is at zero on current cycle
- counter should roll-over

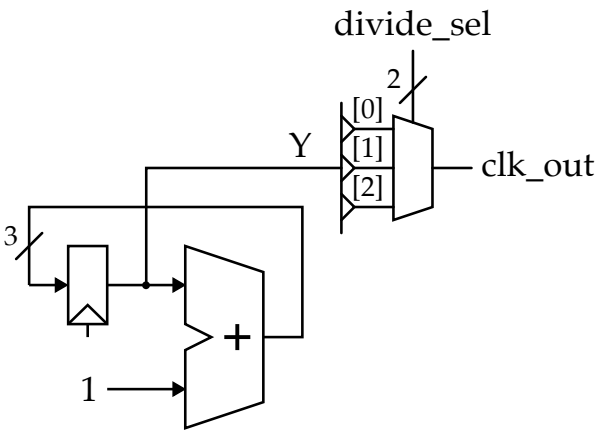
Find the critical path and short path. Derive the setup time constraint and hold time constraint as a function of the flip-flop timing parameters and the combinational block delays for these paths.

2. Clock Dividers







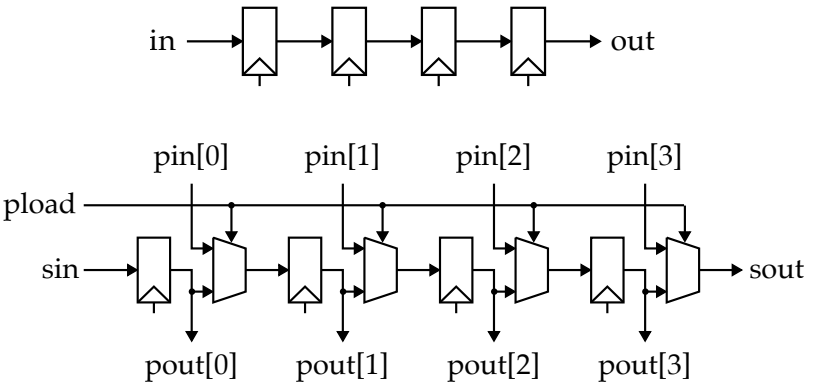


$Y[2]$	$Y[1]$	$Y[0]$
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Summay of Kinds of Clock Dividers

- Fixed power-of-two clock divider
- Configurable power-of-two clock divider
- Fractional clock dividers
- Glitchless dynamic clock dividers

3. Shift Registers

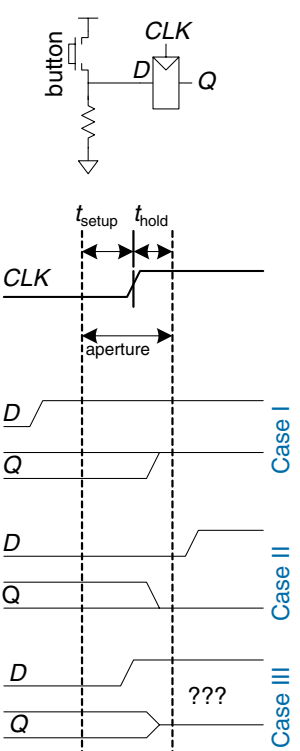


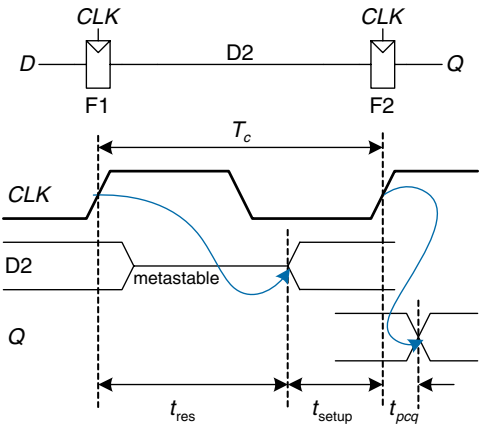
Summay of Kinds of Shift Registers

- Serial-in, serial-out shift registers
- Parallel-in, serial-out shift registers
- Serial-out, parallel-out shift registers
- Bi-directional shifters (can shift left and shift right)
- Variable shift registers (can vary shift amount)

Find the critical path and short path. Derive the setup time constraint and hold time constraint as a function of the flip-flop timing parameters and the combinational block delays for these paths.

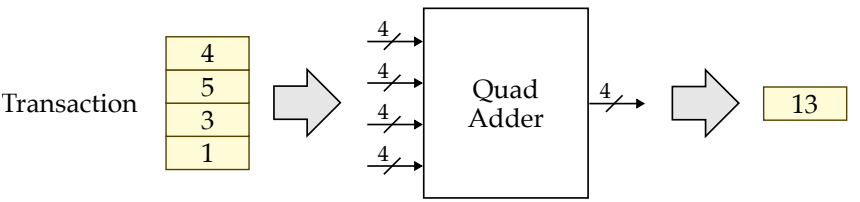
4. Synchronizers





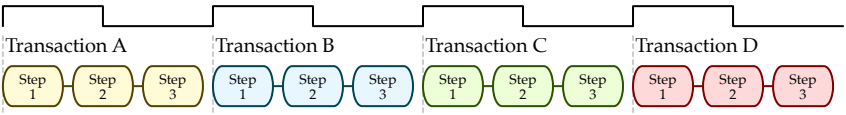
5. Sequential Arithmetic

- A quad adder adds four 4-bit input values to produce one 4-bit output value (ignore overflow)

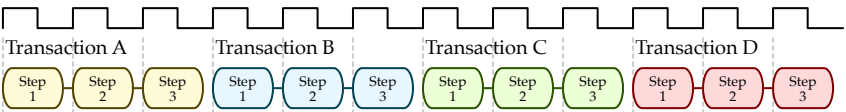


- A *transaction* involves processing a block of four 4-bit values
- The quad adder executes a *sequence* of transactions
- Each *transaction* can be broken down into three steps
  - Step 1. Add element 0 and element 1
  - Step 2. Add element 2 to the result of step 1
  - Step 3. Add element 3 to the result of step 2

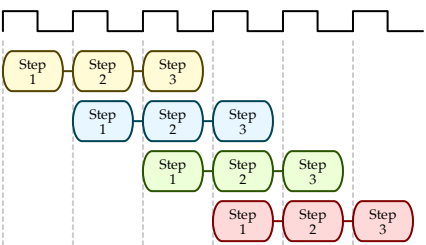
Single-Cycle Quad Adder



Multi-Cycle Quad Adder



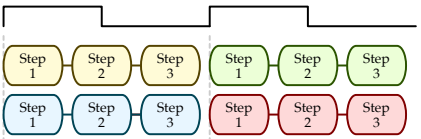
Pipelined Quad Adder



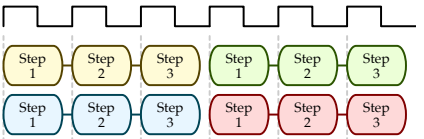
$$\frac{\text{Time}}{\text{Sequence}} = \frac{\text{Transactions}}{\text{Sequence}} \times \frac{\text{Avg Cycles}}{\text{Transaction}} \times \frac{\text{Time}}{\text{Cycle}}$$

	Area	$\frac{\text{Avg Cycles}}{\text{Trans}}$	$\frac{\text{Time}}{\text{Cycle}}$
Single-Cycle	medium	1	long
Multi-Cycle	small	3	short
Pipelined	large	≈ 1	short

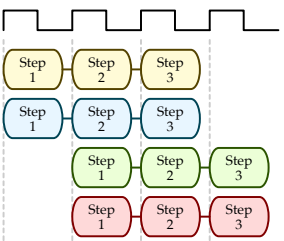
Parallel Single-Cycle Quad Adder



Parallel Multi-Cycle Quad Adder



Parallel Pipelined Quad Adder

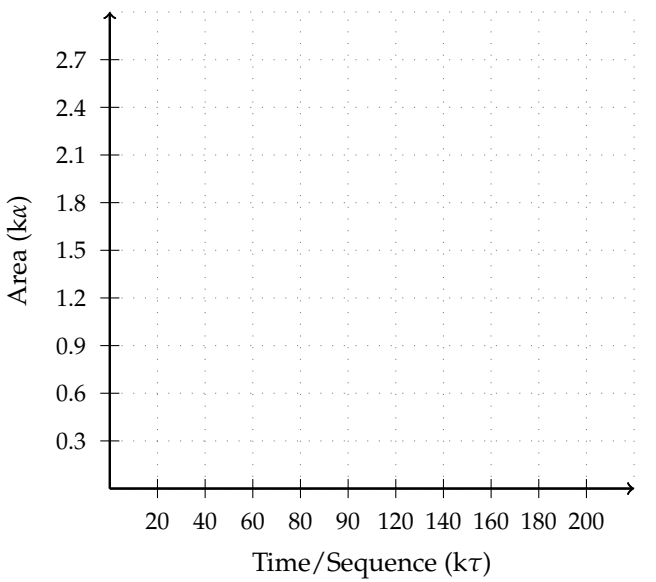


$$\frac{\text{Time}}{\text{Sequence}} = \frac{\text{Transactions}}{\text{Sequence}} \times \frac{\text{Avg Cycles}}{\text{Transaction}} \times \frac{\text{Time}}{\text{Cycle}}$$

	Area	$\frac{\text{Avg Cycles}}{\text{Trans}}$	$\frac{\text{Time}}{\text{Cycle}}$
Parallel Single-Cycle	2× Single-Cycle	0.5	long
Parallel Multi-Cycle	2× Multi-Cycle	1.5	short
Parallel Pipelined	2× Pipelined	≈0.5	short

- Our goal is to do a quantitative comparative analysis of area and performance across six different implementations

	Area ($k\alpha$)	$\frac{\text{Trans}}{\text{Sequence}}$	$\frac{\text{Avg Cycles}}{\text{Trans}}$	$\frac{\text{Time}}{\text{Cycle}}$ (τ)	$\frac{\text{Time}}{\text{Sequence}}$ ($k\tau$)
Single-Cycle		100			
Multi-Cycle		100			
Pipelined		100			
Parallel SCycle		100			
Parallel MCycle		100			
Parallel Pipe		100			



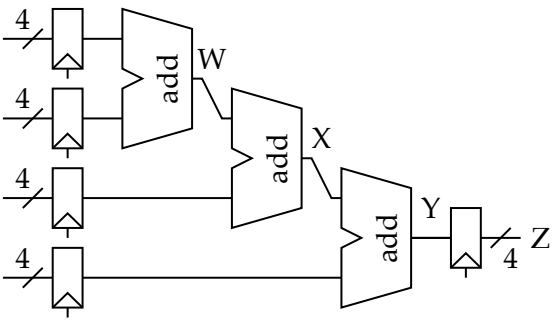
Path-Independent Constant Delay Model

	t_{pd}
4-bit 2-to-1 Mux	8τ
4-bit 3-to-1 Mux	10τ
4-bit Adder	44τ
4-bit Register (t_{cq})	9τ
4-bit Register (t_{setup})	10τ

Area Model

	Area
4-bit 2-to-1 Mux	44α
4-bit 3-to-1 Mux	76α
4-bit Adder	124α
4-bit Register	108α

5.1. Single-Cycle Quad Adder



Area

Time/Cycle

Simulation Table

Cycle	Input	After Reg	W	X	Y	Z
0	A: 3, 1, 2, 0					
1	B: 5, 4, 0, 6					
2	C: 4, 5, 3, 1					
3	D: 2, 3, 5, 4					
4						
5						

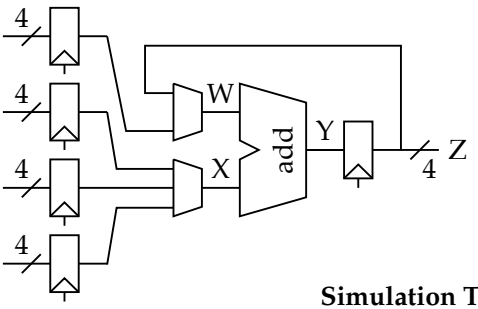
Transaction Diagram

	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Transaction A														
Transaction B														
Transaction C														
Transaction D														

5.2. Multi-Cycle Quad Adder

Area

Time/Cycle



Simulation Table

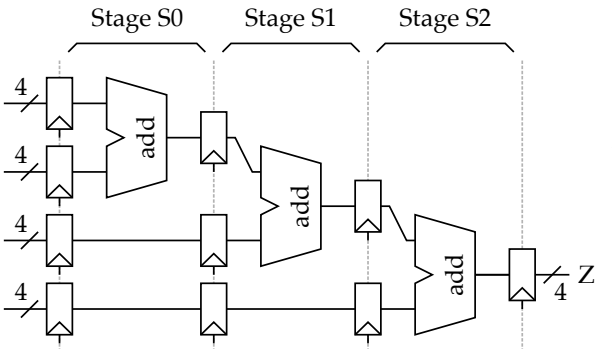
Cycle	Input	After Reg	W	X	Y	Z
0	A: 3, 1, 2, 0					
1						
2						
3	B: 5, 4, 0, 6					
4						
5						
6						

Transaction Diagram

	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Transaction A														
Transaction B														
Transaction C														
Transaction D														

5.3. Pipelined Quad Adder

Area



Time/Cycle

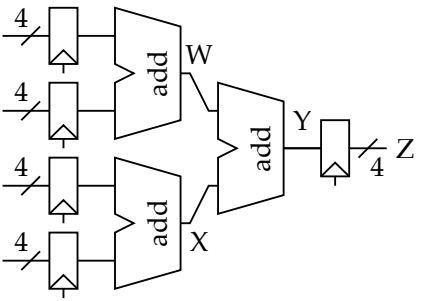
Simulation Table

Cycle	Input	Stage S0	Stage S1	Stage S2	Z
0	A: 3, 1, 2, 0				
1	B: 5, 4, 0, 6				
2	C: 4, 5, 3, 1				
3	D: 2, 3, 5, 4				
4					

Transaction Diagram

	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Transaction A														
Transaction B														
Transaction C														
Transaction D														

5.4. Tree-Based Quad Adders



Area

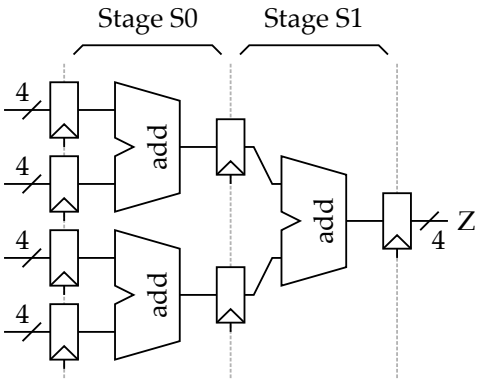
Time/Cycle

Simulation Table

Cycle	Input	After Reg	W	X	Y	Z
0	A: 3, 1, 2, 0					
1	B: 5, 4, 0, 6					
2	C: 4, 5, 3, 1					
3	D: 2, 3, 5, 4					
4						
5						

Transaction Diagram

	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Transaction A														
Transaction B														
Transaction C														
Transaction D														



Area

Time/Cycle

Simulation Table

Cycle	Input	Stage S0	Stage S1	Z
0	A: 3, 1, 2, 0			
1	B: 5, 4, 0, 6			
2	C: 4, 5, 3, 1			
3	D: 2, 3, 5, 4			
4				

Transaction Diagram

	0	1	2	3	4	5	6	7	8	9	10	11	12	13
Transaction A														
Transaction B														
Transaction C														
Transaction D														