ECE 2300 Digital Logic and Computer Organization

Topic 4: Combinational Building Blocks

http://www.csl.cornell.edu/courses/ece2300
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List of Problems

Problem 1. Ripple Carry, Carry-Select, and Carry-Lookahead Adder Comparison

In this problem, we will implement and compare three different adder designs: *Ripple Carry*, *Carry-Select*, and *Carry-Lookahead*. Use the following gates with their corresponding delay and area parameters:

Gate	t_{pd}	t_{cd}	Area
NOT	1τ	1τ	1α
AND2	3τ	1τ	3α
OR2	4τ	1τ	4α
XOR2	7τ	1τ	7α

Part 1.A Ripple Carry Adder

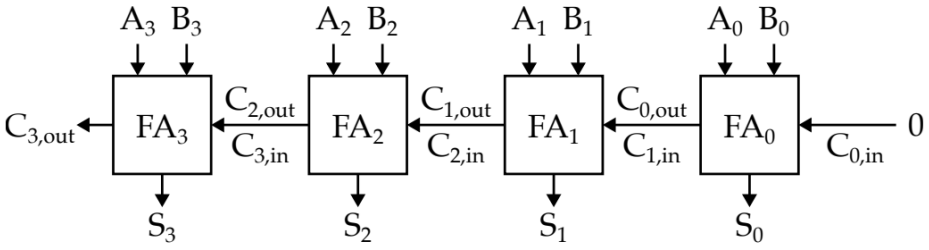
We will start with the *ripple carry adder*. As a first step, we need to inspect the *full adder* module. **Draw the gate network of a full adder from lecture.**

Fill in the table with the propagation and contamination delay of every path through the full adder (utilizing the previously stated timing parameters).

Path	Propagation Delay	Contamination Delay

Compute the area of one full adder module in area units α.

Next, we will build a four-bit ripple carry adder. For this, we connect four full adder modules (see Figure below). **Draw the critical and shortest path on the block diagram. From which port do the paths start and end? Calculate the critical path and shortest path delay in units of τ.**



Compute the area of the four-bit ripple carry adder in area units α (without any optimizations in FA0). How much could the area be reduced by optimizing FA0 for $C_{in} = 0$? What module would FA0 be after optimization?

Derive equations for critical path delay and area for the ripple carry adder as a function of the number of bits b. Assume the full adders are not optimized due to C_{in} of the adder being constant.

Jamayne's Solution

`https://vod.video.cornell.edu/id/1_1vwcshcg`

Part 1.B Carry-Select Adder

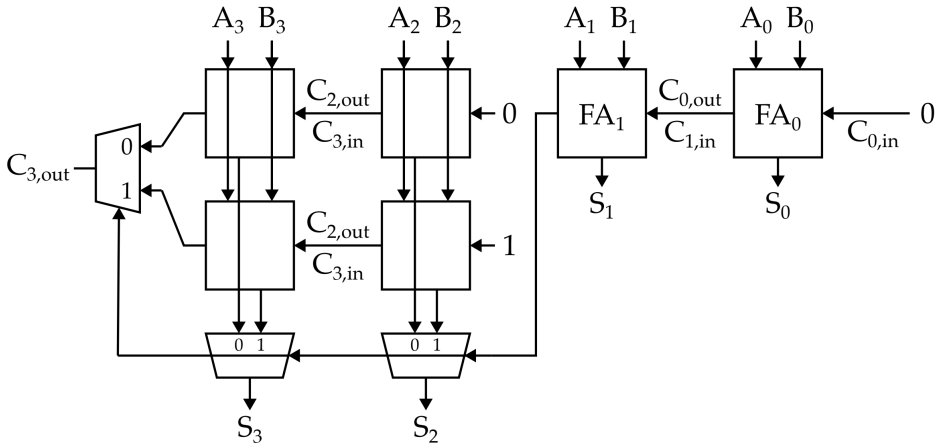
Next, we will investigate the *carry-select adder*. For this design we need (besides the full adder module) the 2-to-1 multiplexor module. **Draw the gate network of the 2-to-1 multiplexor module utilizing the gates from the table.**

Fill in the table with the propagation and contamination delay of every path through the 2-to-1 multiplexor (utilizing the previously stated timing parameters).

Path	Propagation Delay	Contamination Delay

Compute the area of one 2-to-1 multiplexor module in area units α.

We implement a four-bit carry-select adder with a block size of two bits (see Figure below). **Draw the critical and shortest path on the block diagram. From which port do the paths start and end? Calculate the critical path and shortest path delay in units of τ.**

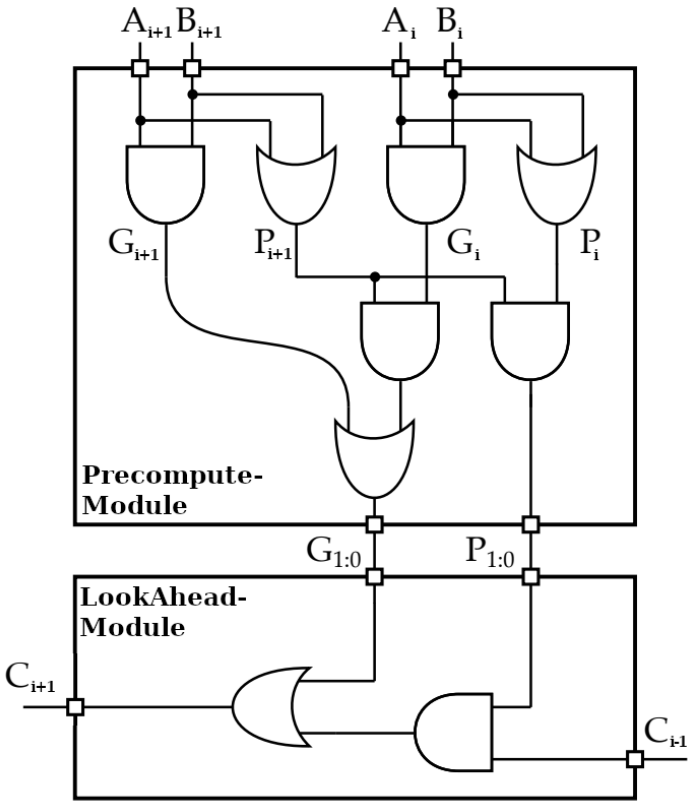


Compute the area of the four-bit carry-select adder in area units α (without optimizing the full adders with constant carry-in).

Derive equations for critical path delay and area for the carry-select adder as a function of the number of bits b. Assume b is even, the carry-select adder always divides the number of bits in half, and the full adders are not optimized due to C_{in} of the adder being constant.

Part 1.C Carry-Lookahead Adder

Lastly, we will examine the *carry-lookahead adder*. This architecture accelerates the carry-chain by pre-computing as much as possible (precompute-module). Afterwards, when the input-carry becomes available, the carry can be quickly generated (lookahead-module).

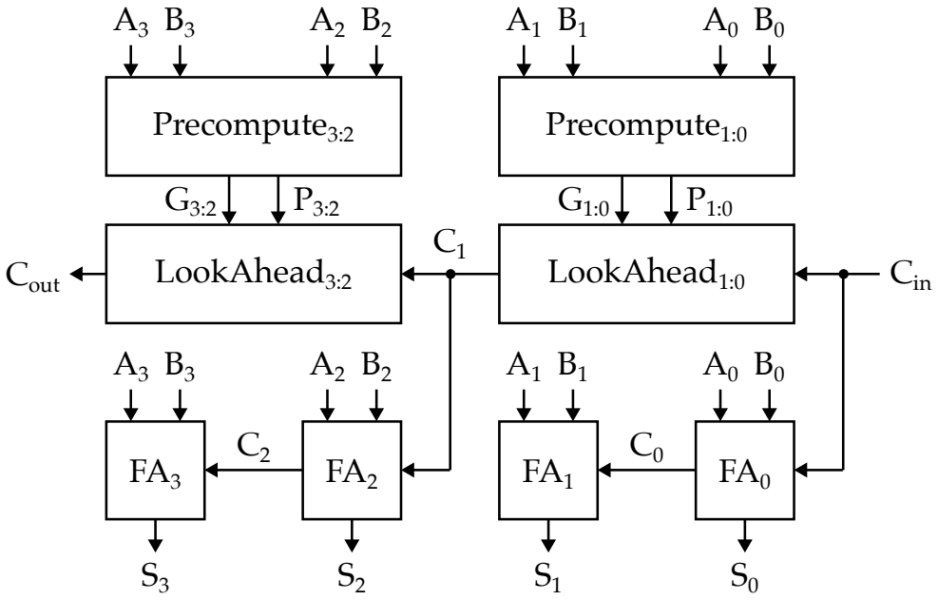


Fill in the table with the propagation and contamination delay of every path through the system containing both the precompute and look-ahead module (utilizing the previously stated timing parameters).

Path	Propagation Delay	Contamination Delay

Compute the area of one system containing both the precompute and look-ahead module in area units α.

We implement a four-bit carry-lookahead adder with a block size of two bits (see Figure below). **Draw the critical and shortest path on the block diagram. From which ports do the paths start and end? Calculate the critical path and shortest path delay in units of τ.**

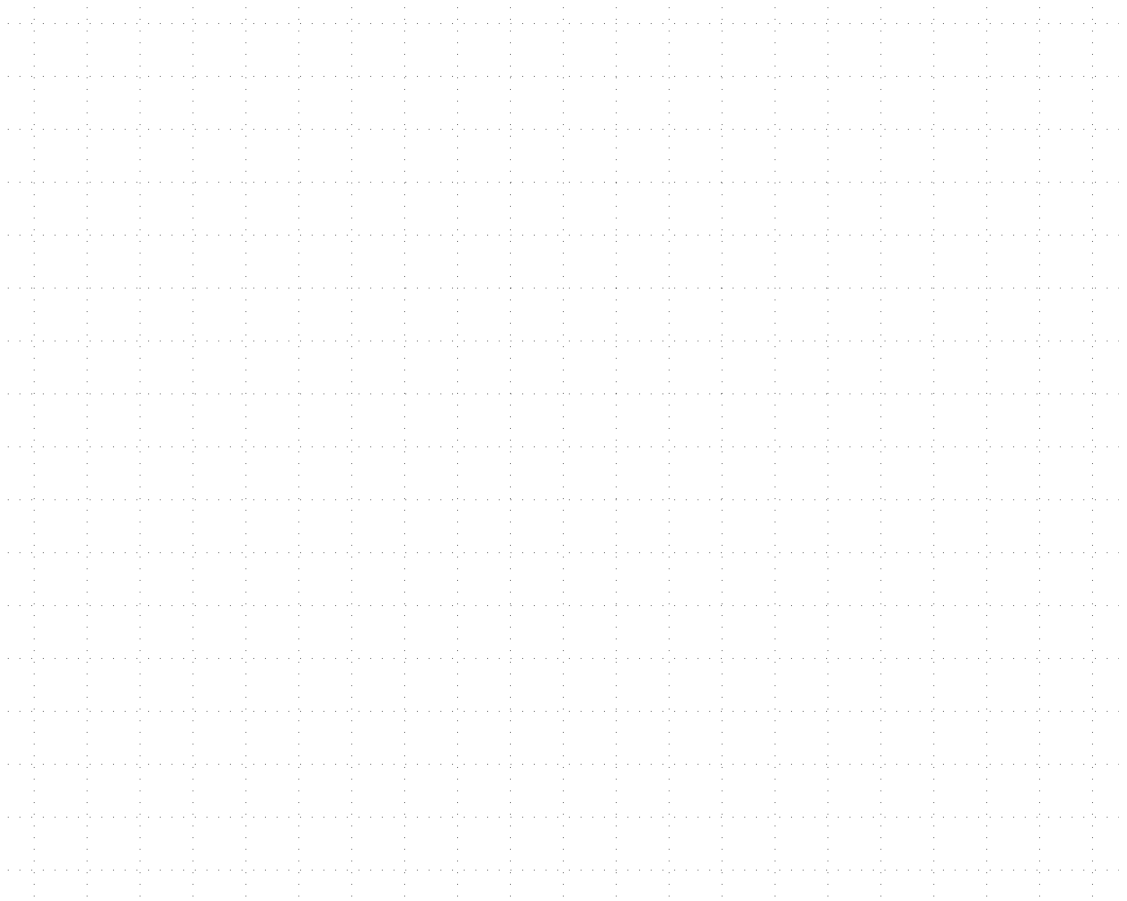


Compute the area of the four-bit carry-lookahead adder in area units α (without optimizing the submodules any further).

Derive equations for critical path delay and area for the carry-lookahead adder (with a block size of two bits) as a function of the number of bits b. Assume b is even and equal or greater than 4. Furthermore, the submodules are not further optimized.

Part 1.D Comparative Analysis

Create a Pareto frontier plot of the three adder designs. *Note: X-Axis is area and Y-Axis is critical path delay.*



Which adder would you choose and why? How would the bit-length of your operands impact your decision?