ECE 2300 Digital Logic and Computer Organization
Topic 3: Boolean Algebra

`http://www.csl.cornell.edu/courses/ece2300`
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List of Problems

Problem 1. From Boolean Equation to Transistor Schematics

Draw the transistor schematics for the following boolean equations. Afterwards, complete the truth tables for the boolean equations (Y_{eq}) and transistor schematics (Y_{schem}). Check for identical output.

Part 1.A Boolean Equation 1

$$Y = \overline{(A+B)C}$$

A	B	C	Y_{eq}	Y_{schem}
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Part 1.B Boolean Equation 2

$$Y = AB + C$$

A	B	C	Y_{eq}	Y_{schem}
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Problem 2. Comparing Different Implementations of the Same Boolean Equation

In this problem, we will develop multiple gate level networks and corresponding transistor schematics for the same boolean equation (below) and compare their area.

$$Y = \overline{AB + CD}$$

Part 2.A Truth Table

First, complete the truth table for the boolean equation (column Y_{eq}).

A	B	C	D	Y_{eq}	Y_{impl1}	Y_{impl2}	Y_{impl3}
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

Part 2.B Implementation IMPL1

Draw the gate network for the boolean equation using NAND2, NOR2, and INV gates. Implement it according the following boolean equation, which is a tranformation from the previous formula. **Afterwards, draw the corresponding transistor schematic. Check for the correct behavior by filling out the truth table (column $\mathbf{Y_{impl1}}$) according to your transistor circuit.**

$$Y = \overline{\overline{\overline{AB}} + \overline{\overline{CD}}}$$

Gate-level network:

Transistor schematic:

Part 2.C Implementation IMPL2

Reduce the number of needed gates by utilizing *De Morgan's Theorem*. Describe the optimization.

Draw the corresponding gate network using NAND2, NOR2, and INV gates. Afterwards, draw the corresponding transistor schematic. Check for the correct behavior by filling out the truth table (column Y_{impl2}) according to your transistor circuit.

Gate-level network:

Transistor schematic:

Part 2.D Implementation IMPL3

We are considering adding a module for this boolean expression to our primitive gate set. Draw the specialized transistor schematic from the original boolean equation. Check for the correct behavior by filling out the truth table (column Y_{impl3}) according to your transistor circuit.

Part 2.E Comparable Analysis

Determine and compare the area of all three transistor circuits in abstract transistor units.

Problem 3. Karnaugh Map

Consider the following Boolean equation with four input variables (A, B, C, D) and one output variable (Y).

$$Y = \overline{A}\,\overline{B}\,\overline{C}D + ABCD + A\overline{B}CD + A\overline{B}C\overline{D}$$

Is this Boolean equation in *canonical sum-of-products* or *minimal sum-of-products form*? Why?

Complete the truth table for the Boolean equation. Furthermore, mark the following don't care combinations: $\overline{A}\,\overline{B}CD$, $A\overline{B}\,\overline{C}D$, $ABC\overline{D}$, $\overline{A}B\overline{C}\,\overline{D}$.

A	B	C	D	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Draw the gate network for the *canonical SOP*. Assume the don't care combinations to be zero and to have access to both normal and inverted signal for each input.

Optimize the given Boolean equation with its don't care combinations utilizing a Karnaugh Map.

CD \ AB	00	01	11	10
00				
01				
11				
10				

Write the Boolean equation in *minimal sum-of-products form* derived using the Karnaugh map in the space below.

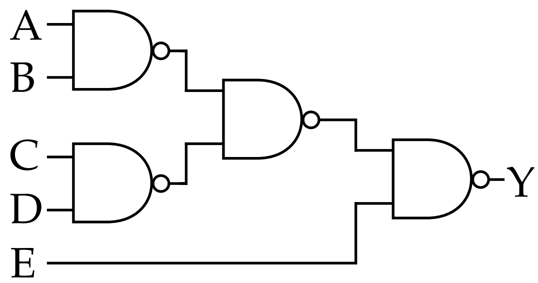
Draw the gate network for the *minimal SOP*. Assume to have access to both normal and inverted signal for each input.

Zephan's Solution

`https://vod.video.cornell.edu/id/1_2em1j8b9`

Problem 4. Simplify Expressions with De Morgan's Theorem

Consider the following gate network.



Write the corresponding boolean expression.

Why could we not just simply minimize this boolean equation with a K-Map?

Simplify the boolean equation using De Morgan's Theorem and bubble pushing methods.

Problem 5. Implementing an Inverse S-Box for Symmetric Nibble Encryption

The Advanced Encryption Standard (AES) is a widely used symmetric-key encryption algorithm (the same key is used for both encryption and decryption). It performs a sequence of word- and byte-operations on the message to be encrypted or decrypted. One critical operation is the Rijndael S-box (`https://en.wikipedia.org/wiki/Rijndael_S-box`), which substitutes one byte for another. For instance, to substitute a byte with decimal value 149 (hexadecimal 0x95) during encryption, you would replace it with the value found at row 9, column 5 of the forward S-box matrix, which contains the hexadecimal value 0x2A (decimal 42).

In this problem, we will work with this toy sbox, which operates on nibbles (4 bits) to keep things simple.

Complete the truth table for the reverse s-box.

Forward Nibble S-Box

Input	Output
0000	1110
0001	0100
0010	1101
0011	0001
0100	0010
0101	1111
0110	1011
0111	1000
1000	0011
1001	1010
1010	0110
1011	1100
1100	0101
1101	1001
1110	0000
1111	0111

Truth table for Reverse Nibble S-Box

I3	I2	I1	I0	O3	O2	O1	O0

Optimize the logic for the four output bits with Karnaugh maps. Write the resulting minimized SOPs for each output.

Output O3

CD \ AB	00	01	11	10
00				
01				
11				
10				

$Y =$ ____________

Output O2

CD \ AB	00	01	11	10
00				
01				
11				
10				

$Y =$ ____________

Output O1

CD \ AB	00	01	11	10
00				
01				
11				
10				

$Y =$ ____________

Output O0

CD \ AB	00	01	11	10
00				
01				
11				
10				

$Y =$ ____________

Problem 6. Proof of De Morgan's Theorem

In lecture we learned about *De Morgan's theorem* (T12′):

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

Proof this theorem by perfect induction.

Next, proof the equation by utilizing the other Boolean theorems and axioms.