ECE 2300 Digital Logic and Computer Organization

Topic 1: Digital Circuits

http://www.csl.cornell.edu/courses/ece2300
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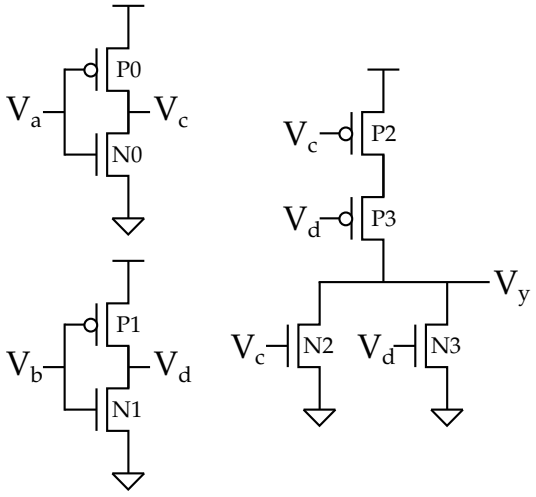
List of Problems

Problem 1. Comparison of Two Circuits

In this problem, we will explore two circuits. First, we will inspect an inverter-first circuit. Afterwards, we will compare it with an inverter-last circuit we already know from lecture.

Part 1.A Circuit Diagram with Voltage Sources of Inverter-First Circuit

Given the transistor-level schematic of this inverter-first circuit, draw the corresponding complete circuit diagram with all voltage sources and an LED connected to the output. Label all transistors and voltage sources. *Hint: The outputs V_c and V_d of the inverters are the inputs of the second stage.*

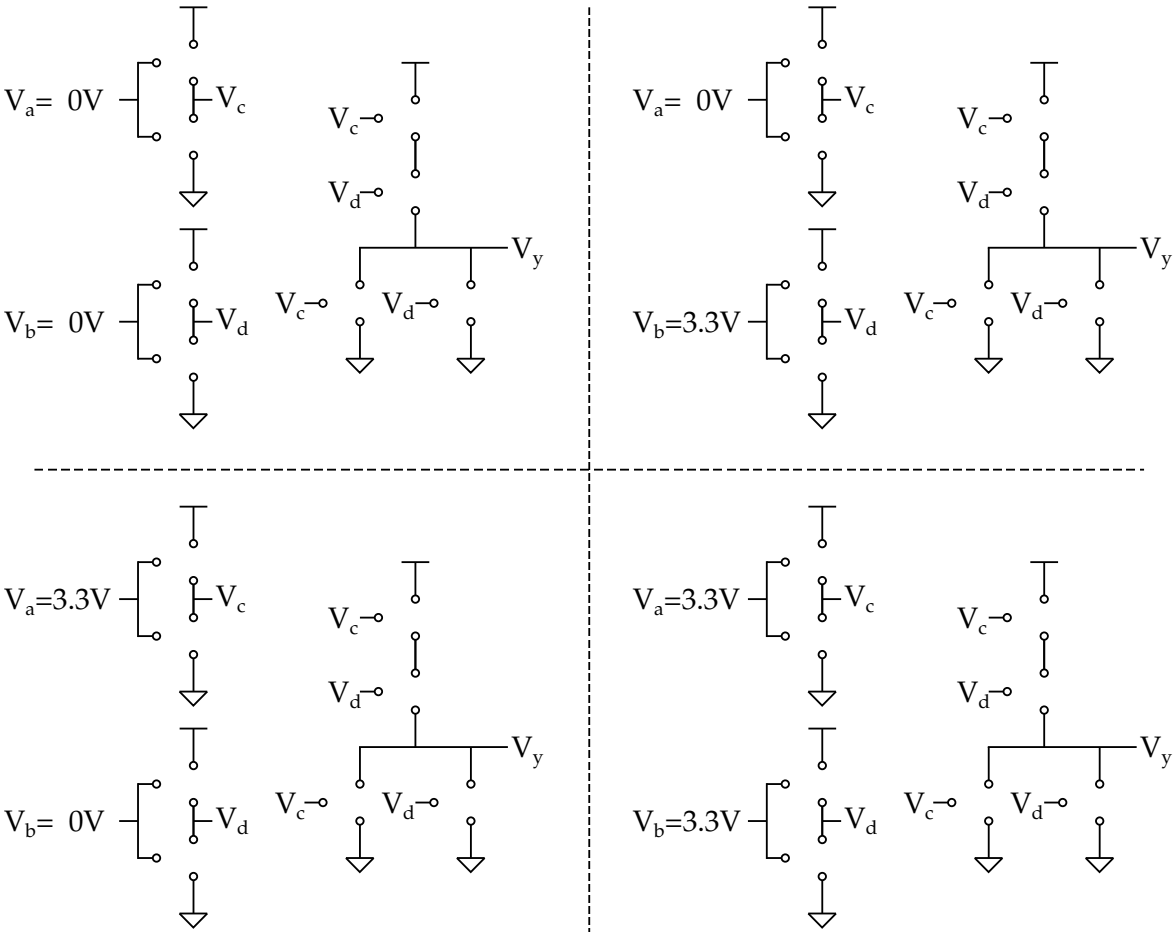


Note

You have hopefully noticed how annoying it is to create these complete circuit diagrams with all connections and voltage sources. Besides, the schematics become confusing. Thus, from now on we will only use transistor circuits.

Part 1.B Switch-Level Model of Inverter-First Circuit

Complete the switch-level models for the inverter-first transistor circuit for the specified input voltages. *Hint: Don't forget to draw the switch contacts of open switches.*

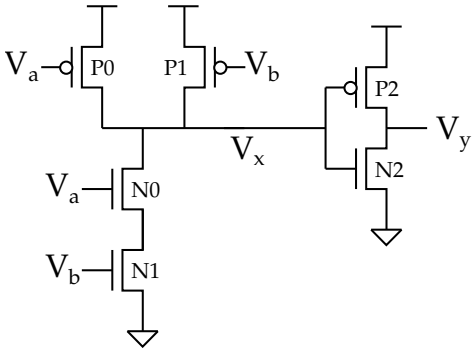


Complete the table. Mark closed transistors with `C` and open with `O`.

V_a	P_0	N_0	V_c	V_b	P_1	N_1	V_d	P_2	P_3	N_2	N_3	V_y
0V				0V								
0V				3.3V								
3.3V				0V								
3.3V				3.3V								

Part 1.C Inverter-Last Circuit

Consider this alternative inverter-last circuit from lecture. **Complete its table.** Only mark closed transistors with `C` and leave cells of open transistors empty.



V_a	V_b	P_0	N_0	P_1	N_1	V_x	P_2	N_2	V_y
0V	0V								
0V	3.3V								
3.3V	0V								
3.3V	3.3V								

Part 1.D Comparative Analysis

Compare the inverter-first and inverter-last circuits by comparing their tables from the previous problems. Address the following questions: (1) How does the output behavior differ between both circuits? (2) How many transistors does each circuit require? (3) Which circuit would you choose for implementation in a real chip, and why?

Note

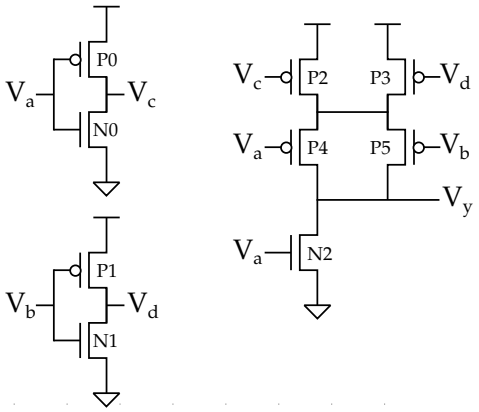
If you want to learn more about the relationship between these two circuits, you should look into "De Morgan's law". We will cover it extensively in topic 3.

Problem 2. Unbalanced CMOS Circuit

In this problem, we will checkout an unbalanced CMOS circuit and fix it afterwards.

Part 2.A Switch-Level Models

Given this transistor schematic, draw the switch-level models for all four input combinations and mark potential issues:
(1) $V_a = 0\,\text{V}$, $V_b = 0\,\text{V}$;
(2) $V_a = 0\,\text{V}$, $V_b = 3.3\,\text{V}$;
(3) $V_a = 3.3\,\text{V}$, $V_b = 0\,\text{V}$;
(4) $V_a = 3.3\,\text{V}$, $V_b = 3.3\,\text{V}$.
Hint: You need to draw all four switch-level model diagrams from scratch.



Complete the table for the switch-level models. Label closed transistors with `C` (and leave cells of open transistors empty). Mark V_y with `Z` when the potential is floating (neither connected to `VDD` or `GND`) and `SC` for short-circuits.

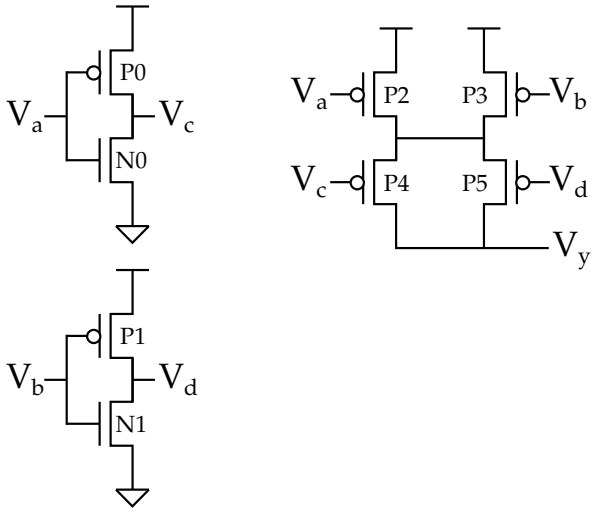
V_a	V_b	P_0	P_1	N_0	N_1	V_c	V_d	P_2	P_3	P_4	P_5	N_2	V_y
0V	0V												
0V	3.3V												
3.3V	0V												
3.3V	3.3V												

Part 2.B Problem Analysis

Explain why some input combinations cause V_y to float and others cause short-circuits. How could these issues be fixed?

Part 2.C Fix Pull-down Network

Assume the pull-up network of the second stage is correct. **Redesign the pull-down network to prevent the output from floating and to eliminate short-circuits.**



Check that all floating outputs and short-circuits were eliminated by filling out the table. Mark closed transistors with `C`.

V_a	V_b	P_0	P_1	N_0	N_1	V_c	V_d	P_2	P_3	P_4	P_5	N_2	N_3	N_4	N_5	V_y
0V	0V															
0V	3.3V															
3.3V	0V															
3.3V	3.3V															

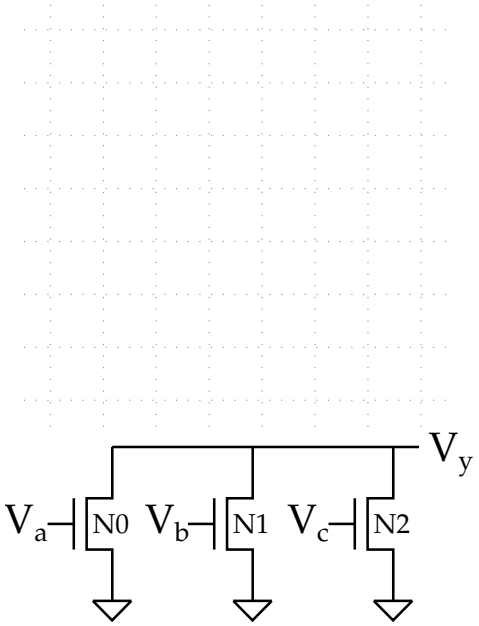
Niklas's Solution

`https://vod.video.cornell.edu/id/1_967s02fy`

Problem 3. Complete the CMOS Circuits

Part 3.A Circuit A

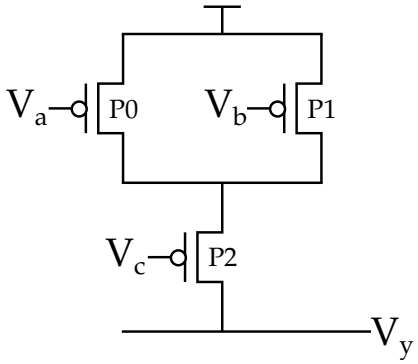
Complete the pull-up network of this CMOS circuit. Label the added transistors and fill out the table. Mark closed transistors with `C` and leave cells of open transistors blank.



V_a	V_b	V_c	P_0	P_1	P_2	N_0	N_1	N_2	V_y
0V	0V	0V							
0V	0V	3.3V							
0V	3.3V	0V							
0V	3.3V	3.3V							
3.3V	0V	0V							
3.3V	0V	3.3V							
3.3V	3.3V	0V							
3.3V	3.3V	3.3V							

Part 3.B Circuit B

Complete the pull-down network of this CMOS circuit. Label the added transistors and fill out the table. Mark closed transistors with `C` and leave cells of open transistors blank.



V_a	V_b	V_c	P_0	P_1	P_2	N_0	N_1	N_2	V_y
0V	0V	0V							
0V	0V	3.3V							
0V	3.3V	0V							
0V	3.3V	3.3V							
3.3V	0V	0V							
3.3V	0V	3.3V							
3.3V	3.3V	0V							
3.3V	3.3V	3.3V							

Paige's Solution

`https://vod.video.cornell.edu/id/1_5cnxx0rp`

Problem 4. Timing Analysis

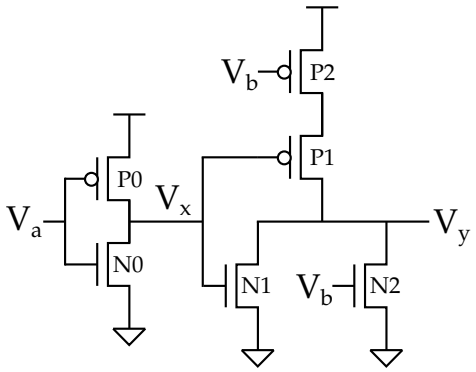
In this problem, we will explore a simple two-input two-stage circuit with different delay models.

Note

When designing digital logic, we work with multiple delay models depending on the situation. For instance, we might use a zero or constant delay model for a quick simulation. However, at later stages of chip design (after the chip's layout is finalized), we might extract its detailed timing behavior and perform much more comprehensive timing simulations. A design might pass all tests in a zero delay model, but fail with actual delays applied. Thus, it is critical to always consider which timing model you are currently using and how this might impact your simulation results.

Part 4.A Logic Behavior

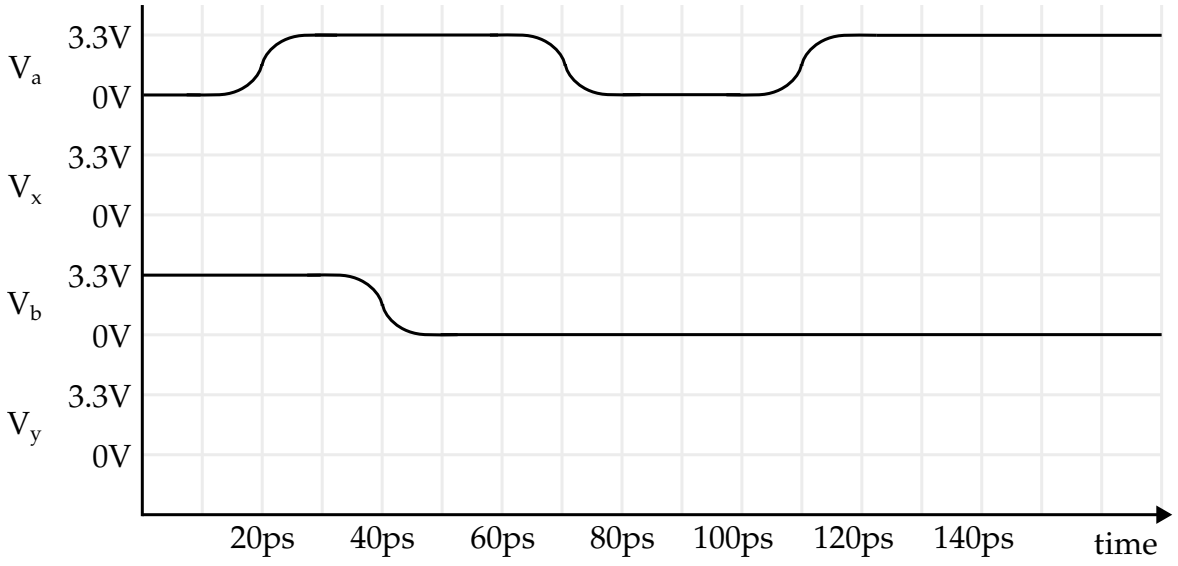
As a first step, complete the following table to get to know the logical behavior of this circuit. Label closed transistors with `C` and leave cells of open transistors empty.



V_a	P_0	N_0	V_x	V_b	P_1	P_2	N_1	N_2	V_y
0V				0V					
0V				3.3V					
3.3V				0V					
3.3V				3.3V					

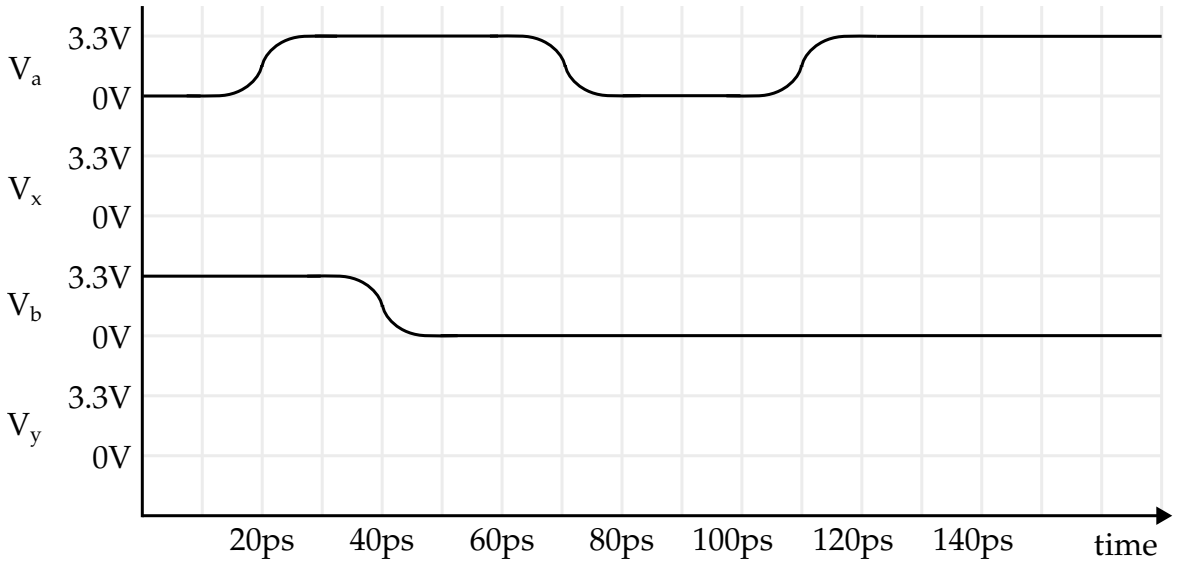
Part 4.B Timing Diagram with Zero Delay Model

Complete the timing diagram for a zero delay model. Mark timing dependencies with arrows (from change in input/intermediate signal to resulting change in output/intermediate signal) in timing diagram. *Hint: Remember that we are drawing voltage levels in topic 1. They cannot jump from one level to another. Instead they change continuously from low to high or vice versa.*



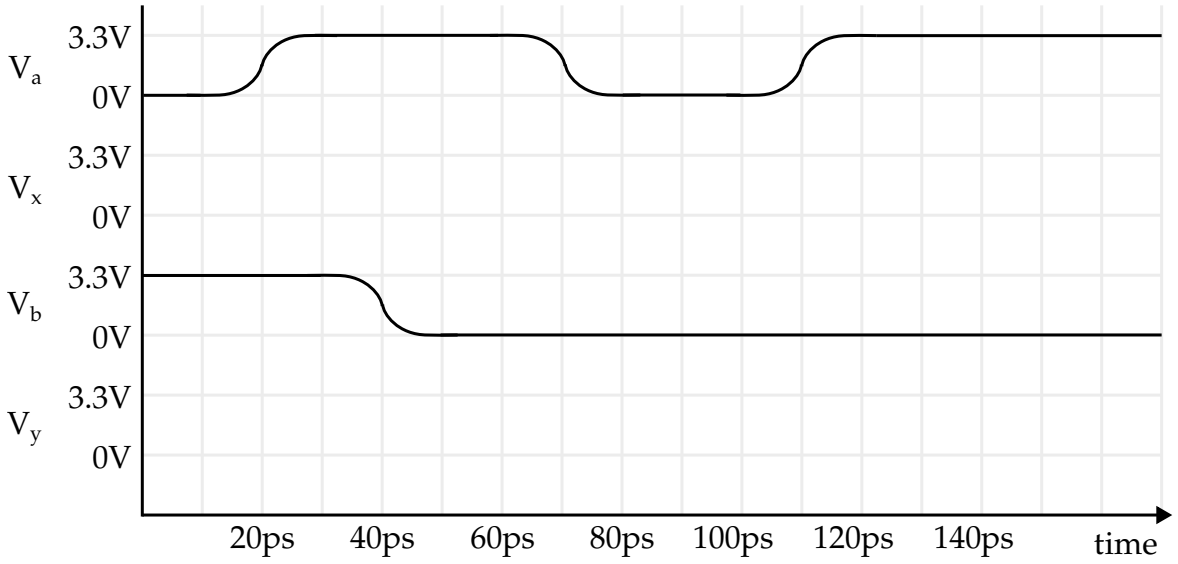
Part 4.C Timing Diagram with Constant Delay Model

Complete the timing diagram for a constant delay model. Mark timing dependencies with arrows in timing diagram.
Use a delay of $t_{inv} = 10\,\text{ps}$ for the inverter and $t_{nor} = 20\,\text{ps}$ for the nor-gate (right module).



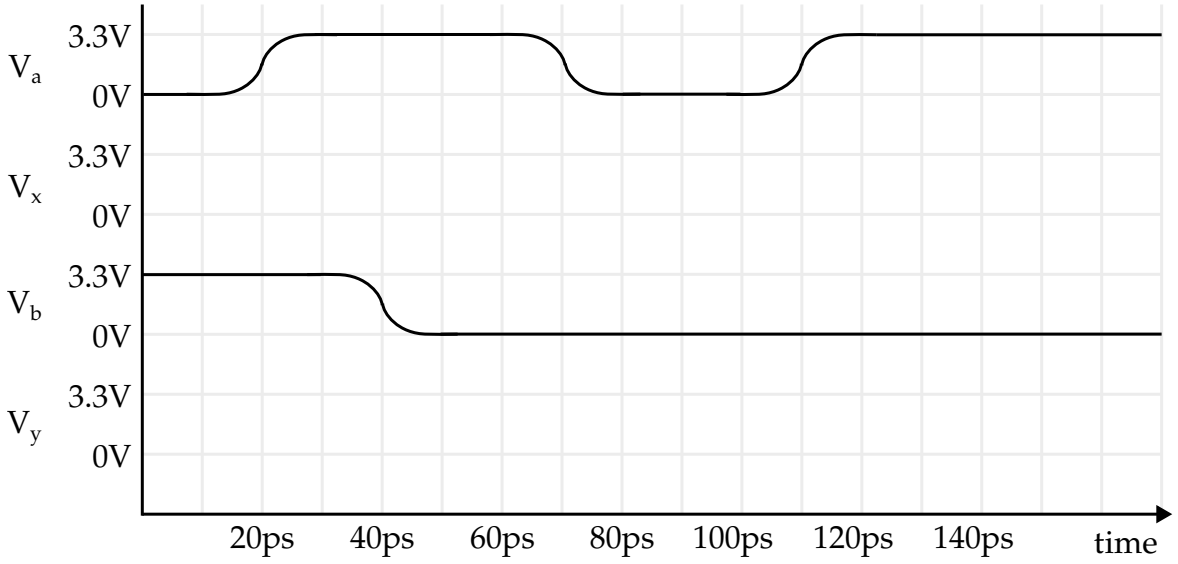
Part 4.D Timing Diagram with Input-Dependent Constant Delay Model

Complete the timing diagram for an input-dependent constant delay model. Mark timing dependencies with arrows in timing diagram.
Use the following input dependent delays: $t_{a\rightarrow x} = 10\,\text{ps}$; $t_{b\rightarrow y} = 20\,\text{ps}$; $t_{x\rightarrow y} = 10\,\text{ps}$.



Part 4.E Timing Diagram with Transition- and Input-Dependent Constant Delay Model

Complete the timing diagram for a transition- and input-dependent delay model. Mark timing dependencies with arrows in timing diagram.
Use the following delays *(Hint: Transition-dependence depends on the change at the output)*:
$t_{a\rightarrow x,hl} = 10\,\text{ps}$; $t_{a\rightarrow x,lh} = 20\,\text{ps}$; $t_{b\rightarrow y,hl} = 20\,\text{ps}$; $t_{b\rightarrow y,lh} = 30\,\text{ps}$; $t_{x\rightarrow y,hl} = 10\,\text{ps}$; $t_{x\rightarrow y,lh} = 30\,\text{ps}$.



Nicholas's Solution

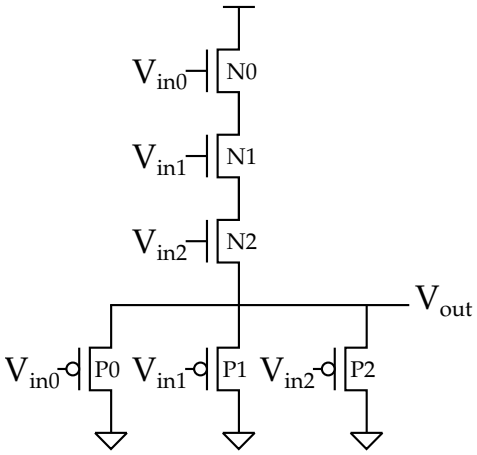
`https://vod.video.cornell.edu/id/1_knal8ljd`

Problem 5. Dead Man's Switch

For your robotics lab, you are tasked with creating the circuit for a special dead man's switch. The robot is allowed to operate only when three buttons are pressed: the operator's left hand button, right hand button, and door switch. The buttons and switches are *active-high*, which means that when pressed they output a high signal (3.3 V). When not pressed they output a low signal (0 V).

Part 5.A Initial Design

You design a circuit that outputs 3.3 V when all three inputs are 3.3 V. **Check for the correct behavior of your circuit with the following table.** Mark closed transistors with `C`.



V_{in0}	V_{in1}	V_{in2}	P_0	P_1	P_2	N_0	N_1	N_2	V_{out}
0V	0V	0V							
0V	0V	3.3V							
0V	3.3V	0V							
0V	3.3V	3.3V							
3.3V	0V	0V							
3.3V	0V	3.3V							
3.3V	3.3V	0V							
3.3V	3.3V	3.3V							

Part 5.B Problem Analysis

Your lab mate John comes by your desk and sees your design. He mentions that he does not think this design will work. Before you can ask him why he thinks so, he leaves for a meeting. You are trying to figure out what is wrong with your circuit.

Explain the issue with your circuit.

Note

For ECE 2300, we only require you to know that pull-up networks consist of PMOS transistors and pull-down networks consist of NMOS transistors.
In ECE 3150, you will learn more about low-level circuit/device issues that prevent NMOS transistors from pulling their output voltage completely up to `VDD` *and PMOS transistors from pulling their output completely down to* `GND`*. You can check out this short video[a] if you don't want to wait and want to get a feel for some analog circuit theory. Furthermore, this video[b] shows the effect in a circuit simulator.*

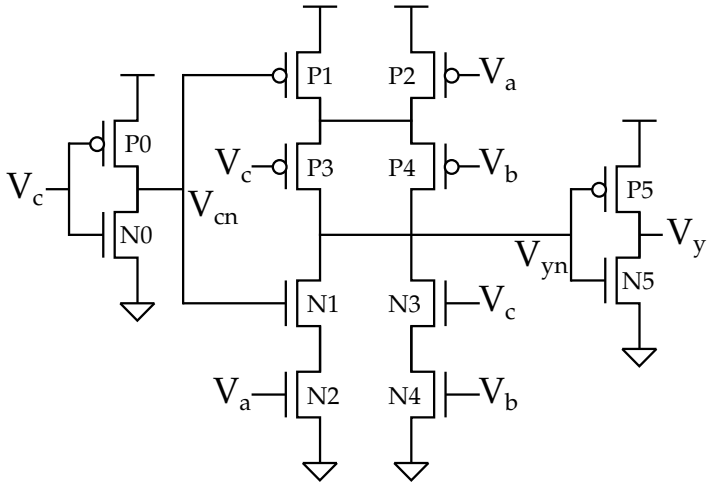
[a] `https://youtu.be/N3r8-58J1X4?si=M2JANOjdhz7WPL5o`
[b] `https://youtu.be/JUhtuQ4Pq3g?si=D60d57nFIvmZ6n9U`

Part 5.C Fix the Circuit

You want to fix the circuit quickly before John comes back. You remember from lecture that you should design a two-stage circuit. The first stage output (V_x) will be 3.3 V as long as any input is not pressed (0 V). The second stage will invert V_x to produce V_{out}.

Draw the transistor schematic of the fixed circuit. Label the transistors and inputs/outputs. **Check that your circuit has the correct behavior.**

Problem 6. Unknown CMOS Circuit



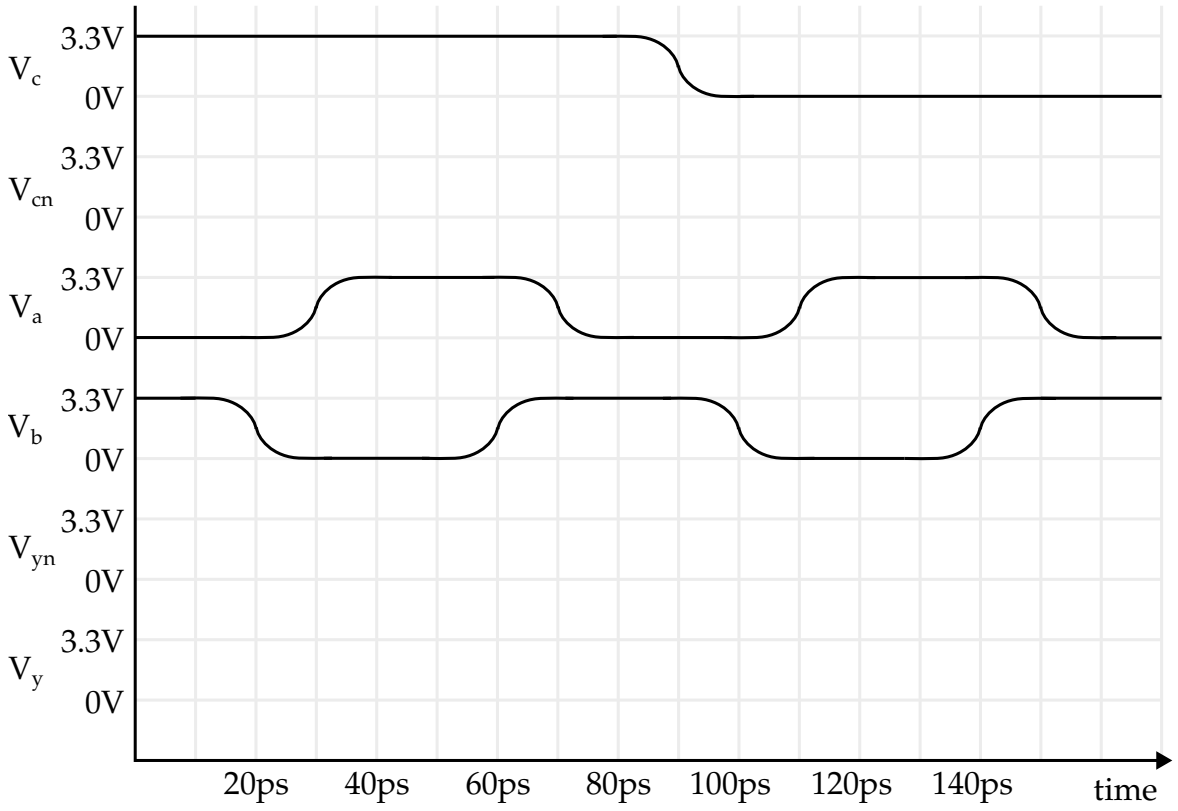
In this problem, we will explore and identify this unknown CMOS circuit.

Part 6.A Timing Diagram

First, complete the table for these potential inputs.

V_c	P_0	N_0	V_{cn}	V_b	V_a	P_1	P_2	P_3	P_4	N_1	N_2	N_3	N_4	V_{yn}	P_5	N_5	V_y
0V				0V	0V												
0V				0V	3.3V												
0V				3.3V	0V												
0V				3.3V	3.3V												
3.3V				0V	0V												
3.3V				0V	3.3V												
3.3V				3.3V	0V												
3.3V				3.3V	3.3V												

Afterwards, complete this timing diagram with a zero delay model. Mark timing dependencies with arrows in timing diagram.



Part 6.B Behavior Analysis

Inspect the output behavior and waveform of the circuit. **Explain what this circuit does.** *Hint: This circuit implements a "multiplexer", and input C is its "select" port.*

Part 6.C 8-Bit Multiplexer

The above circuit implements a 1-bit multiplexer. **How would you implement an 8-bit multiplexer to select between two 8-bit integers?**