



Best Paper, ACM International Conference on Supercomputing, New York, NY, June 2002  
Best Paper, IEEE/ACM International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems, Montreal, QC, July 1998  
Graduate Student Award for Excellence, University of Virginia Department of Computer Science, 1994, 1995  
Samuel N. Alexander Ph.D. Fellowship, Washington, D.C., ACM Chapter, 1994  
Tuition Scholarship for Women, Digital Equipment Corporation, 1990-1992  
Graduate Fellowship, University of Virginia Department of Computer Science, 1990-1991  
AT&T Bell Laboratories Graduate Fellowship, 1988-1990  
John Von Neumann Prize in Supercomputing, Princeton University Department of Computer Science, September 1987

## Publications and Patents

### Refereed Journals

1. K. Singh, E. Ipek, S.A. McKee, B.R. de Supinski, M. Schulz, R. Caruana, "Predicting Parallel Application Performance via Machine Learning Approaches", *Wiley Concurrency and Computation: Practice and Experience*, 19(17):2219-2235, May 2008.
2. N. Xu, S.A. McKee, L. Nozick, R. Ufomata, "Augmenting Priority Rule Heuristics with Justification and Rollout to Solve the Resource-Constrained Project Scheduling Problem", *Elsevier Computers and Operations Research*, 35(10):3284-3297, October 2008.
3. E. Ipek, S.A. McKee, K. Singh, R. Caruana, B.R. de Supinski, M. Schulz, "Efficient Architectural Design Space Exploration via Predictive Modeling", *ACM Transactions on Architecture and Code Optimization*, 4(4), Article 1, January 2008.
4. M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, "Data Cache Techniques to Save Power and Deliver High Performance in Embedded Systems", *Transactions on High Performance Embedded Architectures and Compilers*, 2(1):62-81, 2007. Springer Lecture Notes in Computer Science 4367.
5. J. Marathe, F. Mueller, T. Mohan, S.A. McKee, B.R. de Supinski, A. Yoo, "METRIC: Memory Tracing via Dynamic Binary Rewriting to Identify Cache Inefficiencies", *ACM Transactions on Programming Languages and Systems*, 29(2), Article 12, April 2007.
6. M.J. Geiger, S.A. McKee, G.S. Tyson, "Specializing Cache Structures for High Performance and Energy Conservation in Embedded Systems", *Transactions on High Performance Embedded Architectures and Compilers*, 1(1):50-90, 2007.
7. A. Bunker, G. Gopalakrishnan, S.A. McKee, "Formal Hardware Specification Languages for Protocol Compliance Verification", *ACM Transactions on Design Automation of Electronic Systems*, 9(1):1-32, January 2004.
8. B. Chandramouli, W.C. Hsieh, J.B. Carter, S.A. McKee, "A Cost Model for Integrated Restructuring Optimizations", *Journal of Instruction Level Parallelism*, August 2003.
9. V.S. Pingali, S.A. McKee, W.C. Hsieh, J.B. Carter, "Restructuring Computations for Temporal Data Cache Locality", Springer *International Journal of Parallel Programming*, 31(4):305-338, August 2003.
10. L. Zhang, Z. Fang, M. Parker, B.K. Mathew, L. Schaelicke, J.B. Carter, W.C. Hsieh, S.A. McKee, "The Impulse Memory Controller", *IEEE Transactions on Computers*, 50(11):1117-1132, November 2001.
11. S.A. McKee, Wm.A. Wulf, J.H. Aylor, R.H. Klenke, M.H. Salinas, S.I. Hong, D.A.B. Weikle, "Dynamic Access Ordering for Streamed Computations", *IEEE Transactions on Computers*, 49(11):1255-1271, November 2000.

12. J.B. Carter, W.C. Hsieh, L.B. Stoller, M.R. Swanson, L. Zhang, S.A. McKee, "Impulse: Memory System Support for Scientific Applications", *Scientific Programming*, 7(3-4):195-209, IOS Press, fall 1999.
13. S.A. McKee, R.H. Klenke, M.H. Salinas, K.L. Wright, Wm.A. Wulf, J.H. Aylor, A.P. Batson, "Improving Memory Bandwidth for Streamed References", *IEEE Computer*, 31(7):54-63, July 1998.

#### Refereed Conferences

14. K. Singh, M. Bhadauria, S.A. McKee, "Prediction-based Power Estimation and Scheduling for CMPs", Proc. ACM International Conference on Supercomputing (ICS'09), Manhattan, NY, June 2009 (extended abstract and poster presentation). to appear.
15. M. Bhadauria, V. Weaver, S.A. McKee, "PARSEC: Hardware Profiling for CMP Design of Emerging Workloads", Proc. ACM International Conference on Supercomputing (ICS'09), Manhattan, NY, June 2009 (extended abstract and poster presentation). to appear.
16. Md. Mafijul Islam, P. Stenström, S.A. McKee, "Cancellation of Loads that Return Zero Using Zero Valued Caches", Proc. ACM International Conference on Supercomputing (ICS'09), Manhattan, NY, June 2009 (extended abstract and poster presentation). to appear.
17. P.E. West, Y. Peress, G.S. Tyson, S.A. McKee, "Core Monitors: Monitoring Performance in Multicore Processors", Proc. ACM Computing Frontiers Conference (CF'09), Ischia, IT, May 2009. to appear.
18. G. Bronevetsky, K. Pingali, D. Marques, R. Rugina, S.A. McKee, "Compiler-Enhanced Incremental Checkpointing for OpenMP Applications", Proc. International Parallel and Distributed Processing Symposium (IPPDS'09), Rome, IT, May 2009. to appear.
19. J. Li, X. Ma, K. Singh, M. Schulz, B.R. de Supinski, S.A. McKee, "Machine Learning Based Online Performance Prediction for Runtime Parallelization and Task Scheduling", Proc. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS'09), Boston, MA, April 2009. to appear.
20. V.M. Weaver, S.A. McKee. "Optimizing for Size: Exploring the Limits of Code Density", Proc. Architectural Support for Programming Languages and Operating Systems (ASPLOS '09), Washington DC, March 2009 (poster presentation).
21. G. Venkatasubramanian, D. Wolinsky, R. Figueiredo, P.O. Boykin, J.A.B. Fortes, T. Li, J.-K. Peir, L.K. John, D. Kaeli, D. Lilja, S.A. McKee, G. Memik, A. Roy, B. Burnett, G.S. Tyson, "A Community Distributed Infrastructure for Computer Architecture Research and Education", Proc. Architectural Support for Programming Languages and Operating Systems (ASPLOS '09), Washington DC, March 2009 (poster presentation).
22. M. Bhadauria, V.M. Weaver, S.A. McKee, "Accommodating Diversity in CMPs with Heterogeneous Frequencies", Proc. EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC'09), Paphos, CY, January 2009, pp. 248-262 (28% acceptance). Springer *Lecture Notes in Computer Science 5409*.
23. M.A. Watkins, S. McKee, L. Schaelicke, "Revisiting Cache Block Superloading: A Phase-Adaptive Approach to Increasing Cache Performance", Proc. EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC '09), Paphos, CY, January 2009, pp. 339-354 (28% acceptance). Springer *Lecture Notes in Computer Science 5409*.
24. V.M. Weaver, S.A. McKee, "Can Hardware Performance Counters be Trusted?", Proc. IEEE International Symposium on Workload Characterization (IISWC'08), Seattle, WA, September 2008, pp. 141-150 (35% acceptance).

25. P.A. Castillo Valdivieso, J.J. Merelo Guervós, M. Moretó, F.J. Cazorla, M. Valero, A.M. Mora, J.L. Jiménez Laredo, S.A. McKee, “Evolutionary System for Prediction and Optimization of Hardware Architecture Performance”, Proc. IEEE Congress on Evolutionary Computation (CEC), Hong Kong, CN, May 2008, pp. 1941-1948.
26. G. Bronevetsky, D. Marques, K. Pingali, S.A. McKee, R. Rugina, “Compiler-Enhanced Incremental Checkpointing for OpenMP Applications”, Proc. ACM Symposium on Principles and Practices of Parallel Programming (PPoPP’08), Salt Lake City, UT, February 2008 (extended abstract and poster presentation).
27. V.M. Weaver, S.A. McKee, “Using Dynamic Binary Instrumentation to Generate Multi-Platform SimPoints: Methodology and Accuracy”, Proc. EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC’08), Göteborg, SE, January 2008, pp. 305-319 (34% acceptance). Springer *Lecture Notes in Computer Science* 4917.
28. M. Watkins, S.A. McKee, L. Schaelicke, “A Phase Adaptive Approach to Increasing Cache Performance”, Proc. IEEE/ACM International Conference on Parallel Architectures and Compilation Techniques (PACT’07), Brasov, RO, September 2007 (extended abstract and poster presentation).
29. C. Dolen, C. Haymes, K. Inoue, D. Kuchta, S. Lekuch, J.E. Moreira, E. Shenfield, X. Shen, C. Trammell, M. Tsao, S.A. McKee, “Chameleon Shared Memory Project”, Proc. Linux Cluster Institute International Conference on High-Performance Clustered Computing (LCI’07), Lake Tahoe, CA, May 2007 (best poster award).
30. B.C. Lee, D.M. Brooks, B.R. de Supinski, M. Schulz, K. Singh, S.A. McKee, “Methods of Inference and Learning for Performance Modeling of Parallel Applications”, Proc. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP’07), San Jose, CA, March 2007, pp. 240-258 (33% acceptance).
31. M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, “Leveraging High Performance Data Cache Techniques to Save Power in Embedded Systems”, Proc. EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC’07), Ghent, BE, February 2007, pp. 23-37 (29% acceptance). Springer *Lecture Notes in Computer Science* 4367.
32. N.B. Sam, S.A. McKee, P. Kudva, “Rethinking Processor Design: Parameter Correlations”, Proc. IEEE International Conference on Electronics, Circuits and Systems (ICECS’06), Nice, FR, December 2006, pp. 156-159.
33. E. Ipek, S.A. McKee, B.R. de Supinski, M. Schulz, R. Caruana, “Efficiently Exploring Architectural Design Spaces via Predictive Modeling”, Proc. ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XII), San Jose, CA, October 2006, pp. 195-206 (24% acceptance).
34. M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, “A Precisely Tunable Drowsy Cache Management Mechanism”, Proc. IBM P=ac<sup>2</sup> (P = Power/Performance, a = architecture, and c<sup>2</sup> = circuits × compilers) Conference, Yorktown Heights, NY, October, 2006 (33% acceptance).
35. M.J. Geiger, S.A. McKee, G.S. Tyson, “Beyond Region Caching: Specializing Cache Structures for High Performance and Energy Conservation”, Proc. EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC’05), Barcelona, ES, November 2005, pp. 102-115 (20% acceptance). Springer *Lecture Notes in Computer Science* 3793.
36. E. Ipek, B.R. de Supinski, M. Schulz, S.A. McKee, “An Approach to Performance Prediction for Parallel Applications”, Proc. European Conference Series on Parallel Processing (EuroPar’05), Lisbon, PT, August 2005, pp. 196-205 (30% acceptance). Springer *Lecture Notes in Computer Science* 3648.

37. B.S. White, S.A. McKee, B.R. de Supinski, B.J. Miller, D. Quinlan, M. Schulz, "Improving the Computational Intensity of Unstructured Grid Applications", Proc. ACM International Conference on Supercomputing (ICS'05), Boston, MA, June 2005, pp. 341-350 (28% acceptance).
38. M.J. Geiger, S.A. McKee, G.S. Tyson, "Drowsy Region-Based Caches: Minimizing Both Dynamic and Static Power Dissipation", Proc. ACM Computing Frontiers Conference (CF'05), Ischia, IT, May 2005, pages 378-384.
39. M. Schulz, B.S. White, S.A. McKee, H.S. Lee, J. Jeitner, "Owl: Next-Generation System Monitoring", Proc. ACM Computing Frontiers Conference (CF'05), Ischia, IT, May 2005, pp. 116-124.
40. S.A. McKee, "Reflections on the Memory Wall", Proc. ACM Computing Frontiers Conference (CF'04), Ischia, IT, April 2004, pp. 162-167 (invited paper).
41. T. Mohan, B.R. de Supinski, S.A. McKee, F. Mueller, A. Yoo, M. Schulz, "Identifying and Exploiting Spatial Regularity in Data Memory References", Proc. ACM/IEEE Conference on Supercomputing (SC'03), Phoenix, AZ, November 2003, p. 49 (one of six candidates for best paper, 29% acceptance).
42. S.A. McKee, D.M. Kubarek, "Real World Engineering: a Course for Masters Students Headed for Industry", Proc. ASEE/IEEE Frontiers in Education Conference (FIE'03), Boulder, CO, November 2003, Session F1E, pp. 16-21.
43. T. Mu, J. Tao, M. Schulz, S.A. McKee, "Interactive Locality Optimization on NUMA Architectures", Proc. ACM Symposium on Software Visualization (SoftVis'03), San Diego, CA, June 2003, pp. 133-142 (31% acceptance).
44. M. Schulz, S.A. McKee, "A Framework for Portable Shared-Memory Programming", Proc. IEEE/ACM International Parallel and Distributed Processing Symposium (IPDPS'03), Nice, France, April 2003, pp. 54-62 (29% acceptance).
45. J. Marathe, F. Mueller, T. Mohan, B.R. de Supinski, S.A. McKee, A. Yoo, "METRIC: Tracking Down Inefficiencies in the Memory Hierarchy via Binary Rewriting", Proc. International Symposium on Code Generation and Optimization (CGO'03), San Francisco, CA, March 2003, pp. 289-300 (35% acceptance).
46. Z. Fang, S.A. McKee, M. Valero, "An MPEG-4 Performance Study", Proc. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS'03), Austin, TX, March 2003, pp. 49-57 (33% acceptance).
47. M. Tao, J. Tao, M. Schulz, S.A. McKee, "Visualizing Data Distribution on NUMA Architectures to Guide Incremental Optimizations", Proc. Supercomputing (SC'02), Baltimore, MD, November 2002 (poster).
48. A. Bunker, S.A. McKee, G. Gopalakrishnan, "An Overview of Formal Hardware Specification Languages", Proc. ACM/CRA Grace Hopper Celebration of Women in Computing (GHC'02), Vancouver, BC, October 2002.
49. V.K. Pingali, S.A. McKee, W.C. Hsieh, J.B. Carter, "Computation Regrouping: Restructuring Programs for Temporal Data Cache Locality", Proc. Annual ACM International Conference on Supercomputing (ICS'02), New York, June 2002, pp. 252-261 (best PC-voted paper, 20% acceptance).
50. B. Chandramouli, J.B. Carter, W.C. Hsieh, S.A. McKee, "A Cost Framework for Evaluating Integrated Restructuring Optimizations", Proc. IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'01), Barcelona, ES, September 2001, pp. 131-140 (21% acceptance).

51. Z. Fang, L. Zhang, J.B. Carter, S.A. McKee, W.C. Hsieh, "Reevaluating Online Superpage Promotion with Hardware Support", Proc. International IEEE Symposium on High Performance Computer Architecture (HPCA-7), Monterrey, MX, January 2001, pp. 63-72 (24% acceptance).
52. D.A.B. Weikle, S.A. McKee, K. Skadron, Wm.A. Wulf, "Caches as Filters: a Framework for the Analysis of Caching Systems", Proc. CRA Grace Hopper Celebration of Women in Computing, Cape Cod, MA, September 2000.
53. L. Schaelicke, A. Davis, S.A. McKee, "Profiling Interrupts in Modern Architectures", Proc. IEEE International Symposium on Modeling, Analysis and Simulation of Computers and Telecommunication Systems (MASCOTS'00), San Francisco, CA, August 2000, pp. 115-123.
54. B.K. Mathew, S.A. McKee, J.B. Carter, A. Davis, "Algorithmic Foundations for a Parallel Vector Access Memory System", Proc. ACM Symposium on Parallel Algorithms and Architectures (SPAA'00), Bar Harbor, ME, July 2000, pp. 156-165 (29% acceptance).
55. Z. Fang, L. Zhang, S.A. McKee, J.B. Carter, W.C. Hsieh, "Online Superpage Promotion Revisited", Proc. ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS'00), Santa Clara, CA, June 2000, pp. 114-115 (extended abstract).
56. C. Zhang, S.A. McKee, "Hardware-Only Stream Prefetching and Dynamic Access Ordering", Proc. ACM International Conference on Supercomputing (ICS'00), Santa Fe, NM, May 2000, pp. 167-175 (27% acceptance).
57. B.K. Mathew, S.A. McKee, J.B. Carter, A. Davis, "Design of a Parallel Vector Access Unit", Proc. IEEE International Symposium on High Performance Computer Architecture (HPCA-6), Toulouse, France, January 2000, pp. 39-48 (21% acceptance).
58. L. Zhang, J.B. Carter, W.C. Hsieh, S.A. McKee, "Memory System Support for Image Processing", Proc. IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'99), Newport Beach, CA, October 1999, pp. 98-107 (21% acceptance).
59. S.I. Hong, S.A. McKee, M.H. Salinas, R.H. Klenke, J.H. Aylor, Wm.A. Wulf, "Access Order and Effective Bandwidth for Streams on a Direct Rambus Memory", Proc. IEEE International Symposium on High Performance Computer Architecture (HPCA-5), Orlando, FL, January 1999, pp. 80-89 (21% acceptance).
60. D.A.B. Weikle, S.A. McKee, Wm.A. Wulf, "Caches as Filters: A New Approach to Memory Hierarchy Analysis", Proc. IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS-98), Montreal, QC, July 1998, pp. 1-11 (best paper award).
61. S.A. McKee, C.W. Oliver, Wm.A. Wulf, K.L. Wright, J.H. Aylor, "Design and Evaluation of Dynamic Access Ordering Hardware", Proc. ACM International Conference on Supercomputing (ICS'96), Philadelphia, PA, May 1996, pp. 125-132 (43% acceptance).
62. S.A. McKee, Wm. A. Wulf, "A Memory Controller for Improved Performance of Streamed Computations on Symmetric Multiprocessors", Proc. IEEE/ACM International Parallel Processing Symposium (IPPS'96), Honolulu, HI, April 1996, pp. 159-165 (36% acceptance).
63. S.A. McKee, S.A. Moyer, Wm.A. Wulf, C.Y. Hitchcock, "Bounds on Memory Bandwidth in Streamed Computations", Proc. European Conference Series on Parallel Processing (EuroPar'95), Stockholm, SE, September 1995, pp. 83-99. Springer *Lecture Notes in Computer Science* 966.
64. T.C. Landon, R.H. Klenke, J.H. Aylor, M.H. Salinas, S.A. McKee, "An Approach for Optimizing Synthesized High-Speed ASICs", Proc. IEEE International Conference on Application Specific Integrated Circuit Design (ASIC'95), Austin, TX, September 1995, pp. 245-248 (31% acceptance).

65. S.A. McKee, Wm. A. Wulf, "Access Ordering and Memory-Conscious Cache Utilization", Proc. IEEE International Symposium on High Performance Computer Architecture (HPCA'95), Raleigh, NC, January 1995, pp. 253-262 (19% acceptance).
66. S.A. McKee, S.A. Moyer, Wm.A. Wulf, C. Hitchcock, "Increasing Memory Bandwidth for Vector Computations", Proc. International Conference on Programming Languages and System Architectures, Zurich, CH, March 1994, pp. 87-104. Springer *Lecture Notes in Computer Science* 782.
67. S.A. McKee, R.H. Klenke, A.J. Schwab, Wm.A. Wulf, S.A. Moyer, C. Hitchcock, J.H. Aylor, "Experimental Implementation of Dynamic Access Ordering", Proc. Hawaii International Conference on Systems Sciences (HICSS-27), Maui, HI, January 1994, pp. 431-440.
68. T. Barrera, J. Griffith, S.A. McKee, G. Robins, T. Zhang, "Toward a Steiner Engine: Enhanced Serial and Parallel Implementations of the Iterated 1-Steiner MRST Algorithm", Proc. Great Lakes Symposium on VLSI (GLS-VLSI'93), Kalamazoo, MI, March 1993, pp. 90-94.

#### Refereed Workshops

69. M. Zahran, S.A. McKee, "Adaptive Block Placement Policy for Cache Hierarchies", (at HiPEAC'09) Proc. Workshop on Statistical and Machine Learning Approaches to Architecture and Compilation (SMART), Paphos, CY, January 2009.
70. K. Singh, M. Bhaduria, S.A. McKee, "Real Time Power Estimation and Thread Scheduling via Performance Counters", (at MICRO'41) Proc. Workshop on Design, Architecture, and Simulation of Chip-Multiprocessors (DASmp), Como, IT, November 2008.
71. V.M. Weaver, S.A. McKee, "Are Cycle Accurate Simulations a Waste of Time?" (at ISCA-35) Proc. Workshop on Duplicating, Deconstructing, and Debunking, Beijing, CN, June 2008.
72. M. Curtis-Maury, K. Singh, S.A. McKee, F. Blagojevic, D.S. Nikolopoulos, B.R. de Supinski, M. Schulz, "Identifying Energy-Efficient Concurrency Levels Using Machine Learning", (at IEEE Cluster) Proc. International Workshop on Green Computing (GreenCom'07), Austin, TX, September 2007.
73. E. Ipek, J.F. Martínez, B.R. de Supinski, S.A. McKee, M. Schulz, "Dynamic Program Phase Detection in Distributed Shared-Memory Multiprocessors", (at IPDPS'06) Proc. Workshop on the National Science Foundation Next Generation Software Program (NSF/NGS), Rhodes, GR, April 2006, p. 280.
74. M. Schulz, B.S. White, S.A. McKee, H.S. Lee, "A Vision for Next-Generation System Monitoring", (at HPCA-11) Proc. Workshop on Hardware Performance Monitor Design and Functionality, San Francisco, CA, February 2005.
75. T. Suh, H.S. Lee, S.A. McKee, M. Schulz, "Evaluating System-Wide Monitoring Capsule Design Using Xilinx Virtex-II Pro FPGA", (at HPCA-11) Proc. Workshop on Architecture Research using FPGA Platforms (WARFP'05), San Francisco, CA, February 2005 (abstract and presentation).
76. P.K. Szwed, D. Marques, R.M. Buels, S.A. McKee, M. Schulz, "SimSnap: Fast-Forwarding via Native Execution and Application-Level Checkpointing", (at HPCA-10) Proc. Workshop on the Interaction between Compilers and Computer Architectures (Interact-8), Madrid, ES, February 2004.
77. Z. Fang, S.A. McKee, "MPEG4: Fallacies and Paradoxes", Proc. IEEE Annual Workshop on Workload Characterization (WWC-5), Austin, TX, November 2002.

78. T. Mohan, B.R. de Supinski, S.A. McKee, F. Mueller, A. Yoo, "Dynamic Detection of Streams in Memory References", Second Annual Symposium of the Los Alamos Computer Science Institute (LACSI), Santa Fe, NM, October 2001 (abstract and poster).
79. B.R. de Supinski, A. Yoo, F. Mueller, S.A. McKee, "Benchmarking SMP Memory Systems Performance", SCICOMP 4 (IBM SP Scientific Computing User Group), Knoxville, TN, October 2001 (abstract and presentation).
80. F. Mueller, T. Mohan, B.R. de Supinski, S.A. McKee, A. Yoo, "Partial Data Traces: Efficient Generation and Representation", (at PACT'01), Proc. Workshop on Binary Translation (WBT'01), Barcelona, ES, September 2001.
81. L. Zhang, S.A. McKee, J.B. Carter, W.C. Hsieh, "Prefetching within the Impulse Adaptable Memory Controller: Initial Results", (at ISCA), Proc. Workshop on Solving the Memory Wall Problem, Vancouver, BC, June 2000.
82. S.A. McKee, "Compiling for Efficient Memory Utilization", (at HPCA-2), Proc. Workshop on the Interaction of Compilers and Computer Architecture (INTERACT-1), San Jose, CA, February 1996 (abstract and presentation).

#### Refereed Tutorials

83. R. Figueiredo, co-PIs J.-K. Peir, J.A.B. Fortes, T. Li, P.O. Boykin, G.S. Tyson, L.K. John, D. Kaeli, D. Lilja, G. Memik, S.A. McKee, "Archer: Zero-Configuration Virtual Appliances for Architecture Simulation", in conjunction with IEEE International Symposium on Workload Characterization (ISSWC'09), Austin, TX, October 2009.
84. D. Brooks, B.R. de Supinski, B.C. Lee, S.A. McKee, M. Schulz, K. Singh, "Methods of Learning and Inference for Large Design and Parameter Spaces" in conjunction with 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XIII), Seattle, WA, March 2008.
85. S.A. McKee, K. Singh, D. Brooks, B.C. Lee, B.R. de Supinski, M. Schulz, "Inference and Learning for Large Scale Micro-Architectural Analysis", in conjunction with the ACM/IEEE International Symposium on Computer Architecture (ISCA), Federated Computer Research Conferences, San Diego, CA, June 2007.

#### Other

86. Wm.A. Wulf, S.A. McKee, "Hitting the Memory Wall: Implications of the Obvious", *Computer Architecture News*, 23(1):20-24, March 1995. (152 citations on citeseer.ist.psu.edu, and over 25,500 results from a Google Scholar search for "Hitting the Memory Wall")

#### Patents

- Method and Device for Maximizing Memory System Bandwidth by Accessing Data in a Dynamically Determined Order; U.S. Patent number 6,154,826. Inventors: Wm.A. Wulf, S.A. McKee, R.H. Klenke, A.J. Schwab. S.A. Moyer, J.H. Aylor, C.Y. Hitchcock, III. November 28, 2000.

#### Software Tools

1. K. Singh, S.A. McKee, B.R. de Supinski, M. Schulz, "Using Machine Learning to Explore Huge Parameter Spaces for High End Computing Applications: Tools and Examples", (used for journal articles #1 and #3; for conference articles #19, #30, #33, and #36; and for workshop article #72) Cornell Computer Systems Lab Technical Report CSL-TR-2007-1049, July 2007. "Fusion Prediction Modeling Tools"  
URL: <http://fusion.csl.cornell.edu/tools/fpmt.html>.
2. V.M. Weaver, S.A. McKee, "Basic Block Vector Tools" (used for conference article #12)  
URL: [http://www.csl.cornell.edu/~vince/projects/bbv\\_research](http://www.csl.cornell.edu/~vince/projects/bbv_research).

**Grants, Gifts, and Awards**

1. EC HiPEAC Adaptive Compilation Cluster, €10,000 for collaborative travel to University of Siena, sole PI S.A. McKee, 2008.
2. NSF 0750851 “CRI: CRD Collaborative Research: Archer — Seeding a Community-based Computing Infrastructure for Computer Architecture Research and Education”, main PI Renato Figueiredo, co-PIs J.-K. Peir, J.A.B. Fortes, T. Li, P.O. Boykin (Univ. of Florida), G.S. Tyson (Florida State Univ.), L.K. John (Univ. of Texas at Austin), D. Kaeli (Northeastern Univ.), D. Lilja (Univ. of Minnesota), G. Memik (Northwestern Univ.), S.A. McKee (Chalmers Univ. of Technology), 2007.
3. DOE Lawrence Livermore National Laboratory Center for Applied Scientific Computing sub-contract B571234, PI D. Quinlan; “Leveraging OpenAnalysis for Alias Analysis within ROSE”, sole PI S.A. McKee, \$40,000, 2007.
4. NSF CNS Award 0708788, “CRI: IAD Keeping Pace with Growing Computing Needs: A Strategy for Enhancing Multi-Core Microprocessor Research and Education at Cornell University”, co-PIs D. Albonesi, J.F. Martínez, S.A. McKee, \$93,865, 2007.
5. NSF CCF Award 0702616, “Towards Designing Complex Systems: Exponential Design/Configuration/Parameter Space Exploration Tools That Are Efficient, Accurate, and Easily Usable”, sole PI S.A. McKee, \$300,000, 2007-2010.
6. Intel Academic Equipment Donations (for partially building a 64-bit Xeon based cluster), \$26,030, 2007.
7. Cornell Faculty Grant for Undergraduate Research, \$3,000, with Richard X. Yu, summer 2007.
8. Cornell University Undergraduate Research Award (sponsored by Intel), \$3,000, with D. Elias Bermudez, summer 2007.
9. Cornell University Undergraduate Research Award (sponsored by Intel), \$3,000, with Cathy Chen, summer 2007.
10. Cornell University Undergraduate Research Award (sponsored by Intel), \$3,000, with Alexis Collins, summer 2007.
11. Cornell University Undergraduate Research Award (sponsored by Intel), \$3,000, with David Drew, academic year 2006-2007.
12. Cornell University Undergraduate Research Award (sponsored by Intel), \$3,000, with James Lee, academic year 2006-2007.
13. Cornell University Undergraduate Research Award (sponsored by Motorola), \$800, with Siu Yu Cherie Kwan, fall 2006.
14. Cornell University Undergraduate Research Award (sponsored by Intel), \$3,000, with Ruke Ufomata, summer 2006; \$2,000 academic year 2006-2007 (student is now a Cornell Presidential Research Scholar).
15. Intel Academic Equipment Donations (six Dell laptops for undergraduate research “mobile lab”), Sole PI S.A. McKee, 2006.
16. Intel Research Foundation Equipment Donation (120 dual-processor 64-bit x86 chips), Sole PI S.A. McKee, 2006.
17. Cornell University Undergraduate Research Award (sponsored by Intel), \$2,000, with Daniel Lee, summer 2005.
18. Cornell University Undergraduate Research Award (sponsored by Intel), \$2,000, with Pamela Chuang, spring 2005.
19. NSF CNS Award 0509406, “Collaborative SMA: Dynamic Program Phase Adaptation and

- Hardware Reconfiguration in Multiprocessor Systems”, PI J.F. Martínez, Co-PI S.A. McKee, \$350,000 total, \$150,000 to PI McKee, 2005-2007.
20. Intel Research Foundation Equipment Donation, Sole PI S.A. McKee, \$74,374, 2004-2005.
  21. DOE Lawrence Livermore National Laboratory Center for Applied Scientific Computing award, ASC, PI D. Dossa; “BlueGene/L: Studies in Scalability and Reconfigurability: Memory Performance”, Subcontract PI S.A. McKee, \$65,000, 2004-2005.
  22. Intel Academic Equipment Donation, Sole PI S.A. McKee, \$67,413, 2004.
  23. NSF ST-HEC Award 0444413, “Scalable, Interoperable Tools to Support Autonomic Optimization of High-End Applications”, Main PI S.A. McKee, co-PIs A. Malony (University of Oregon) and G.S. Tyson (University of Florida) \$750,000 (PI McKee amount \$329,670), 2004-2007.
  24. REU Supplement 0530488 to award NSF ST-HEC Award 0444413, Sole PI S.A. McKee, \$15,000, 2004.
  25. NSF ITR/NGS Medium Award 0325536, “Toward Autonomous Computing: System-Wide Hardware/Software Monitoring and Adaptation”, Main PI S.A. McKee, co-PI H.S. Lee (Georgia Institute of Technology), \$830,000 (PI McKee amount \$415,000), 2003-2008.
  26. REU Supplement 0434682 to NSF ITR/NGS Medium Award 0325536, Sole PI S.A. McKee, \$12,000, 2004.
  27. Cornell University Undergraduate Research Award, \$2,000, with Udit Agrawal, 2004.
  28. Cornell University Undergraduate Research Award, \$2,000, with David B. Hodgdon, 2004.
  29. Cornell University, President’s Council of Cornell Women Affinito-Stewart Junior Faculty Award, Sole PI S.A. McKee, \$9,500, 2003.
  30. AAAS/NSF Women’s International Science Cooperation Travel Grant, with Universitat Politècnica de Catalunya, Sole PI S.A. McKee, \$4,000, 2003.
  31. Cornell University, Cornell Information Technology Innovation in Teaching Grant, Sole PI S.A. McKee, 2003-2004.
  32. Small Business Initiative for Research (SBIR) Award, PIs: SRC Computers, Inc., \$15,000, Subcontract PI S.A. McKee, 2002.
  33. DOE Lawrence Livermore National Laboratory Center for Applied Scientific Computing award LLNL LDRD 01-ERD-043, PI B.R. de Supinski; collaborator: A. Yoo; “Overcoming the Memory Wall for SMP-Based Systems”. Subcontract PI S.A. McKee, \$238,000, 2001.
  34. Intel Foundation Equipment Donation, “The Impulse Memory Controller Project”, PI S.A. McKee, co-PI J.B. Carter, \$10,000, 2001.
  35. NSF CCR CSA Award 0073532, “Understanding and Improving Memory System Performance”, \$184,998, Sole PI S.A. McKee, 2000-2003.
  36. REU Supplement 0211668 to NSF CCR CSA Award 0073532, Sole PI S.A. McKee, \$5,000, 2002.
  37. NSF POWRE Award 9806043, “Understanding and Improving Memory System Performance”, Sole PI S.A. McKee, \$75,000, 1998-2000.

## Research Highlights

### **Models to Predict per-Core Power Consumption** 2008-present

PI: S.A. McKee

Diminishing performance returns and increasing power consumption of single-threaded processors have made chip multiprocessors (CMPs) an industry imperative. Unfortunately, low power efficiency and bottlenecks in shared hardware structures can prevent optimal use when running multiple sequential programs. For multithreaded programs, adding a core may harm performance *and* increase power consumption. To better exploit otherwise limitedly beneficial cores, software components such as hypervisors and operating systems can provide estimates of application performance and power consumption. They can use this information to improve system-wide performance and reliability and to estimate per-core power consumption. Advising K. Singh. Supported by NSF CNS Award 0509406.

### **Exploring the Microarchitectural Behavior of an Industrial Processor in the Presence of Transient Faults** 2008-present

PI: S.A. McKee Collaborators: M.K. Gschwind, V. Salapura

Soft errors are an ubiquitous, ever-increasing problem that will compromise future computing integrity at every echelon. Many architectures provide protection from these transient events for large arrays, such as register files and caches, but often, little is done to protect common latches from corruption, such as those used in configuration and in the pipeline. It is important that we identify the most vulnerable processor components at the latch level, so as to mitigate soft errors before they manifest in the architectural state. This research evaluates the vulnerability of latches within an IBM PowerPC-based processor core. We simulate a VHDL model of the processor, and use an RTX error injection method to inject bit-flips into the latch output nets at runtime. We then perform an analysis of the system's behavior while executing applications (paying particular attention to the floating point unit), and propose solutions to increase processor robustness. Advising C. Trammell. Supported by IBM graduate internships and IBM faculty fellowship.

### **Multi-Platform SimPoints to Enable More Thorough Architectural Design Studies** 2007-

PI: S.A. McKee

Developing multiplatform tools to generate Simulation Points (SimPoints) for accurate partial execution application simulation studies. We leverage the SimPoint methodology developed at UCSD, which is widely adopted and enables highly accurate partial-simulation experiments, greatly speeding thorough architectural simulation studies. We have examined three binary instrumentation tools for generating SPEC2000 and SPEC2006 SimPoints across nine implementations of the IA-32 architecture. We created our own plug-ins for two tools, Qemu and Valgrind, and we compare results to Intel's PinPoints. We validate our approaches via hardware performance counters, finding that some applications exhibit little phase behavior and others exhibit behavior too complicated for phase detection. Furthermore, we verify the UCSD finding that multiple SimPoints must be modeled to generate accurate results: we model up to 20 to achieve error rates below 5%. Current work focuses on developing SimPoints for many other platforms: for instance, we are close to having tools to generate MIPS SimPoints. Advising V.M. Weaver. Supported by NSF Awards ST-HEC 0444413 and CCF 0702616.

### **The Chameleon Shared Memory System** 2006-2008

PI: S.A. McKee Collaborators: J.E. Moreira, S. Chiras, and X. Shen

Developing a thin architectural layer to support shared memory in a Cell Broadband Processor-based blade system. We have implemented lightweight, FPGA-based hardware support for shared memory, enabling any processor to access SDRAM on any other blade via a DDR-2 memory controller and optical interconnect. This enables a lighter weight solution than tradi-

tional SMPs, since blades can be added one at a time. Likewise, it enables a more easily programmable system than clusters relying on message passing communication protocols. We thus attempt to deliver the best of both worlds (SMPs and clusters) at low cost. Current research focuses on programmability. Advising C.D. Dolen. Supported by IBM graduate internships and IBM Faculty Award.

**High Performance, Energy Efficient Memory Systems 2005-present**

PI: S.A. McKee Collaborator: G.S.Tyson

Exploring alternative cache organizations for lower-power memory hierarchies for embedded and multicore systems. We have developed a simple, scalable policy for implementing drowsiness (lowering voltage on most lines to save leakage power) and cache decay. Adding drowsiness and column associativity to region-based caches saves energy without sacrificing performance in embedded systems. Adding our scalable drowsiness mechanism also works well with traditional CPUs and traditional L1/L2 cache hierarchies. Our cache decay mechanism operates as a snoop filter in multicore systems, saving both dynamic and leakage power with minimal effect on performance. Advising M.B. Bhadauria. Supported by Canadian NSERC doctoral fellowship.

**Models for Understanding and Improving Computer Systems Behavior: Predicting Application Performance and Speeding Architectural Design Space Exploration 2003-2009**

PI: S.A. McKee

Investigating methods to reduce number of experiments required for predicting HEC (high-parameter) application behavior and studying architectural design space exploration. Growing system complexity combined with increasing usability and reliability requirements render many traditional architectural modeling techniques obsolete. Platforms affected range from embedded systems to desktops to high-throughput commercial systems to the high-end computing (HEC) systems that constitute our nation's most powerful supercomputers. Computer designs and accompanying workloads have grown sufficiently complex that modeling them fully in detail is simply intractable. We attack these problems via Machine Learning approaches to predictive modeling. We have applied such techniques to predicting application runtimes for large-scale parallel scientific codes with large parameter spaces, and to architectural design space exploration. In the former, we predict runtimes with 93-95% accuracies. For the latter, by sampling 1-2% of a full design space, we can predict IPC with 98-99% accuracies, on average. Continuing work focuses on making our automated approaches more efficient in their sampling rates and investigating full systems (software+hardware in tandem), as well as combining with statistical approaches to speed design space exploration. Advised E. Ipek. Advising K. Singh. Supported by NSF Awards ST-HEC 0444413 and CCF 0702616, and an internship at Lawrence Livermore National Lab.

**Using Native Execution to Fast-Forward Applications for Analysis or Simulation 2005-2007**

PI: S.A. McKee

Developing a very fast, retargetable approach for application fast-forwarding. Our first goal is speeding architectural simulation. Most acceleration techniques model only portions (samples or simulation intervals) of an application's execution in detail, either by estimating statistics for other execution segments or by only taking statistics from representative samples. These usually require modifying the simulation model, performing pre-characterization of modeled workloads, and/or modifying application binaries. These approaches are therefore tied to specific simulators or architectures, and are often difficult to extend to new tools or ISAs. To address these issues, we leverage Application-Level Checkpointing and native execution to fast-forward programs to simulation intervals on Alpha, x86, SPARC, and MIPS platforms. Checkpoint code is inserted in application source, a process less fragile than binary rewriting and requiring no additional simulation beforehand to create checkpoint state. Our second goal

is to allow precisely the same execution intervals to be examined in partial simulation experiments across platforms and regardless of optimizations used in compiling the target application. Advising V.M. Weaver. Supported by NSF ST-HEC Award 0444413.

#### **Understanding and Exploiting Phase Behavior of Parallel Programs** 2004-2006

PI: S.A. McKee                      Co-PI: J.F. Martínez                      Collaborator: B.R. de Supinski  
Exploring methods to identify phases in parallel programs at runtime and to use this information along with phase prediction to drive hardware reconfiguration. Much prior work has focused on dynamic phase-based behavior in uniprocessor or Simultaneous Multithreaded (SMT) applications, but we are the first to provide solutions for parallel applications. The project thus far addresses NUMA shared-memory systems, and is expanding to Symmetric Multiprocessors (SMPs), Message Passing (MP/MPI), and hierarchical systems. The impact of this work will affect our understanding of a range of parallel applications, and driving how we manage hardware reconfiguration. It will also increase programmer productivity, bringing parallel computing further into the mainstream. Advised M.S. student E. Ipek. Supported by NSF CNS Award 0509406 and an internship at Lawrence Livermore National Lab.

#### **Optimizing Applications Using High-Level Abstractions** 2003-2008

PI: D. Quinlan                      Co-PI: S.A. McKee  
Developing compiler analysis and transformations necessary to optimize adaptive mesh-based codes that use libraries of abstractions in C++. The use of high-level programming abstractions, such as matrices and mesh entities, is a key to achieving productivity in scientific applications. Unfortunately, such abstractions frequently obfuscate compiler analysis because of their pervasive use of pointers or because they are implemented in libraries for which source code is unavailable. Our work exploits the semantics of abstractions, as employed in unstructured mesh codes, to overcome the limits of compiler analysis and to guide domain-specific optimizations. Advised B.S. White. Supported by DOE Krell Institute HPCS Fellowship under grant number DE-FG02-97ER25308 and DOE LLNL subcontract B571234.

#### **System-Wide Hardware/Software Monitoring and Adaptation** 2003-present

PI: S.A. McKee                      Co-PI: H.S. Lee                      Collaborator: G.S. Tyson  
Conducting joint work with Georgia Tech to investigate reconfigurable, continuous hardware monitors and the software to exploit them. As microarchitectural and system complexity grows, comprehending system behavior becomes increasingly difficult, often requiring gathering and sifting through voluminous event traces or coordinating results from multiple, non-localized sources. We address this complexity with a framework that deploys programmable elements throughout a system, locating hardware monitors at event sources. Monitors run and writeback results autonomously with respect to the CPU, avoiding large system overheads of interrupt-driven monitoring and removing the need to communicate irrelevant events to higher software levels. The framework is applicable to a broad range of monitoring goals. Initial focus is on cluster communication and memory system performance: efficient memory access logging, runtime data collection for automatic optimization, memory access characterization through histograms, dynamic pattern recognition, heap access control, and network intrusion detection. Framework feasibility is supported by simulation results showing that, even with aggressive feedback, our monitors cause little system perturbation. Work with Florida State investigates lighter weight methods that deduce system information from monitoring a small number of signals withing the microprocessor. Advised C. Dolen and C. Trammell. Supported by NSF ITR/NGS Award 0325536.

#### **Next-Generation Memory Systems** 2003-present

PI: S.A. McKee  
Designing smarter memory systems to exploit information about memory access patterns. Currently developing seamless, easy to use alias management for address-remapping control-

lers in SMPs and CMPs. We have validated the coherence protocol that allows multiple aliased addresses to be alive at once in one or more caches and are conducting design-space studies. Advising P.K. Szwed. Supported by IBM Corp.

#### **Overcoming the Memory Wall for SMP Systems 2001-2002**

PI: B.R. de Supinski

Subcontract PI: S.A. McKee

Co-Investigators: F. Mueller, M. Schulz, A. Yoo

Led Utah/Cornell team developing better tools and metrics to evaluate memory behavior of parallel programs and design smarter SMP memory systems to exploit structured memory access patterns. Initial work created experimental infrastructure—in particular, a tool (METRIC) for dynamic partial address trace generation and analysis—and conducted initial studies of the memory system design space. Collaborated with SRC Computers, to investigate using reconfigurable processing elements to improve global memory performance. Advised T. Mohan and I. Kumar. Supported by NSF CCR CSA award 0073532, DOE LLNL LDRD award 01-ERD-043, and SBIR with SRC Computers.

#### **The Impulse Adaptable Memory System 1998-2002**

PI: J.B. Carter

Co-Investigators: S.A. McKee, W.C. Hsieh, A. Davis

Co-led team building an adaptable main-memory controller that improves utilization of processor caches and the system memory bus. By remapping unused physical addresses, the memory controller can access discontinuous data as if it were densely allocated, create superpages without copying, and aggressively prefetch within the memory controller without danger of cache pollution. Studied effects of DRAM prefetching and scheduling, guided design of Parallel Vector Access Unit and development of analytic models of performance and remapping costs/benefits, and drove dissemination of research results. Co-advised B.K. Mathew. Mentored several graduate students. Supported by DARPA Data Intensive Systems award.

#### **Speculative Stream Prefetching and Access Ordering 1999-2000**

PI: S.A. McKee

Investigated opportunities to optimize access order when detecting streams in hardware and prefetching them to cache from Rambus memory systems. Studied placing stream data in L2 and in a multilateral cache with smaller lines. Advised C. Zhang. Supported by NSF CCR CSA award 0073532.

#### **A New Approach to Cache Analysis 1996-1998**

PI: S.A. McKee

Co-investigator: Wm.A. Wulf

Developed an analysis methodology (viewing caches as filters) that provides the theory to support cache hierarchy design, along with mathematical tools and supporting software. Designed measures to graph locality in streams of memory requests, and developed tools to aid in the manipulation and interpretation of this data. Co-advised D.A.B. Weikle. Supported by NSF POWRE Award 9806043 and NSF CCR CSA award 0073532.

#### **Dynamic Multipath Architecture 1996-1998**

Co-investigators: H. Akkary and K. Chow

Investigated a speculative, out-of-order, multi-threaded processor model (Intel proprietary IP).

#### **The Stream Memory Controller (SMC) and the Weird Machine (WM) 1990-1996**

PI: Wm.A. Wulf

Designed/developed hardware support (the SMC) for dynamic access ordering, a technique for increasing memory efficiency for vector computations. Managed joint CS/EE SMC research group from 1995-96; managed CS side of project from 1994-96. Collaborated on the design of operating system and architectural support for security for the WM machine. Maintained and augmented WM compiler and simulator. Supervised masters students. Took the lead in pursuing a patent on foundations for this work (awarded November, 2000). Supported by NSF MIP award 9307626.

**The Plan 9 Operating System 1988**

Mentor: R. Pike

Added support for debugging to the Plan 9 operating system kernel, and then implemented an instruction-level debugger employing these kernel facilities. Supported by AT&T Bell Laboratories graduate internship.

**Research Advising*****Former Staff, Students, and Interns***

1. Martin Schulz, Ph.D., Technische Universität-München; Postdoc/Research Associate 2002-2004, Cornell University, projects: Hardware and Software for Efficient Memory Utilization in Uniprocessors and SMP Systems; System-Wide Monitoring and Adaptation; Middleware for Portable Parallel Programming. *Research Scientist at LLNL.*
2. Daniel J. Marques, Ph.D., Cornell University, Postdoctoral Research Associate, March-August 2006. project: Automatic Application-Level Checkpointing for High Performance Computing Solutions. *Research Staff Member at Univ. Texas at Austin.*

***Graduated Ph.D. Students***

3. Peter K. Szwed, M.S. 2001, Syracuse University. Ph.D. 2009, Cornell University, dissertation topic: An Intelligent Memory System for Symmetric Multiprocessors, 2003-present, *IBM Corp. Employee.*
4. Brian S. White, Ph.D. 2008, Cornell University, dissertation: *Improving Computational Intensity of Irregular Mesh-Based Scientific Applications.* *Dept. of Energy Krell Institute High-Performance Computer Science Fellow. Postdoctoral Fellow in Computational Bio-Physics, Cornell University.*
5. Dee A.B. Weikle, Ph.D. 2001, University of Virginia, dissertation: *A New Approach to Cache Analysis.* co-advised with Bill Wulf, 1997-2001. *Research Scientist at Univ. of Virginia.*

***Graduated Masters Students***

6. Catherine Trammell, M.S. 2009, Cornell University, thesis: *Exploring the Microarchitectural Behavior of an Industrial Processor in the Presence of Transient Faults.* *Engineer at NVidia Corp.*
7. Christopher D. Dolen, M.S. 2007, Cornell University, thesis: *The Chameleon Shared Memory System;* Ph.D. research area: System-Wide Monitoring and Adaptation, 2006-2007.
8. I-Chun Li, M.E. 2006, Cornell University, project: Converting a Cache Performance Analysis Tool to Use Valgrind for Application Trace Generation. *Engineer at S3 Graphics.*
9. Engin Ipek, B.S. 2003, M.S. 2005, Cornell University, thesis: *Efficiently Exploring Architectural Design Spaces via Predictive Modeling.* *Research Scientist at Microsoft Corp.*
10. Amy Henning, M.E. 2005, Cornell University, research project: BlueGene/L: Improving Application Memory Performance on a Massively Parallel Machine. *Lawrence Livermore National Lab Fellow. Member of Technical Staff at IBM Corp.*
11. Yong Hu, M.S. 2004, Cornell University, thesis: *Andromeda: a VIA-Based Software DSM System with Multithreading and Page Prefetching.* *Member of Technical Staff at Oracle, Inc.*
12. Philip Sieh, M.E. 2004, Cornell University, project: Personal Inertial Navigation System.

13. Abhijeet Dhanapune, M.E. 2004, Cornell University, project: Performance Evaluation of Routing Protocols and Methods of Energy Conservation in MANETs.
14. Robert M. Buels, M.E. 2004, Cornell University, project: A Computer Vision System for Tracking Multiple Identical Zebrafish.
15. Venkata Tumati, M.E. 2004, Cornell University, project: MPEG4 Performance Analysis.
16. Biren Patel, M.E. 2004, Cornell University, project: Electronic Throttle Body.
17. Brad Kopek, M.E. 2003, Cornell University, project: The Common Messaging Layer over the Scalable Coherent Interface.
18. Jeremiah G. Ronquillo, M.E. 2003, Cornell University, project: Graphical User Interface for the emulegOS Capture the Flag Simulator.
19. Peter Wang, M.E. 2003, Cornell University, project: RF Communications Augmentation of the Lego Mindstorm RCX.
20. Tushar Mohan, M.S. 2003, University of Utah, thesis: *Detecting and Exploiting Memory Reference Regularity*.
21. Indrajeet Kumar, M.E. 2002, University of Utah, project: Balancing Memory Activity and Computation in Reconfigurable Co-Processors.
22. Binu K. Mathew, M.S. 2000, University of Utah, thesis: *Design of a Parallel Vector Access Unit*. co-advised with Al Davis.
23. Chengqiang Zhang, M.E. 2000, University of Utah, project: Hardware-Only Stream Prefetching and Dynamic Access Ordering.
24. Hua Wang, M.E. 2001, University of Utah, project: Tools for a New Approach to Cache Analysis.

#### ***Graduated Undergraduate Students***

25. D. Elias Bermudez, B.S. 2008, Cornell University, project: Pervasive System Monitoring, and Next-Generation Memory System Design, summer 2007-2008. *Cornell University Engineering Learning Initiatives Fellow*.
26. David J. Drew, B.S. 2008, M.E. 2009, Cornell University, projects: Compiling for C++ and Benchmark Suite Composition; High Performance, Energy Efficient Memory Hierarchies, 2006-2008.
27. Siu Yu Cherie Kwan, B.S. 2008, Cornell University, project: Statistical Modeling of Architectural Parameter Correlations, 2006-2007. *Cornell University Engineering Learning Initiatives Fellow*.
28. Christopher D. Leary, B.S. 2008, Cornell University, projects: Building a Python-Based Graphical Interface for the Jgraph Graph Description Language; Hardware Support for Detecting Software Memory Access Bugs, spring 2007-2008.
29. Richard Yu, B.S. 2008, Cornell University, project: Learning the Ropes of Computer Systems Research. *Cornell Faculty Undergraduate Research Grant Fellow*.
30. Daniel Fitzgerald, B.S. 2007, Cornell University, project: Effective Communication and Dissemination of Research Results, summer 2006.
31. Daniel Lee, B.S. 2007, Cornell University, project: Analyzing Dynamic Caching Efficiency on Modern Systems, summer 2005. *Cornell University Engineering Learning Initiatives Fellow*.
32. James Juwon Lee, B.S. 2007, Cornell University, project: Compiling for C++ and Benchmark Suite Composition, summer 2006. *Cornell University Engineering Learning Initiatives Fellow*.

33. Udit Agrawal, B.S. 2006, Cornell University, projects: Debugging and Testing an RF Interface for LEGO Mindstorm Robots; Faster Architectural Simulation Fast-Forwarding, 2003-2005. *Cornell University Learning Initiatives for Future Engineers Fellow*.
34. Pamela Chuang, B.S. 2006, Cornell University, project areas: A User Interface for Configuring Reconfigurable Monitors; Faster Architectural Simulation Fast-Forwarding; Translating and Optimizing a Task Scheduling Algorithm (Visual Basic/Windows to C/Linux). *Cornell University Engineering Life Initiatives Fellows/NSF REU student*.
35. Mark A. Berger, B.S. 2006, M.E. 2007, Cornell University, project areas: Exploring Hardware Assists for Exploiting Data Locality; Faster Architectural Simulation Fast-Forwarding, 2004-2005. *NSF REU student*.
36. Pete J. Poulos, B.S. 2005, University of Utah, project: Simulation Tools to Model Adaptable Memory Controllers in SMP Systems, 2001.
37. David B. Hodgdon, B.S. 2004, Cornell University, project areas: Distributed Shared Memory Clusters, and Porting the DynInst Toolset to the Macintosh OS-X.
38. Michael S. King, B.S. 2002, University of Utah, project: Simulation Tools to Model Adaptable Memory Controllers in SMP Systems, summer 2001.

#### ***Graduated Undergraduate Summer Interns***

39. Laura Grit, B.S. 2001, Hope College, Ph.D. 2008, Duke University, project: Analyzing Performance Differences of Executables Generated with Different Research Compilers, 2000. *CRA Distributed Mentor Project intern*.
40. Larissa Amy, B.S. 2000, Bucknell University, M.S. 2005, University of Virginia, project: An Interactive Pattern Matching Tool to Facilitate Memory Trace Analysis, 1999. *CRA Distributed Mentor Project intern*.
41. Gergana Markova, B.S. 2000, M.S. 2002, Purdue University, project: Tuning an Architectural Simulator to Realistically Model I/O Latencies, 1999. *CRA Distributed Mentor Project intern*.

#### ***Current Students***

##### ***Graduate Students***

1. Major B. Bhadauria, M.S. 2007, Ph.D. 2009, Cornell University, thesis: *High Performance, Low Power Memory Hierarchies for Embedded Systems and CMPs*, dissertation: *Thread Scheduling for Performance/Power Tradeoffs in Heterogeneous Chip Multiprocessors*. *Canadian NSERC Graduate Fellow*.
2. Karan Singh, M.S. 2007, Ph.D. 2009, Cornell University, M.S. thesis: *Predicting Parallel Application Performance via Machine Learning Approaches*, dissertation: *Prediction Strategies for Power-Aware Computing on Multicore Processors*. *Tau Beta Pi Fellow*.
3. Vincent Weaver, M.S. 2007, Ph.D. 2009, Cornell University, research area: Tools for More Efficient Computer Architecture Design, 2004-present.
4. Nana B. Sam, M.S. 2003, Cornell University. Ph.D. student, Cornell University, dissertation: *Statistical Approaches to Predicting Microarchitectural Performance*, 2006-present (on family leave). *Intel Corp. Employee*.

##### ***Undergraduate Students***

5. Huang Yu Ku, B.S. 2009, Cornell University, project: Statistical Modeling of Application Behavior for Architectural Design Space Exploration, summer 2006.

6. Ruke Ufomata, B.S. 2009, Cornell University, project: Porting a Task Scheduling Program from Visual Basic and Optimizing Performance, 2006-2007. *Cornell University Engineering Learning Initiatives Fellow*, 2006-2007. *Cornell Presidential Research Scholar* 2007-2009.
7. William Baughman, B.S. 2009, Cornell University, project: Developing an Eclipse Open Source-Based GUI for the Jgraph Postscript Graphing Language, summer 2007.
8. Cathy Chen, B.S. 2009, Cornell University, project: Studying Custom Memory Hierarchy Design for Chip Multiprocessor Based Personal Electronics, 2007-2008. *Cornell University Engineering Learning Initiatives Fellow*.
9. Alexis A. Collins, B.S. 2009, Cornell University, project: Studying Custom Memory Hierarchy Design for Chip Multiprocessor Based Personal Electronics, 2007-2008. *Cornell University Engineering Learning Initiatives Fellow*.
10. Chris Fromann, B.S. 2009, Cornell University, project: Learning the Ropes of Computer Systems Research, summer 2007.
11. Jessica Loeb, B.S. 2009, Cornell University, project: Studying Custom Memory Hierarchy Design for Chip Multiprocessor Based Personal Electronics, 2007-2008.

## Teaching Experience

### Chalmers University of Technology, Gothenburg, SE

Instructor, EDA281, "Parallel Computer Organization and Design"  
1 doctoral student, 10 masters students, winter 2009

### Cornell University, Ithaca, NY

Instructor, ENGRD150, "Engineering Seminar"  
16 freshmen, fall 2007

18 freshman students, fall 2003

Instructor, ECE685, "Memory Technologies and Systems"

6 Ph.D. students, 5 undergraduates, fall 2007

10 graduate (doctoral and MEng) students, 2 undergraduates, fall 2006 (taught as ECE 699)

7 doctoral students, 2 MEng students, fall 2005 (taught as ECE 699)

Instructor, ECE/COMS314, "Computer Organization"

155 undergraduate students (one Physics graduate student), spring 2007

172 undergraduate students, spring 2006

138 undergraduate students (one graduate ORIE student), spring 2005

140 undergraduate students, spring 2004

Instructor, ECE595, "Real-World Engineering"

18 M.E. students, spring 2003

28 M.E. students, fall 2003

This pilot course strove to instill confidence along with communication, teamwork, and problem solving skills appropriate for careers in industry. The vehicle for learning and practicing these skills is studying the hardware/software interface, where the hardware is a LEGO Mindstorm robot with a Hitachi H8 series microprocessor, and the software is BrickOS or C application programs. Students design and implement a "Capture the Flag" game and make videotaped oral presentations, multiple written reports, and team web portfolios.

### University of Utah, Salt Lake City, UT

Instructor, CS5460, "Operating Systems"

70 undergraduate students, 10 graduate students, fall 2000

Co-Instructor, CS6935, "Computer Systems Seminar"  
20 graduate students/staff, spring 1999  
12 graduate students/staff, spring 1998

### **Oregon Graduate Institute, Portland, OR**

Instructor, CSE585, "Advanced Memory Systems Architecture"  
10 graduate students, fall 1997  
Instructor, CSE522, "Advanced Computer Architecture"  
12 graduate students, spring 1997

### **Reed College, Portland, OR**

Co-Instructor, MATH442, "The Computer Science of Video Games"  
12 undergraduate students, spring 1998  
Dylan McNamee (then Asst. Prof. in CSE Dept. at OGI) and I created this broad, capstone course to teach Reed undergraduates fundamentals of Computer Science.

### **University of Virginia, Charlottesville, VA**

Instructor, CS216, "Program and Data Representation"  
12 undergraduate students, summer 1995  
Teaching Assistant, CS360, "Computer Organization"  
40 undergraduate students, fall 1990

### **Princeton University, Princeton, NJ**

Section Designer/Instructor, CS217, "Systems Programming and Computer Organization"  
approximately 15 undergraduate students, 1998  
At Princeton, I created and taught an experimental lecture/discussion for the systems programming course. This format proved very successful; the course was taught this way for many years.  
Teaching Assistant, CS217, "Systems Programming and Computer Organization"  
approximately 45 undergraduate students, 1997

### **Invited Talks**

1. "Accommodating Diversity in CMPs with Heterogeneous Frequencies", HiPEAC International Conference on High Performance Embedded Architectures and Compilers, CY, January 2009.
2. "Building Smarter Memory Systems from the Ground Up", Chalmers University of Technology, June 2008.
3. "My Quest to Become a Good Teacher", Cornell Engineering Academic Excellence Workshops, October 2007.
4. "Using Dynamic Binary Instrumentation to Generate Multiplatform Simulation Points", University of Wisconsin, September 2007.
5. "Constructing Application Performance Models Using Neural Networks", Schloss Dagstuhl International Conference and Research Center for Computer Science, Seminar 07341, Code Instrumentation and Modeling for Parallel Performance Analysis, August 2007.
6. "Architectural Design Space Exploration via Predictive Modeling", University of California at Irvine, January 2007.
7. "Managing Complexity: Applying Predictive Modeling to Problems in Computer Engineering", Cornell University, January 2006 (Electrical and Computer Engineering Faculty Retreat).
8. "Architectural Design Space Exploration via Predictive Modeling", University of Illinois at Urbana-Champaign, December 2006.

9. \_\_\_\_, University of Virginia, November 2006.
10. \_\_\_\_, University of Michigan, November 2006.
11. \_\_\_\_, Massachusetts Institute of Technology, November 2006.
12. \_\_\_\_, Sun Microsystems, October 2006.
13. \_\_\_\_, Stanford University, October 2006.
14. \_\_\_\_, University of Rochester, September 2006.
15. “Memory System Optimizations for Performance and Low Power in Multicore-Based High-End Systems”, Computing Technologies Institute, Chinese Academy of Sciences, Beijing, CN, June 2006.
16. “Architectural Design Space Exploration via Predictive Modeling”, Computing Technologies Institute, Chinese Academy of Sciences, Beijing, CN, June 2006.
17. \_\_\_\_, INRIA Futurs Research Center, France, May 2006.
18. “Dynamic Program Phase Detection in Distributed Shared-Memory Multiprocessors”, Rhodes, GR, April 2006 (invited workshop presentation).
19. “Architectural Design Space Exploration via Predictive Modeling”, IBM TJ Watson Research Center, Yorktown Heights, NY, February 2006.
20. \_\_\_\_, Cornell University, Ithaca, NY, February 2006.
21. “Owl: Next-Generation System Monitoring”, Ischia, IT, May 2005 (conference presentation).
22. “The Importance of ASC Funding to Computer Science Research”, Santa Fe, NM, October 2005 (Annual Los Alamos Computer Science Institute Symposium (LACSI) panel presentation).
23. “Architectural Design Space Exploration via Predictive Modeling”, Princeton University, Princeton, NJ, November 2005.
24. “An Approach to Performance Prediction for Parallel Applications”, Lisbon, PO, August 2005 (conference presentation).
25. “Owl: An FPGA Prototype for Next-Generation System Monitoring”, Ohio Supercomputer Center-Springfield Operations Status Meeting, Lawrence Livermore National Laboratory, Livermore, CA, July 2005.
26. “Reflections on the Memory Wall”, ACM Computing Frontiers, Ischia, IT, April 2004 (invited special session presentation).
27. “Putting the ‘Real’ Into ‘Real-World Engineering’: Introducing Electronic Student Portfolios to Assess Student Learning”, Cornell University, Ithaca, NY, October 2003 (Learning and Teaching with Technology EXPO presentation).
28. “Perspectives on the Memory Wall Problem”, Glen Eden, OR, April 2003 (Salishan Department of Energy High Speed Computing Conference invited conference presentation).
29. “An MPEG-4 Performance Study”, Austin, TX, March 2003 (conference presentation).
30. Young Researcher’s Panel, Baltimore, MD, November 2002 (15th ACM/IEEE Conference on Supercomputing panel presentation).
31. “MPEG4: Fallacies and Paradoxes”, Austin, TX, November 2002 (workshop presentation).
32. “A Parallel Vector Access Memory System”, the Pennsylvania State University, State College, PA, October 2002.
33. “Smarter Memory Controllers: a Parallel Vector Access Memory System”, Cornell University, Ithaca, NY, April 2002.
34. \_\_\_\_, University of Pittsburgh, Pittsburgh, PA, April 2002.

35. \_\_\_\_, IBM T.J. Watson Research Center, Yorktown Heights, NY, April 2002.
36. \_\_\_\_, University of California at Davis, Davis, CA, March 2002.
37. \_\_\_\_, Lawrence Livermore National Lab, Livermore, CA, March 2002.
38. \_\_\_\_, Brown University, Providence, RI, February 2002.
39. “Impulse: Building a Smarter Memory Controller”, University of British Columbia, Vancouver, BC, January 2002.
40. “Partial Data Traces: Efficient Generation and Representation”, Barcelona, ES, September 2001 (workshop presentation).
41. “Smarter Memory Controllers: Improving Memory System Performance from the Bottom Up”, Technische Universität-München, Munich, DE, June 2000.
42. \_\_\_\_, Universitat Politècnica de Catalunya, Barcelona, ES, January 2000.
43. \_\_\_\_, Lawrence Livermore National Laboratories, Livermore, CA, December 1999.
44. \_\_\_\_, University of Illinois at Urbana-Champaign, Urbana, IL, September 1999.
45. “Graduate School: Why Go, What to Look for, What to Expect”, Purdue University, West Lafayette, IN, September 1999.
46. “Maximizing Effective Memory Bandwidth for Streaming Computations”, University of California at Santa Barbara, Santa Barbara, CA, November 2001.
47. \_\_\_\_, University of Rochester, Rochester, NY, December 2001.
48. \_\_\_\_, University of Rhode Island, Kingston, RI, February 2002.
49. \_\_\_\_, Vanderbilt University, Nashville, TN, spring 1998.
50. \_\_\_\_, University of British Columbia, Vancouver, BC, spring 1996.
51. \_\_\_\_, University of California at Davis, Davis, CA, spring 1996.
52. \_\_\_\_, University of Minnesota, Minneapolis, NM, spring 1996.
53. \_\_\_\_, Oregon Graduate Institute, Hillsboro, OR, spring 1996.
54. \_\_\_\_, Harvey Mudd College, Claremont, CA, spring 1996.
55. \_\_\_\_, Intel Corp., Portland, OR, spring 1996.
56. “How Virtual Memory Really Works”, Reed College, Portland, OR, spring 1998.
57. \_\_\_\_, Harvey Mudd College, Claremont, CA, spring 1996.
58. “The Stream Memory Controller”, Harvey Mudd College, Claremont, CA, spring 1996.
59. \_\_\_\_, Intel Research Forum, Portland, OR, April 1996.
60. “Access Order and Effective Bandwidth for Streams on a Direct Rambus Memory”, Orlando, FL, January 1999 (conference presentation).
61. “Caches as Filters: A New Approach to Memory Hierarchy Analysis”, Montreal, QB, July 1998 (conference presentation).
62. “Design and Evaluation of Dynamic Access Ordering Hardware”, Philadelphia, PA, May 1996 (conference presentation).
63. “A Memory Controller for Improved Performance of Streamed Computations on Symmetric Multiprocessors”, Honolulu, HI, April 1996 (conference presentation).
64. “Compiling for Efficient Memory Utilization”, San Jose, CA, February 1996 (workshop presentation).
65. “Bounds on Memory Bandwidth in Streamed Computations”, Stockholm, SE, September 1995 (conference presentation).

66. "Access Ordering and Memory-Conscious Cache Utilization", Raleigh, NC, January 1995 (conference presentation).
67. "Increasing Memory Bandwidth for Vector Computations", Zurich, CH, March 1994 (conference presentation).
68. "Adding Debugging Support to the Plan 9 Operating System", Princeton, NJ, fall 2008.

## Professional Activities

### Member

International Federation for Information Processing (IFIP) Working Group 10.3, 2009-present.

### Advisory Committee Member

IEEE Technical Committee on Computer Architecture, 2001-2006.

### Board Member at Large

ACM SIGMICRO, 2005-present.

### Editorial Board Member

Springer *International Journal on Parallel Processing (IJPP)*, 2005-present.

### Guest Editor

S.A. McKee, *Journal of Instruction Level Parallelism (JILP)*, vol. 10, June 2008.

S.A. McKee, *ACM Transactions on Emerging Technologies (JETC)*, 3(2), July 2007.

S.A. McKee, *EC Transactions on High Performance Embedded Architectures and Compilers (Trans. HiPEAC)*, 2(1) 2007 (special section). Springer *Lecture Notes in Computer Science* 4367.

S.A. McKee, Springer *International Journal of Parallel Programming (IJPP)*, 35(3), June 2007.

S.A. McKee, with M. Schulz, B. Childers, K. Inoue, *ACM SIGArch Computer Architecture News*, 30(3), June 2002 (Proc. HPCA'02 Work in Progress Session).

S.A. McKee, with M. Schulz, B. Childers, *IEEE Technical Committee on Computer Architecture (TCCA) Newsletter*, October 2001 (Proc. PACT'01 Work in Progress Session).

S.A. McKee, *IEEE Technical Committee on Computer Architecture (TCCA) Newsletter*, spring 2000 (Proc. HPCA'00 Work in Progress Session).

### Steering Committee Member

ACM International Conference on Computing Frontiers (CF), May 2005-present.

IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), October 2002-October 2004.

### General Chair/Co-Chair

ACM/IEEE/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT) (with Martin Schulz, Lawrence Livermore National Laboratory), September 2009.

### Program Committee Chair/Co-Chair

ACM International Conference on Supercomputing (ICS) (with Bronis R. de Supinski, Lawrence Livermore National Laboratory), May 2011.

ACM International Conference on Computing Frontiers (CF), May 2006.

New Investigator Papers, ACM/IEEE Grace Murray Hopper Celebration of Women in Computing (GHC), October 2004.

IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT) (with Erik Altman, IBM T.J. Watson Research), September 2002.

#### Program Committee Member

ACM/IEEE International Symposium on Computer Architecture (ISCA), PC Chair: Wen-mei Hwu, June 2008.

ACM International Conference on Computing Frontiers (CF), May 2006.

IEEE International Parallel and Distributed Processing Symposium (IPDPS), PC Chair: Yves Robert, Architecture Track Vice-Chair, David Kaeli; April 2008.

ACM SIGPLAN Workshop on Memory Systems Performance and Correctness (MSPC), with ACM 13th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), PC Chair: Brad Chen; March 2008.

Workshop on Design, Architecture, and Simulation of Chip Multiprocessors (dasCMP), with IEEE/ACM 40th Symposium on Microarchitecture (MICRO), PC Co-Chairs: Norman Jouppi, Rakesh Kumar, and Dean Tullsen; December 2007.

Workshop on Experimental Computer Science (ExpCS), with the ACM Federated Computer Research Conferences (FCRC), PC Co-Chairs Dror Feitelson and Larry Rudolf; June 2007.

Second Workshop on Modeling, Benchmarking, and Simulation (MoBS), with the ACM/IEEE International Symposium on Computer Architecture (ISCA), PC Co-Chairs: Lieven Eeckhout and Joshua Yi; June 2007.

First Workshop on Statistical and Machine learning approaches applied to ARchitectures and compilaTion (SMART), with EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), PC Co-Chairs: John Cavazos and Grigori Fursin; February 2007.

2nd Annual EC International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), PC Co-Chairs: Per Stenström and David Whalley; February 2007. Springer *Lecture Notes in Computer Science* 4367.

IEEE International Parallel and Distributed Processing Symposium (IPDPS), PC Chair: Arnold Rosenberg, Architecture Track Vice-Chair: Allan Gottlieb; April 2006.

4th Workshop on Memory Performance Issues (WMPI'06), with IEEE Symposium on High Performance Computer Architecture (HPCA), PC Co-Chairs: John B. Carter and Lixin Zhang; February 2006.

1st Workshop on Introspective Architectures (WISA'06), with IEEE Symposium on High Performance Computer Architecture (HPCA), PC Co-Chairs: Hsien-Hsin Lee, Trevor Mudge, and Milos Prulovic; February 2006.

ACM Workshop on Memory Performance: Dealing with Applications, Systems, and Architecture (MEDEA), with IEEE/ACM International Conference on Parallel Architectures and Compilation Techniques (PACT), PD Co-Chairs: Sandro Bartolini and Roberto Giorgi; September 2005.

IEEE International Conference on Computer Design (ICCD), PC Co-Chairs: David Brooks and Michael Gschwind; October 2005.

ACM International Conference on Supercomputing (ICS), PC Chair: Larry Rudolph; June 2005.

IEEE International Workshop on Interaction between Compilers and Architectures (INTERACT), with IEEE Symposium on High Performance Computer Architecture (HPCA), PC Chair: Wei Chung Hsu; February 2005.

IEEE International Symposium on High Performance Computer Architecture (HPCA), PC Chair: Jose Duato; February 2004.

IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), PC Co-Chairs: Mary Hall and Vivek Sarkar; September 2003.

IEEE International Symposium on Modeling, Analysis and Simulation of Computers and Telecommunication Systems (MASCOTS), PC Chair: David Nicol; August 2001.

IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), PC Chair: Mary Lou Soffa; October 2000.

IEEE International Conference on Parallel Processing (ICPP), PC Chair: David Lilja; August 2000.

Workshop on Solving the Memory Wall Problem, with ACM/IEEE International Symposium on Computer Architecture (ISCA), PC Co-Chairs Haldun Hadimioglu and David Kaeli; June 2000.

IEEE International Symposium on High Performance Computer Architecture (HPCA), PC Chair: Kai Li; January 2000.

IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), PC Co-Chairs: Paraskevas Evripidou and Gabby Silberman; October 1999.

IEEE International Conference on Computer Design (ICCD), PC Chair: Lizy John; October 1999.

IEEE/ACM International Workshop on Computer Architecture for Machine Perception (CAMP), PC Chair: Charles Weems; October 1997.

#### Workshops Chair

ACM/IEEE International Symposium on Computer Architecture (ISCA), June 2008.

ACM/IEEE International Symposium on Computer Architecture (ISCA), June 2004.

#### Treasurer/Registration Chair

ACM International Conference on Computing Frontiers (CF), May 2005.

#### Publications Chair

ACM International Symposium on Microarchitecture (MICRO-38), November 2005.

IEEE International Symposium on High Performance Computer Architecture (HPCA), January 2001.

IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT), October 1999.

#### Publicity Chair

First International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), November 2005.

IEEE/ACM/IFIP International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2001.

## Workshop/Session Organizer

CRA/CDC/NSF/Intel/IBM Computer Architecture Summer School Workshop (with I. Bahar, Brown University; M.J. Irwin, The Pennsylvania State University; R. Joseph, Northwestern University; M.R. Martonosi, Princeton University; L. Peh, Princeton University; and K. Shaw, University of Richmond; supported by NSF *Broadening Participation in Computing*), July 2006.

IEEE International Symposium on High Performance Computer Architecture (HPCA) Work In Progress Session, February 2002.

IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT) Work In Progress Session, September 2001.

ACM/IEEE Grace Murray Hopper Celebration of Women in Computing CRA DMP Mentoring Workshop, September 2000.

IEEE International Symposium on High Performance Computer Architecture (HPCA) Work In Progress Session, January 2000.

## Scholarship Committee

ACM/IEEE Grace Murray Hopper Celebration of Women in Computing (GHC), September 2000.

## Government/Industry/International Invitation-Only Workshops

Seminar 07341: Code Instrumentation and Modeling for Parallel Performance Analysis, Schloss Dagstuhl, DE, August 2007.

DOE High Speed Computing Conference (Salishan), Glen Eden Beach, OR, April 2007.

Los Alamos Computer Science Institute (LACSI), Santa Fe, NM, October April 2005.

DOE High Speed Computing Conference (Salishan), Glen Eden Beach, OR, April 2005.

DOE High Speed Computing Conference (Salishan), Glen Eden Beach, OR, April 2004.

DOE High Speed Computing Conference (Salishan), Glen Eden Beach, OR, April 2003.

DOE/CRA High-End Computing Revitalization Task Force (HECRTF), Washington, DC, June 2003.

DOE Scientific Case for Large-Scale Simulation (SCaLeS), Arlington, VA, June 2003.

Intel High-End Computing Roundtable, Chantilly, VA, August 2003.

## Reviewing Activities

Countless reviews for top conferences, journals, and ad hoc external proposal reviews (impossible to track), plus service on NSF and LLNL proposal review panels, 1990-present.

## University Service

### **Cornell University, Ithaca, NY**

School of Electrical and Computer Engineering

Member of graduate committees:

M. Watkins, B. Keller, S.J. Jackson, C.C. LaFrieda, A. Browder (ECE, M.S. 2007), G. Bronevetsky (CS, Ph.D. 2006), R. Fernandes (CS, Ph.D. 2006), M. Khalili (ECE, Ph.D. 2005), J.R. Teifel (ECE, Ph.D. 2004).

Undergraduate Advising, 2003-present.

Electrical and Computer Engineering Computing Committee, 2003-present.

Computer Science Field Qualifying Exam Committee, 2003.

Computing Research Association Representative, 2002-present.

## **University of Utah, Salt Lake City, UT**

School of Computing

Member of graduate committees:

Z. Fang (CS, Ph.D. 2006), B. Chandramouli (CS, M.S. 2002), V.S. Pingali (CS, M.S. 2002), L. Schaelicke (CS, Ph.D. 2001), L. Zhang (CS, Ph.D. 2003);

Graduate Studies Committee, 2001-2002.

Graduate Recruiting, 2001-2002.

Ph.D. Qualifying Exam Committee, fall 2000.

Computer Policy Committee, 1999-2000.

Graduate Recruiting Committee, 1998-1999 (co-organized Graduate Recruiting Visit).

Faculty Recruiting Systems Subcommittee, 1998-1999.

ACM Student Programming Competition

Utah Assistant Coach, November 1999.

Regional Competition Judge, November 1999.

Intermountain Junior Science and Humanities Competition

Judge, 1999.

## **University of Virginia, Charlottesville, VA**

Computer Science Department

Member of graduate committees:

D.A.B. Weikle (CS, Ph.D. 2001), S. Hong (EE, M.S. 1999).

Undergraduate Curriculum Committee, 1993-1995.

Library Committee, 1992-1995.

Youth Summer Enrichment Program: Laboratory Instructor, 1994.

## **Professional Society Memberships**

Association for Computing Machinery (SIGARCH, SIGMICRO)

International Association for Electrical and Electronics Engineers Computer Society (TCCA, WIE), Senior Member

American Association of University Women

American Association for the Advancement of Science