

Major B. Bhaduria

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Research Interests

- Computer system architecture design and modeling
- Power efficient computing systems
- Software/hardware evaluation
- Thread and hardware resource scheduling

Awards

- NSERC Postgraduate Scholarship-Doctoral (PGS-D) Fellowship Award 2008-2010

Education

- B.A.Sc. Computer Engineering, University of Toronto, May 2004
- M.S. Computer Engineering, Cornell University, May 2008
 - Thesis: *High Performance Techniques for Reducing Cache Power*
- Ph.D. Computer Engineering, Cornell University, Expected August 2009
 - Dissertation: *Thread Scheduling for Chip Multiprocessors*

Professional Experience

- Cornell University, Ithaca, NY
 - 08/2005-present MS/PhD student, Graduate Research Assistant
- Microsoft Research, Redmond, WA
 - 06/2007-09/2007 (summer) Intern Researcher
- ICNexus, Taipei, Taiwan
 - 05/2004-08/2005 ASIC Design Engineer
- ATI Technologies, Markham, ON, Canada
 - 05/2002-08/2003 Associate Engineer, Integrated Circuit & Dev. Group
- HR Branch, Ministry of Community and Social Services, Toronto, ON, Canada
 - 05-08/2001 (summer) I.T. Consultant
 - 05-08/2000 (summer) Systems Officer

Industry Skills

- Logic design and synthesis of VHDL and Verilog netlists, FPGA, Motorola 68k, ARM processors
- C++, C, Java, PERL, TCL, MATLAB, Assembler, SQL, shell script, HSPICE

Publications in Refereed Conferences, Workshops & Journals

1. M. Bhadauria, V. Weaver, S.A. McKee, "**PARSEC: Hardware Profiling for CMP Design**", *Poster at International Conference on Supercomputing*, Yorktown Heights, NY, June, 2009
2. K. Singh, M. Bhadauria, S.A. McKee, "**Prediction-based Power Estimation and Scheduling for CMPs**", *Poster at International Conference on Supercomputing*, Yorktown Heights, NY, June, 2009
3. M. Bhadauria, V. Weaver, S.A. McKee, "**Accommodating Diversity in CMPs with Heterogeneous Frequencies**", *HiPEAC International Conference on High Performance Embedded Architectures and Compilers*, Cyprus, January, 2009
4. K. Singh, M. Bhadauria, S.A. McKee, "**Real Time Power Estimation and Thread Scheduling via Performance Counters**", *Workshop on Design, Architecture, and Simulation of Chip Multi-Processors*, at MICRO-41, Italy, November, 2008
5. M. Bhadauria, S. A. McKee, "**Optimizing Thread Throughput for Multithreaded Workloads on Memory Constrained CMPs**", *ACM International Conference on Computing Frontiers*, Ischia, Italy, May, 2008.
6. M. Bhadauria, S. A. McKee, K. Singh, G.S. Tyson, "**Data Cache Techniques to Save Power and Deliver High Performance in Embedded Systems**", *Transactions on High-Performance Embedded Architectures and Compilers*, 2(1):62-81, 2007.
7. M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, "**Leveraging High Performance Data Cache Techniques to Save Power in Mobile Embedded Systems**" *HiPEAC International Conference on High Performance Embedded Architectures and Compilers*, Belgium, January, 2007, pp.23-37.
8. M. Bhadauria, S.A. McKee, K. Singh, G.S. Tyson, "**A Precisely Tunable Drowsy Cache Management Mechanism**", *IBM P= ac^2 (P= Power/Performance, a = architecture, and c^2 =circuits/compilers) Conference*, October, 2006.

Technical Reports

1. M. Bhadauria, R. Huang, S. A. McKee, "**Improving Performance and Energy through Multithreaded Program Scheduling**", *Cornell Computer Systems Lab Technical Report CSL-TR-2008-1053*, September, 2008
2. M. Bhadauria, V. Weaver, S.A. McKee, "**A Characterization of the PARSEC Benchmark Suite for CMP Design**", *Cornell Computer Systems Lab Technical Report CSL-TR-2008-1052*, September 2008

Research Work

1. Modified simulators to implement region caches, snoop directory cache coherence protocols, alternate caching structures and bloom filters. Implemented memory controller modeling DDR2 memory and memory access scheduling for multithreaded benchmarks.
2. Used performance counters to measure throughput of CMPs, predict per core power consumption and identify memory bottlenecks. Characterized benchmark suites using performance counters on real hardware and simulators, pinpointing architectural bottlenecks in modern computer systems.