

Table of Contents

Chapter 1	Introduction.....	1
1.1	Distributed Shared Memory.....	2
1.2	Cache Coherence Protocol Design Space.....	4
1.3	Evaluating the Cache Coherence Protocols.....	6
1.4	Research Contributions.....	7
1.5	Organization of the Dissertation.....	8
Chapter 2	Cache Coherence Protocols.....	10
2.1	The Cache Coherence Problem.....	10
2.2	Directory-Based Coherence.....	12
2.3	Bit-vector/Coarse-vector.....	16
2.4	Dynamic Pointer Allocation.....	21
2.5	Scalable Coherent Interface.....	25
2.6	Cache Only Memory Architecture.....	32
2.7	Which Protocol is Best?.....	36
Chapter 3	FLASH Architecture.....	37
3.1	An Argument for Flexibility.....	37
3.2	FLASH and MAGIC Architecture.....	38
3.3	MAGIC Subsystem Protocol Support.....	46
3.3.1	Processor Interface.....	46
3.3.2	Network Interface.....	49
3.3.3	I/O Interface.....	51
3.3.4	Inbox.....	52
3.3.5	Protocol Processor.....	55
3.4	The Software Queue.....	57
3.5	Programming MAGIC.....	59
Chapter 4	FLASH Protocol Implementations.....	60
4.1	FLASH Protocol Development Environment.....	60
4.1.1	FLASH Protocol Development Tool Chain.....	63
4.2	FLASH Bit-vector/Coarse-vector Implementation.....	65
4.2.1	Global Registers.....	67
4.2.2	Message Types.....	68
4.2.3	Jumtable Programming.....	70
4.2.4	Additional Considerations.....	71
4.3	FLASH Dynamic Pointer Allocation Protocol Implementation.....	73
4.3.1	Global Registers.....	76
4.3.2	Message Types.....	77
4.3.3	Jumtable Programming.....	78
4.3.4	Additional Considerations.....	78
4.4	FLASH SCI Implementation.....	80
4.4.1	FLASH SCI Cache States.....	82
4.4.2	Differences Between FLASH SCI and IEEE Specification.....	83
4.4.3	Global Registers.....	88

4.4.4	Message Types.....	88
4.4.5	Jumtable Programming.....	90
4.4.6	Additional Considerations.....	90
4.5	FLASH COMA Implementation.....	93
4.5.1	Global Registers.....	96
4.5.2	Message Types.....	96
4.5.3	Jumtable Programming.....	96
4.5.4	Additional Considerations.....	98
4.6	Protocol Summary.....	99
Chapter 5	Simulation Methodology.....	101
5.1	Applications.....	101
5.2	The FLASH Simulator.....	103
5.2.1	Processor Model.....	104
5.2.2	FlashLite.....	104
5.3	Synchronization.....	109
Chapter 6	Results.....	111
6.1	Key Questions Revisited.....	111
6.2	DSM Latencies.....	112
6.3	Direct Protocol Overhead.....	114
6.4	Message Overhead.....	118
6.5	Application Performance.....	119
6.5.1	FFT.....	120
6.5.2	Ocean.....	129
6.5.3	Radix-Sort.....	134
6.5.4	LU.....	137
6.5.5	Barnes-Hut.....	141
6.5.6	Water.....	142
6.6	Application Summary.....	143
Chapter 7	Conclusions, Related Work, and Beyond.....	146
7.1	Related Work.....	147
7.2	Future Work.....	151
Appendix A	Example Protocol Handlers.....	154
A.1	Bit-vector/Coarse-vector Handlers.....	154
A.2	Dynamic Pointer Allocation Handlers.....	159
A.3	SCI Handlers.....	162
A.4	COMA Handlers.....	165
Appendix B	Table of Results.....	170
References		175