WCED Program

8:00-8:30AM Breakfast
8:30-9:30AM Session I

- Printed Circuit Board Layout Time Estimation
  C. Bazeghi and J. Renau (University of California, Santa Cruz)

- Accommodating Workload Diversity in Chip Multiprocessors via Adaptive Core Fusion
  E. İpek, M. Kırman, N. Kırman, and J. Martínez (Cornell University)

- Designing Hardware that Supports Cycle-Accurate Deterministic Replay
  B. Greskamp, S.R. Sarangi, and J. Torrellas (University of Illinois)

9:30-9:45AM Short Break
9:45-10:45AM Session II

- Leveraging Bloom Filters for Smart Search Within NUCA Caches
  R. Ricci, S. Barrus, D. Gebhardt, and R. Balasubramonian (University of Utah)

- RegionTracker: Using Dual-Grain Tracking for Energy Efficient Cache Lookup
  J. Zebchuk and A. Moshovos (University of Toronto)

- Using Speculation Cost Predictability in Low-Power Cost-Aware Branch Prediction
  E. Atoofian, A. Baniasadi, and F. Khosrow-Khavar (University of Victoria)

10:45-11:15AM Break
11:15AM-12:30PM Panel Discussion

Title: An Agenda for Computer Architecture Research on Hardware Complexity
Moderator: Josep Torrellas, University of Illinois
Panelists:

- Dennis Abts, Cray
- Dan Leibholz, AMD
- Jose Renau, University of California, Santa Cruz
- John Shen, Intel