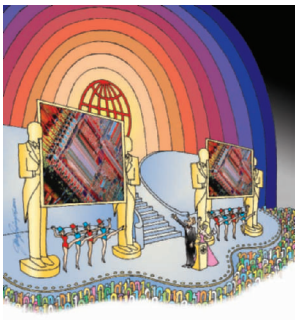
MICRO'S TOP PICKS FROM MICROARCHITECTURE CONFERENCES



David H. Albonesi
Cornell University

Each year, our colleagues in the computer architecture research community produce an impressive body of work in areas from tiny embedded devices to the highest performing multicore systems. Some of the very best of this work appears in the highly competitive, top computer architecture conferences, where acceptance rates between 15 and 25 percent have become the norm. Even with the "filtering" of the review process, a large amount of outstanding material finds its way into conference proceedings. For instance, 140 papers comprising roughly 1,500 pages appeared in five of the leading microarchitecture conferences in the past year. For the busy computing professional, mining this large amount of information for the subset of the papers that are of the most interest can be a daunting task, even with the advent of search engines.

Last year, *IEEE Micro* instituted a Top Picks issue, featuring a sampling of articles based on papers from the top architecture conferences. The idea was to showcase some of the very best, most industry-relevant, research efforts that had appeared in these forums in the past year. We continued the tradition this year, with a call for extended abstracts that argue for the relevance of the work to architects and designers of current and future-generation microprocessors or computing systems. We received a strong response of 44 abstract submissions.

Last year's overwhelming response to the call for papers called for two major changes this year to better formalize the selection process. First, we assembled a program committee consisting of industry architects, program chairs (or, when they were unavailable, program committee members) of the top architecture conferences (Micro-36, HPCA 10, ISCA 31, PACT 2004, and ASPLOS XI), and other well-known computer architects. We were fortunate to have these dedicated set of professionals to serve on this committee:

- Brad Calder, University of California, San Diego
- Krisztian Flautner, ARM
- Wen-mei Hwu, University of Illinois at Urbana-Champaign
- Norm Jouppi, Hewlett-Packard
- Josep-L. Larriba-Pey, UPC
- Ruby Lee, Princeton University
- Margaret Martonosi, Princeton University
- Chuck Moore, AMD
- Jaime Moreno, IBM
- Shubu Mukerjee, Intel
- Yale Patt, University of Texas at Austin
- Kevin Rudd, Intel
- Balaram Sinharoy, IBM
- Per Stenstrom, Chalmers University
- Marc Tremblay, Sun Microsystems
- Mateo Valero, UPC

The second change to the review process was the use of the online review system widely adopted by the top architecture conferences. We modified the review software to accommodate abstracts and full papers, and to account for the work's industry relevance. Reviewers—three from industry and three from academia for each paper—considered the work's technical strength compared to others that had appeared in top architecture conferences, and its industry rele-

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vance. We asked reviewers to weight these two factors equally. Following the review process, we held lengthy and, at times, contentious (but civil), online discussions to decide on the nine full-length and four short articles included in this year's issue. The entire process followed strict conflict-of-interest rules: Program committee members never even knew the rankings of submissions for which they had a conflict or for which they were coauthors.

As with last year, there were many excellent submissions, making it very difficult to choose the final selections. Page limits clearly forced us to leave out some very strong contributions, and the use of the industry relevance criteria made us pass up some novel work that the committee as a whole felt needed some time to mature before we could judge it to be "relevant." We plan to showcase some of this work in future *IEEE Micro* issues.

The articles in this year's Top Picks issue address many of the critical challenges facing industry architects with the relentless scaling of CMOS technology. Whereas five years ago, optimizing performance was the objective of the vast majority of microarchitecture papers, over half of the articles in this year's Top Picks issue primarily address other pressing concerns. The "2005 Micro Top Picks" sidebar lists a loosely categorized breakdown of this year's Top Picks articles.

Several University of Rochester students were instrumental in the success of the review process. Greg Briggs, as webmaster, made extensive and timely changes to the review software, while Nick Nelson, Ed Tan, Yongkang Zhu, Wael El-Essawy, and Ali El-Moursy retrieved the original papers and uploaded them to the site. The *IEEE Micro* staff, especially Janet Wilson and Kimberly Merritt, worked tirelessly from submission to final notification. Finally, the members of the program committee and Editor-in-Chief Pradip Bose were the most talented and devoted group of professionals that one could ever hope to work with.

Based on this year's experience, we have identified several changes to the Top Picks process for next year. We welcome your feedback on this year's issue and suggestions for next year.

2004 Micro Top Picks

Robust processor microarchitectures

- "Razor: Circuit-Level Correction of Timing Errors for Low-Power Operation"
- "Fingerprinting: Bounding Soft-Error-Detection Latency and Bandwidth"
- "Reducing the Soft-Error Rate of a High-Performance Microprocessor"

Energy efficient systems

- "Performance-Directed Energy Management for Storage Systems"

Microarchitectural support for software debugging and system performance analysis

- "iWatcher: Simple, General Architectural Support for Software Debugging"
- "Interaction Cost: For When Event Counts Just Don't Add Up"

Advanced processor microarchitectures

- "Continual Flow Pipelines: Achieving Resource-Efficient Latency Tolerance"
- "Helper Threads Via Virtual Multithreading"
- "The Vector-Thread Architecture"

Optimizing parallel microarchitectures

- "Transactional Coherence and Consistency: Simplifying Parallel Hardware and Software"
- "Speculative Incoherent Cache Protocols"

Scalable disambiguation of memory operations

- "Memory Ordering: A Value-Based Approach"
- "Scalable Hardware Memory Disambiguation for High-ILP Processors"

David H. Albonesi is an associate professor in the school of electrical and computer engineering at Cornell University. His research interests include microarchitecture with an emphasis on adaptive architectures, power-aware computing, and multithreading. Albonesi has a PhD from the University of Massachusetts at Amherst. He is a senior member of the IEEE, and a member of the IEEE Computer Society and the ACM.

Direct questions and comments about this special issue to David H. Albonesi, School of Electrical and Computer Engineering, Cornell University, 333 Rhodes Hall, Ithaca, NY 14853; albonesi@csl.cornell.edu.