WINDS 2010
Workshop on the Interaction between Nanophotonic Devices and Systems

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December 2010
Recent Nanophotonic Device-Level Work

Sherwood-Droz, OptExp'08

Orcutt, PS'09

Manipatruni, OptExp'10

Luxtera 2006

Intel 2010

IBM 2010
Recent Nanophotonic System-Level Work

Kirman, MICRO’06
Vantrease, ISCA’08
Shacham, TOC’08
Morris, JSTQE’10
Li, DAC’09
Gu, DATE’09
Cianchetti, ISCA’09
Batten, IEEE Micro’09
Joshi, NOCS’09
Koka, ISCA’10
Kurian, PACT’10
Pan, ISCA’09
Beamer, ISCA’10
Xue, ISCA’10

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Honeymoon Period of Nanophotonic System-Level Research

- Drove excitement in system-level community about this technology
- Illustrated potential benefit albeit with projected device parameters
- Less emphasis on practical issues required to really achieve these benefits
  - Transceiver circuits
  - Clocking
  - Off-chip laser design
  - Thermal tuning
  - Manufacturing
  - Reliability
Possible Post-Honeymoon Research Trajectories?

Communities Diverge
Maintaining Relevance Gap

Disruptive Device Breakthrough
Solves All Challenges

Stop Large-Scale System Research

Meet in the Middle
Goal for WINDS 2010

To begin to move beyond the honeymoon period by bringing together device-level and system-level nanophotonic researchers to talk about their work and to share their experiences with this emerging technology.
Workshop Agenda: Morning Sessions

9:00 – 10:00 am: Invited Tutorials

- Microphotonics for Next Generation Computers
  Michael Watts (MIT)
- Designing Nanophotonic Interconnection Networks
  Christopher Batten (Cornell)

10:30 – 12:00 am: Invited Talks

- Future State-of-the-Art Electrical Interconnect
  Byungsub Kim (Intel)
- Scaling and Designing Nanomodulators for Chip-Level Integration
  Sasikanth Manipatruni (GE Global Research)
- Keynote: The Oracle Macrochip: Architecture and Devices
  Frankie Liu and Michael O. McCracken (Oracle, Sun Labs)
Workshop Agenda: Afternoon Sessions

1:30 – 2:50 pm: Early Afternoon Session

- **EOS: A Monolithic CMOS Photonic Platform**
  V. Stojanović et al. (MIT)

- **Scalable Nanophotonic Interconnect for Cache-Coherent Multicores**
  R.W. Morris and A.K. Kodi (Ohio University)

- **Device Guidelines for WDM Interconnects Using Silicon Microrings**
  N. Sherwood-Droz, K. Preston, J.S. Levy, and M. Lipson (Cornell)

- **System-Level Trimming Issues in On-Chip Nanophotonic Networks**
  C. Nitta, M. Farrens, and V. Akella (U.C. Davis)
3:30 – 4:50 pm : Late Afternoon Session

- *Initial Results of Prototyping a 3D Integrated Intra-Chip Free-Space Optical Interconnect*  
  B. Ciftcioglu et al. (University of Rochester)

- *Towards Chip-Scale Plasmonic Interconnects*  
  H.M.G. Wassel et al. (UCSB/Stanford)

- *Exploring Benefits and Designs of Optically Connected Disintegrated Processor Architecture*  
  Y. Pan, Y. Demir, N. Hardavellas, J. Kim, and G. Memik (Northwestern/KAIST)

- *Implementing System-in-Package with Nanophotonic Interconnect*  
  M. Cianchetti, N. Sherwood-Droz, and C. Batten (Cornell)
Workshop Committee

Program Committee Chairs

- David Albonesi (Cornell University)
- José Martínez (Cornell University)

Program Committee

- Nathan Binkert (HP Labs)
- Luca Carloni (Columbia University)
- Ajay Joshi (Boston University)
- Nevin Kırman (Intel Labs)
- Herb Schwetman (Oracle, Sun Labs)