Exploring Benefits and Designs of Optically Connected Disintegrated Processor Architecture

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Transistor density grows exponentially
But, processors are physically constrained
  – Low yield, bandwidth wall, power wall
  – *Dark silicon*: we can build dense devices we cannot afford to power

Optically-Connected Disintegrated Processor (OCDP)
  – Divide (impractical) monolithic processor into chiplets
  – Improves yield
  – Breaks the bandwidth wall
  – **Breaks the power wall**
    • Spread out chiplets, cheaper cooling
Motivation

- Advantage of nanophotonics
  - Latency
  - Bandwidth density
- Using nanophotonics for inter-chip interconnect
  - Reduced memory latency
  - Increased off-chip bandwidth
  - Increased total chip area
  - Increased power budget
- Analytical model* for performance estimation

Memory Latency

Motivation
- OCDP Architecture
- Power Comparison
- Conclusion

![Graph showing memory latency and speedup](motivation.jpg)

- Speedup vs. Memory Latency (ns)
- Baseline

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WINDS 2010 (in conj. With MICRO 43)
Off-chip Bandwidth

Motivation
- OCDP Architecture
- Power Comparison
- Conclusion

![Graph of Off-chip Bandwidth vs Speedup]

- Baseline
- Off-chip Bandwidth (GB/s)
- Speedup
Scaling Power, Chip Area

- Motivation
  - OCDP Architecture
  - Power Comparison
  - Conclusion

![Graph showing the relationship between speedup and total die area for different power budgets and off-chip bandwidths.](image)
Motivation

- Performance impact
  - Reduced memory latency → minimal
  - Improved off-chip bandwidth → small
  - Total chip area → small
  - Power budget → big

- Power budget scalability is critical
  - Spread out chiplets
  - Cheaper cooling

- Optically-Connected Disintegrated Processor (OCDP)
## Off-chip Optical Channels

<table>
<thead>
<tr>
<th>Material</th>
<th>Optical Loss</th>
<th>Propagation Speed</th>
<th>Pitch (density)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Waveguide</td>
<td>0.3 dB/cm*</td>
<td>0.286c</td>
<td>20um</td>
</tr>
<tr>
<td>Optic Fiber</td>
<td>0.2 dB/km</td>
<td>0.676c</td>
<td>250um</td>
</tr>
</tbody>
</table>

- Optical fiber is low-loss, high speed
  - Enables further spreading out chiplets
  - *BW density was a challenge*

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* J. Cardenas et al., Optics Express 2009
Dense Off-chip Coupling

- Dense optical fiber array [Lee et al., OSA/OFC/NFOEC 2010]
- <1dB loss, 8 Tbps/mm demonstrated
OCDP Design Considerations

- Inter-chiplet optical channel technology
  - Optic fiber for low loss

- Inter-chiplet optical channel organization
  - Point-to-point [Koka et al., ISCA 2010]
  - Minimize waveguide and coupler loss

- On-chip topology
  - Scalable chiplet size

- On-chip / off-chip bandwidth interfacing
  - Distributed BW, seamless integration
OCDP Architecture

- Motivation
- OCDP Arch.
- Power Comparison
- Conclusion

Cross-chiplet assemblies share an optical bus, forming optical crossbars (FlexiShare)
Firefly on-chip topology [Pan et al., ISCA 2009]
- Flexible chiplet sizing, optical on-chip communication

FlexiShare optical crossbars [Pan et al., HPCA 2010]
- Flexible bandwidth provisioning
- Light-weight optical arbitration needed, proposed
Extending across chiplets

- Distributed bandwidth across chiplets
- Flexible inter-chiplet bandwidth provisioning
- Minimal number of couplers
- Seamless on-chip/off-chip interfacing

Chiplet 1

Chiplet 0

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## Technology Assumptions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Loss</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupler</td>
<td>1 dB</td>
<td>Detector Sensitivity</td>
<td>0.01 mW</td>
</tr>
<tr>
<td>Splitters</td>
<td>1 dB</td>
<td>DWDM</td>
<td>16 λ</td>
</tr>
<tr>
<td>Non-linear</td>
<td>1 dB</td>
<td>fiber coupler loss</td>
<td>0.1</td>
</tr>
<tr>
<td>Modulator Insertion</td>
<td>0.1 dB</td>
<td>fiber loss</td>
<td>2.00E-06 dB/cm</td>
</tr>
<tr>
<td>Waveguide</td>
<td>0.3 dB/cm</td>
<td>ring heating power</td>
<td>40 uW/ring</td>
</tr>
<tr>
<td>Ring Through</td>
<td>0.001 dB</td>
<td>Modulation Power</td>
<td>80 fJ/bit</td>
</tr>
<tr>
<td>Filter Drop</td>
<td>1.5 dB</td>
<td>Demodulation Power</td>
<td>40 fJ/bit</td>
</tr>
<tr>
<td>PhotoDetector</td>
<td>0.1 dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Moderate DWDM (16-way)
Optical Power (320-core)

- Motivation
- OCDP Architecture
- Power Eval.
- Conclusion

- 5-chiplet OCDP vs. single-chip topologies
- Total number of optical channels (wavelengths) held constant.

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~ 30% power reduction compared to the best alternative.
Scaling Up

- Motivation
- OCDP Architecture
- Power Eval.
- Conclusion

Total Optical Loss (dB)

- OCDP limits the total on-chip waveguide length
- Better optical scalability

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- OCDP shows very good power scalability.
- Single-chip is impractical for 1280-core processor
Conclusion

- OCDP leverages
  - Low latency / high bandwidth density
  - Low loss optic fibers
- Power scalability is critical
  - Minimize optical loss on the path
- Seamless on-chip / off-chip interfacing
  - Firefly intra-chiplet (distributed off-chiplet BW)
  - Point-to-point (Dragonfly) inter-chiplet
- Performance evaluation needed
- Chiplet composition to be explored
Questions?

THANK YOU!
On-chip Optical Channel

» Silicon photonics with DWDM