Future State-of-the-Art Electrical Interconnect

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Many-core processor era



Tilera 64 core processor

 \rightarrow 1000 cores in the future ?



Global interconnects for latency



- Increasing number of cores \rightarrow latency issue.
- Global NoC interconnects are attractive.



Nanophotonic on-chip interconnect



- Batten et. al., Micro2009
 Large bandwidth with small energy cost per bit over long distance
- Extra cost
 - CMOS compatible fabrication, extra area, energy overhead.
- We are keep improving ...

The winning interconnects?



- Nanophotonics v.s. electrical repeater
- Compare bandwidth and power consumption.



The winning interconnects?



Outline

- □ Fair comparison metrics.
- Trade-off of repeated interconnects.
- Trade-off of equalized interconnects.
- Status of equalized electrical interconnects based on silicon measurement.



Fair interconnect metrics?

- For a given target distance
- Data rate density = (Data rate)/ (cross-sectional width)
- Energy per bit
- Latency



In general, we cannot normalize these metrics by length.



Trade-off: repeated interconnects



Repeater trade-off: three dimensional surface.

Wires and circuits are jointly optimized.

Trade off: repeated interconnects



- Same energy per bit: same capacitance
- Larger data rate density : Tsb < Tsa</p>
- Larger latency : Tdb > Tda

Trade-off: repeated interconnects



Repeater trade-off: three dimensional surface.

Wires and circuits are jointly optimized.

Equalized Interconnects



Potentially lower power and higher data rate than repeaters.



Evolution of equalized interconnects



Review: equalization in frequency domain



Review: equalization in time domain



Trade-off: equalized interconnect



- Rx can sense small voltage ~ 100mV.
- Tx swing is adjusted for target eye size (constant).
- Tx swing is proportional to attenuation.
- By rule of thumb, energy per bit cost $\mu e^{l\sqrt{2pfRC}}$

Review: power consumption of equalization



Power overhead required

- New topologies greatly reduced power overhead.
 - Eg.) Kim ISSCC2009, Mensink ISSCC2007, …



Trade off: equalized interconnect



Equalized and unequalized pulses corresponding for

- For a given data rate density tareget, latency is fixed.
- The channel determines equalized Tx and Rx waveforms and the proper sampling time T_d (latency).

Trade-off: equalized interconnects



 Trade-off curve of equalized interconnect is 3dimensional line.



The winning interconnect



- Depends on application requirements.
- In general,
 - Rpt. wins in short distance (<5mm) or long distance applications (>10mm).
 - Eq. wins in medium distance (5mm-10mm).

Current status: equalized interconnects



- 2-3Gb/s/um with 400fJ/b-600fJ/b over 10mm in 90nm CMOS ASIC technology.
- We can expect further improvement in 22nm high-performance processor technology.



Conclusion

- To set the right direction of nanophotonics, we must compare them to the winning electrical interconnects, either repeated or equalized.
- Fair comparison metrics
 - data rate density, energy per bit, and latency.
- A repeated interconnect trade off is a 3-dimensional surface.
 - latency $\leftarrow \rightarrow$ data rate density
- Equalized interconnects provide better energy efficiency for the same performance in many situations than repeated ones.
- There is no absolute winner.
 - In general, an equalized interconnect is better for 5-10mm distance.

