Scaling and Designing Nanomodulators for Chip-Level Integration

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WINDS 2010 Invited Talk
Workshop on the Interaction between Nanophotonic Devices and Systems
Sunday, December 5th, 2010 • Atlanta, Georgia

In this talk, I will discuss nanomodulators with special emphasis on chip-level integration. Three key issues viz. energy/bit, areal and linear bandwidth density, and robustness will be addressed. Device-level ideas with novel control techniques to enable wide temperature range, direct digital logic driven modulators operating at sub 10 fJ/bit energy and $>$10 Tbit/mm^2 will be presented. I will then derive the fundamental scaling limits for the nanophotonic interconnects based on electro-optic device operation. I will show the scaling of total energy per bit, optical cross-over distance, bandwidth density and tuning power. These device figures of merit can be applied to any generic interconnect irrespective of the detailed physical working mechanism.

Sasikanth Manipatruni is at the General Electric (GE) Global Research Center working in nanophotonic interconnects for massively parallel magnetic resonance and ultrasound imaging. He obtained his Ph.D. working with Prof. Michal Lipson at Cornell university. He graduated from Indian Institute of Technology (IIT) Delhi at the top of his class in EE. He was a KVPY national science fellow of the Indian Institute of Sciences and worked at Swiss Federal Institute of Technology, Zurich. He has 10 patent applications in nanophotonics and MR, 40 peer reviewed journal and conference papers. He serves as a peer reviewer for OSA, IEEE and Nature. His business plan for fab-less photonics was awarded the first place at Asia Moot Corp and selected as an outstanding product at World Moot Corp.