## WARP 2015 6th Workshop on Architectural Research Prototyping

Co-Located with the 42nd International Symposium on Computer Architecture Sunday, June 14th, 2015 • Portland, Oregon http://www.csl.cornell.edu/warp2015

## Workshop Organizers

Christopher Batten Cornell University

David Wentzlaff Princeton University

## Program Committee

David Brooks Harvard University

Steve Keckler NVIDIA, UT Austin

Mark Oskin *Univ. of Washington* 

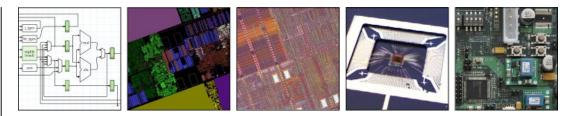
Jose Renau *UC Santa Cruz* 

## **Important Dates**

Submission Deadline *April 10, 2015* 

Notification of Selection *April* 27, 2015

Final Abstract Submission May 22, 2015



Building prototype systems can be one of the best ways to validate assumptions, gain intuition about practical design issues, and provide platforms for future software research. While the research ideas behind these prototypes can be published in top-tier conferences, there are not many venues suitable for focusing on the actual prototype itself. At the same time, building an FPGA, ASIC, or full-custom computer architecture prototype is a non-trivial endeavor and requires a significant financial and time commitment. This workshop is intended as a forum for the builders in our community to share their practical on-the-ground experiences, to provide a status update on their progress, and to convey insights for those considering prototyping their ideas.

This half-day workshop will be held on Sunday, June 14th, 2015, co-located with ISCA-42 in Portland, OR. The workshop will primarily include presentations selected by the technical program committee based on extended abstract submissions.

We invite submissions on all aspects of building prototype systems for computer architecture research. Submissions can discuss new or pending prototypes that have not been published in any other venue, or submissions can discuss the practical prototyping implications of previously published work. Submissions more in the spirit of a short position paper are also encouraged. Topics of particular interest include, but are not limited to:

- Status updates on FPGA, ASIC, or full-custom prototypes for computer architecture research that have been recently constructed or are currently under construction
- Implementation technology trade-offs (FPGAs, ASICs, vs full-custom)
- Practical guidance on what works and what doesn't, including strategies for:
  - High-level specification
  - Register-transfer-level implementation
  - Pre- and post-construction verification
  - Packaging and board design
  - Managing complex electronic design automation toolflows
- Practical advice on managing the increasing design complexity inherent in building computer architecture research prototypes that integrate general-purpose processors and memory systems with specialized accelerators
- How to balance the often conflicting goals of prototypes as research vehicles containing novel architectural mechanisms vs. prototypes as high-performance software development platforms
- How to balance student's thesis goals vs. engineering work
- How to secure funding for building prototypes

See workshop webpage for submission details.