ECE 5745 Complex Digital ASIC Design, Spring 2017

Course Syllabus

School of Electrical and Computer Engineering
Cornell University

revision: 2017-01-26-00-34

1. Course Information

**Prereqs**

ECE 4750 Computer Architecture

**Instructor**

Prof. Christopher Batten, 323 Rhodes Hall, cbatten@cornell.edu
Office Hours: 323 Rhodes Hall, Wednesday, 4:30–5:30pm

**Admin. Assistant**

Daniel Richter, 314 Rhodes Hall, tdr27@cornell.edu

**Lectures**

403 Phillips Hall, Tuesday and Thursday, 2:55–4:10pm (until spring break)

**Section**

407 Phillips Hall, Friday, 2:30–3:20pm (until spring break)

**Required**

Neil H. E. Weste & David M. Harris

“CMOS VLSI Design: A Circuits and Systems Perspective”
4th edition, Addison Wesley, 2010
Available at Cornell bookstore ($183), Amazon ($152),
or on reserve in Uris Library

**Website**

http://www.csl.cornell.edu/courses/ece5745

2. Description

This course aims to provide a strong foundation for students to understand the principle and practice of designing, implementing, testing, and evaluating complex standard-cell ASIC chips using automated state-of-the-art computer-aided design (CAD) tools. This course is at the intersection of computer architecture, digital circuits, and CAD and is suitable for students pursuing careers in both research and industry. For students pursuing research topics in computer architecture, the course will provide deeper insight into critical physical design issues for future computing systems, while for students pursuing research topics in digital circuits, the course will provide system-level insight into future large-scale chip designs. For students pursuing a career in the chip-design industry, the course will provide valuable design experience from architecture to digital circuits.

The course is divided into four parts: the first three parts are lecture-based, while the final part is an extensive design project. The first part provides an overview of ASIC design including: hardware description languages; CMOS devices; CMOS circuits; full-custom design methodology; automated design methodologies; testing and verification; packaging and I/O. The second part provides a deeper study of CMOS digital-circuit fundamentals including combinational logic, sequential state, and interconnect. The third part provides a deeper study of CAD algorithms including synthesis algorithms and physical design automation algorithms. The final part is an open-ended design project where small groups of students design, implement, test, and evaluate an interesting technique in computer architecture using functional-, microarchitectural-, register-transfer-, and layout-level modeling. This five-week long design experience will include weekly
project meetings with the course instructors, milestone documents, a project demonstration, and a
detailed final report.

3. Objectives

The field of computer systems can be visualized as a stack of abstraction and implementation layers
with application requirements at the top and technology constraints at the bottom. The intermediate
layers include devices, circuits, gate-level design, register-transfer-level (RTL) design, microar-
chitecture, instruction set architecture, compilers, operating systems, programming languages, and
algorithms. Computer engineering is usually focused in the middle of this stack spanning circuits
to operating systems.

Currently, the ECE curriculum provides numerous courses at the RTL, microarchitecture, and archi-
tecture layers including ECE 4750 Computer Architecture, ECE 5730 Memory Systems, ECE 5770
Resilient Computing, and ECE 5750 Advanced Computer Architecture. ECE 4750 is probably the
lowest-level of these courses: students learn the fundamentals of designing processors, memories,
and networks, and apply this knowledge through a series of lab assignments. Students gradually
design, implement, test, and evaluate a simple multicore system capable of running parallel micro-
benchmarks at the register-transfer level. The lab assignments focus on cycle-level performance
(i.e., the impact a technique has on the number of cycles it takes to execute a program). Although
ECE 4750 teaches students some basic principles involved in evaluating the cycle time, energy, and
area impact of various design decisions, they do not have an opportunity to put this into practice. In
addition, the focus of ECE 4750 is firmly on general-purpose subsystems as opposed to application-
specific subsystems. At the opposite end of the computer engineering spectrum is ECE 4740 Digital
VLSI Design, ECE 5710 Arithmetic Circuits, and ECE 5740 Advanced Digital VLSI. These courses
teach students the fundamentals of digital circuit design, but the scope of these courses is on small
custom-designed subsystems involving hundreds of transistors.

This course bridges the gap between computer architecture and digital circuits. Students will learn
how to take the RTL designs from ECE 4750 and use automated tools to generate realistic layout.
The course will enable students to quantitatively evaluate the cycle time, energy, and area impact of
the techniques they learned in ECE 4750. ECE 4750 and this course dovetail nicely together creating
a year-long digital design experience for students. By the end of this course, students should be
able to:

• **describe** concepts related to the overall ASIC design methodology, CMOS digital circuits, and
  CAD algorithms and explain how these concepts interact.

• **apply** this understanding to new ASIC design problems within the context of balancing
  application requirements against technology constraints; more specifically, quantitatively
  assess a design’s execution time in cycles, cycle time, area, and energy.

• **evaluate** various design alternatives and make a compelling quantitative and/or qualitative
  argument for why one design is superior to the other approaches.

• **demonstrate** the ability to implement and verify designs of varying complexity at the
  register-transfer level and to push these designs through a commercial ASIC CAD toolflow.

• **create** new baseline and alternative designs at the register-transfer level, the associated
  effective testing strategies, and a thorough evaluation plan.
write comprehensive technical reports that describe designs implemented at the register-transfer level, explain the testing strategy used to verify functionality, and evaluate the designs to determine the superior approach.

4. Prerequisites

This course is targeted towards advanced senior undergraduates, M.Eng. students, and first-year Ph.D. students. ECE 4750 is a prerequisite for all undergraduates and M.Eng. students. Students are more likely to be successful in this class if they did well in ECE 4750. Since ECE 4750 is a prerequisite, students are expected to be very proficient with Linux and the command line, implementing designs using well-structured synthesizable register-transfer-level models, writing test harnesses, and evaluating designs using simulators. Students are expected to be familiar with all of the ECE 4750 lab assignments.

We will be using a new hardware modeling framework that is based on a combination of Python and Verilog. Students which have never used Python before may want to spend additional time reviewing the textbook titled “Think Python: How to Think Like a Computer Scientist” by A. B. Downey (Green Tea Press, 2014). Those students with less experience working with the Verilog hardware description language are strongly encouraged to read Chapter 4 in “Digital Design and Computer Architecture, 2nd edition” by D. M. Harris and S. L. Harris (Morgan Kaufmann, 2012), and/or to review “Verilog HDL: A Guide to Digital Design and Synthesis, 2nd edition” by S. Palnitkar (Prentice Hall, 2003).

Note that we will cover enough circuits and CAD in this course such that advanced circuit-level or CAD courses are not prerequisites. However, those students that have taken such courses will be able to see how digital circuits are composed into much larger multi-million transistor designs, and how CAD algorithms can be used in practice.

5. Required Materials

The required textbook for the course is Neil H. E. Weste and David M. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective, 4th edition,” Addison Wesley, 2011. Please use the 4th edition, since there have been significant changes compared to earlier editions. This book is available at the Cornell bookstore and is on reserve in Uris Library. There will be occasional assigned readings from the book, but more importantly this is an excellent book that all serious digital ASIC designers should have on their bookshelf.

6. Format and Procedures

This course includes a combination of lectures, optional discussion sections, a problem set, laboratory assignments, a midterm, and a five-week design project. The design project includes a preproposal, proposal, weekly meetings, milestone documents, demonstration, and final report. Students are expected to work with a partner on the lab assignments and the design project. Assessment rubrics for the lab assignments and design project will be distributed early in the semester.

- Lectures – Lectures will be from 2:55pm to 4:10pm every Tuesday and Thursday until spring break. There will be no lectures after spring break. Lectures will take place in 403 Phillips Hall. We will start promptly at 2:55pm so please arrive on time. Students are expected to attend all lectures, be attentive during lecture, and participate in class discussion. Please turn
of all cellular phones during class. Use of cellular phones and laptops during lecture is not 
allowed (see Section 9.C).

- **Discussion Section** – There will be a discussion section most Fridays before spring break 
from 2:30pm to 3:30pm in 407 Phillips Hall. Attendance at the weekly discussion sections are 
onoptional but strongly encouraged. These discussion sections will be relatively informal, with 
the primary focus being on facilitating student’s ability to complete the lab assignments and 
prepare for the design project. There may be some problem-based learning activities during 
these discussion sections.

- **Problem Set** – The course will include one (significant) problem set to enable students to 
apply concepts learned during lecture into practice. The problem set is meant to be completed 
individually, although students are encouraged to study together and discuss information 
and concepts covered in lecture with other students (see Section 9.F for collaboration policy). 
The problem set must be submitted in PDF format via the online CMS assignment submission 
system (see Section 10). You can use any program you want to compose your solutions, but 
you must convert the final document to PDF. Students are strongly encouraged to type their 
solutions; if students absolutely must write up their answers by hand, then they must scan 
their final version into a legible PDF. Illegible scans will not be graded. No other means of 
submission or electronic format will be accepted.

- **Lab Assignments** – The course will include two lab assignments that allow students to begin 
quantitatively evaluating area, cycle time, cycle counts, and energy consumption for various 
design alternatives. Students must work with a partner (see Section 9.F for collaboration pol-
icy). Students will be using the ECE Computing Resources to complete the lab assignments, 
the lab code must be submitted via GitHub, and the lab report must be submitted in PDF 
format via the online CMS assignment submission system (see Section 10). No other means 
of submission or electronic format will be accepted.

- **Midterm** – The course includes an evening midterm that covers all of the lecture material 
extcept for the final lecture which is on the same day as the midterm. If students have a 
scheduling conflict with the midterm, they must let the instructor know as soon as possible, 
but no later than two weeks before the midterm. Taking the midterm is a requirement for 
passing the course. Graded exams and the exam solutions are only available for review in 
310/314 Rhodes Hall under the supervision of a course instructor. You may not remove your 
graded exam, nor may you remove the exam solutions from 310/314 Rhodes Hall.

- **Design Project Preproposal/Proposal** – Students are required to submit both a project pre-
proposal and proposal as PDFs online via CMS (see Section 10). Students are strongly en-
couraged to discuss their project ideas with the instructors before the preproposal is due. The 
preproposal will be reviewed by the course instructors and feedback delivered to the students 
to factor into their proposal.

- **Design Project Meetings** – After spring break, each project group will meet with the course 
instructors once a week during the regularly scheduled course meeting times. Project meet-
ings will be held in the instructor’s office, 323 Rhodes Hall. Students are expected to show up 
on time and be prepared for the meeting. Students will be asked to demonstrate progress by 
remotely logging into the course computing resources and running unit tests or small exper-
iments on their design.

- **Design Project Milestones** – There will be three project milestone documents due after spring 
break. Each milestone document must be submitted as a PDF online via CMS. Each project
milestone document focuses on a portion of the design project final report; so an initial draft of the final report can consist of simply assembling the project milestone documents into a coherent narrative.

• **Design Project Demonstration** – During the final week of classes, students will schedule time to meet with the instructors and demonstrate their design project. This demonstration is a key part of the project assessment. Students should prepare a step-by-step demonstration that illustrates the project’s code quality, functionality, and illustrates some of the results discussed as part of the project report.

• **Design Project Report** – The project report is due during the standard final exam time for this course. Students are not allowed to make significant changes to their code after the project demonstration. Instead, students should focus on writing a well-structured report which describes the motivation, related work, baseline design, design alternatives, testing strategy, and evaluation for their design project.

7. **Assignment and Exam Schedule**

The current schedule is on the course website. All assignments are due on Thursdays at 11:59pm, except for project milestone documents which are due on Fridays at 11:59pm (see Section 9.D for late assignment policy). All assignments should be submitted electronically via CMS, except for lab and project code which is submitted via GitHub. Project demonstrations will occur during the final week of classes. Changes to this schedule will be posted as announcements via Piazza.

<table>
<thead>
<tr>
<th>Thu</th>
<th>Feb 16</th>
<th>Lab 1 – ASIC Integer Multiplier</th>
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<tbody>
<tr>
<td>Thu</td>
<td>Mar 2</td>
<td>Preproposal Due</td>
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<td>Thu</td>
<td>Mar 9</td>
<td>Lab 2 – ASIC Sorting Accelerator</td>
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<tr>
<td>Thu</td>
<td>Mar 16</td>
<td>Proposal Due</td>
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<td>Thu</td>
<td>Mar 23</td>
<td>Problem Set Due</td>
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<tr>
<td>Thu</td>
<td>Mar 30</td>
<td>Midterm from 7:30–10:30pm in 203 Phillips Hall</td>
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<tr>
<td>Fri</td>
<td>Apr 21</td>
<td>Milestone 1 – Baseline Design and Testing Strategy Document</td>
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<td>Fri</td>
<td>Apr 28</td>
<td>Milestone 2 – Alternative Design Document</td>
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<td>Fri</td>
<td>May 5</td>
<td>Milestone 3 – Evaluation Document</td>
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<tr>
<td>Fri</td>
<td>May 12</td>
<td>Design Project Demonstrations</td>
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<tr>
<td>May</td>
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<td>Design Project Report due date/time is TBD</td>
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8. **Grading Scheme**

Each part or criteria of every assignment is graded on a four-point scale. A score of 4.25 is an A+, 4 roughly corresponds to an A, 3 roughly corresponds to a B, 2 roughly corresponds to a C, and so on. A score of 4.0 usually indicates that the submitted work demonstrates no misunderstanding (there may be small mistakes, but these mistakes do not indicate a misunderstanding) or there may be a very small misunderstanding that is vastly outweighed by the demonstrated understanding. A score of 3.0 usually indicates that the submitted work demonstrates more understanding than misunderstanding. A score of 2.0 usually indicates that the submitted work demonstrates a balanced amount of understanding vs. misunderstanding. A score of 1.0 usually indicates that the submitted work demonstrates more misunderstanding than understanding. A score of 4.25 is reserved for when the submitted work is perfect with absolutely no mistakes or is exceptional in some other way.
Total scores are a weighted average of the scores for each part or criteria. Parts or criteria are usually structured to assess a student’s understanding according to four kinds of knowledge: basic recall of previously seen concepts, applying concepts in new situations, qualitatively and quantitatively evaluating design alternatives, and creatively implementing new designs; these are ordered in increasing sophistication and thus increasing weight. In almost all cases, scores are awarded for demonstrating understanding and not for effort. Detailed rubrics for all quizzes, problem sets, and exams are provided once the assignment has been graded to enable students to easily see how the score was awarded. For lab assignments, a detailed Lab Assignment Assessment Rubric is available on the public course webpage.

The final grade is calculated using a weighted average of all assignments with the following distribution. Note that the design project as a whole is worth roughly half of the final grade. **If you are not willing to put a significant amount of work into this course after spring break, please do not take this course.**

<table>
<thead>
<tr>
<th>Assignment</th>
<th>Weight</th>
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<tbody>
<tr>
<td>Lab Assignment 1</td>
<td>5%</td>
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<tr>
<td>Lab Assignment 2</td>
<td>10%</td>
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<tr>
<td>Problem Set</td>
<td>10%</td>
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<tr>
<td>Midterm</td>
<td>30%</td>
</tr>
<tr>
<td>Design Project Milestone 1</td>
<td>5%</td>
</tr>
<tr>
<td>Design Project Milestone 2</td>
<td>5%</td>
</tr>
<tr>
<td>Design Project Milestone 3</td>
<td>5%</td>
</tr>
<tr>
<td>Design Project Demonstration</td>
<td>10%</td>
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<tr>
<td>Design Project Report</td>
<td>20%</td>
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Note that to pass the course, a student must at a bare minimum satisfy the following requirements: (1) submit the problem set; (2) submit at least one lab assignment; (3) take the midterm exam; and (4) submit the design project report. **If a student does not satisfy these criteria then that student will fail the course regardless of the student’s numerical grade.**

### 9. Policies

This section outlines various policies concerning usage of cellular phones and laptops in lecture, turning in assignments late, regrading assignments, collaboration, and accommodations for students with disabilities.

#### 9.A Auditor and Listener Policy

Casual listeners that attend lecture but do not enroll as auditors are not allowed; you must enroll officially as an auditor. Auditors are allowed to enroll in the course as long as there is sufficient capacity in the lecture room. Auditors must attend most of the lectures. If you do not plan on attending the lectures, then please do not audit the course. Please note that students are not allowed to audit the course and then take it for credit in a later year unless there is some kind of truly exceptional circumstance.

#### 9.B Course Re-Enrollment Policy

Students are not allowed to enroll for credit for a significant fraction of the course, drop or switch to auditor status, and then re-enroll for credit in a later year. It is not fair for students to have access
to assignment solutions and possibly even take the midterm before deciding to drop the course and take it again in a later year; this would essentially enable students to take the course twice to improve their grade.

9.C Cellular Phones and Laptops in Lecture Policy

Students are prohibited from using cellular phones and laptops in lecture unless they receive explicit permission from the instructor. It is not practical to take notes with a laptop for this course. Students will need to write on the handouts and quickly sketch diagrams during lecture. The distraction caused by a few students using (or misusing) laptops during lecture far outweighs any benefit. Tablets are allowed as long as they are kept flat and used exclusively for note taking. If you feel that you have a strong case for using a laptop during lecture then please speak with the instructor.

9.D Late Assignment Policy

All written documents must be submitted electronically in PDF format via CMS, and code must be submitted electronically via GitHub (as explained in the lab handout). No other formats will be accepted! All assignments must be submitted by 11:59pm on the due date. No extensions will be granted except for a family or medical emergency. We will be using CMS, an automated online assignment submission system. You can continue to resubmit your files as many times as you would like up until the deadline, so please feel free to upload early and often. If you submit an assignment even one minute past the deadline, the system will automatically mark it as late. There is no grace period. There are no slip-days for this course. You may submit your assignment up to two days late, but your score will be deducted one letter grade (i.e., a full point on the 4.25 scale) for each day the assignment is late.

9.E Regrade Policy

Addition errors in the total score are always applicable for regrades. Regrades concerning the actual solution should be rare and are only permitted when there is a significant error. Please only make regrade requests when the case is strong and a significant number of points are at stake. Regrade requests should be submitted online via a private post on Piazza within one week of when an assignment is returned to the student. You must provide a justification for the regrade request.

9.F Collaboration Policy

The work you submit in this course is expected to be the result of your individual effort only, or in the case of lab assignments and the design project, the result of you and your partner’s effort only. Your work should accurately demonstrate your understanding of the material. The use of a computer in no way modifies the standards of academic integrity expected under the University Code.

You are encouraged to study together and to discuss information and concepts covered in lecture with other students. You can give “consulting” help to or receive “consulting” help from other students. Students can also freely discuss basic computing skills or the course infrastructure. However, this permissible cooperation should never involve one student (or lab group) having possession of or observing in detail a copy of all or part of work done by someone else, in the form of an email, an email attachment file, a flash drive, a hard copy, or on a computer screen. Students are not allowed to seek consulting help from online forums outside of Cornell University.
Students are not allowed to use online solutions (e.g., from Course Hero) from previous offerings of this course. Students are encouraged to seek consulting help from their peers and from the course staff via office hours and the online Piazza discussion forums. **If a student receives consulting help from anyone outside of the course staff, then the student must acknowledge this help on the submitted assignment.**

During examinations, you must do your own work. Talking or discussion is not permitted during the examinations, nor may you compare papers, copy from others, or collaborate in any way. Students must not discuss an exam’s contents with other students who have not taken the exam. If prior to taking it, you are inadvertently exposed to material in an exam (by whatever means) you must immediately inform an instructor.

Should a violation of the code of academic integrity occur, then a primary hearing will be held. See [http://www.theuniversityfaculty.cornell.edu/AcadInteg](http://www.theuniversityfaculty.cornell.edu/AcadInteg) for more information about academic integrity proceedings.

Examples of acceptable collaboration:

- Bob is struggling on a problem set about processor pipelining, so he seeks consulting help from Alice, a fellow student in the course. Alice goes through various examples from the lecture and reading materials to help Bob understand the concepts, and they sketch a few pipeline diagrams related to the problem solution together on a whiteboard. Bob and Alice work independently to flesh out the details of the problem solution and they each write up their work independently. Bob acknowledges the help he received from Alice on his submission.

- Bob and Ben are struggling to complete a lab assignment which requires implementing a direct-mapped cache. They talk with Alice and Amy and learn that both groups are really struggling. So the four students get together for a brainstorming session. They review the lecture and reading materials and then sketch on a whiteboard some ideas on how to implement a direct-mapped cache. They might also sketch out some Verilog code snippets to try and understand the best way to describe some of the hardware. Then each group independently writes the code for the assignment and includes an acknowledgment of the help they received from the other group. At no time do the groups actually share code.

Examples of unacceptable collaboration:

- Bob is struggling on a problem set about processor pipelining, so he seeks consulting help from Alice, a fellow student in the course. Alice shows Bob her completed problem set solutions and walks him through the various steps required to solve the problem. Bob takes some notes during their discussion, and then independently writes up his solutions. Bob acknowledges the help he received from Alice on his submission, but it doesn’t matter since Alice explicitly shared her solutions with Bob.

- Bob and Ben are struggling to complete a lab assignment which requires implementing a direct-mapped cache. They talk with Alice and Amy and learn that both groups are really struggling. So the four groups get together for a joint coding session. Each student works on one module in the cache, then they combine the modules together to create the final working direct-mapped cache. The four students share and copy each others code often in order to finish the assignment. Each group submits the final code independently. Each group acknowledges the help it received from the other group, but it doesn’t matter since they explicitly shared code.

Notice that the key is that students should not share the actual solutions or code with each other. Consulting with your fellow students is fine and is an important part of succeeding in this course.
9.G Accommodations for Students with Disabilities

In compliance with the Cornell University policy and equal access laws, the instructor is available to discuss appropriate academic accommodations that may be required for students with disabilities. Requests for academic accommodations are to be made during the first three weeks of the semester, except for unusual circumstances, so arrangements can be made. Students are encouraged to register with Student Disability Services to verify their eligibility for appropriate accommodations.

10. Online and Computing Resources

We will be making use of a variety of online websites and computing resources.

- **Public Course Website** – [http://www.csl.cornell.edu/courses/ece5745](http://www.csl.cornell.edu/courses/ece5745)
  This is the main public course website which has the course details, updated schedule, lecture slide handouts, tutorials, and most handouts.

- **Piazza Discussion Forums** – [http://www.csl.cornell.edu/courses/ece5745/piazza](http://www.csl.cornell.edu/courses/ece5745/piazza)
  We will be using Piazza for all announcements and discussion on course content, lab assignments, and the projects. The course staff is notified whenever anyone posts on the forum and will respond quickly. Using the forum allows other students to contribute to the discussion and to see the answers. Use common sense when posting questions such that you do not reveal solutions. Please prefer posting to Piazza as opposed to directly emailing the course staff unless you need to discuss a personal issue.

- **CMS** – [http://www.csl.cornell.edu/courses/ece5745/cms](http://www.csl.cornell.edu/courses/ece5745/cms)
  We will be using the online CMS assignment submission system for managing all assignments including distributing grades. We will enroll students that sign up for the course in CMS. We will also be posting restricted materials (e.g., problem sets, quizzes, solutions) on the CMS site. We will not be using CMS to post announcements.

- **ECE Computing Resources** –
  The ECE department has a cluster of Linux-based workstations and servers which we will be using for the lab assignments. You can access the ECE computing resources by using the ECE Linux Computing Lab in 314 Phillips Hall, you can use the CIT Windows Computing Lab in 318 Phillips Hall, or you can log into the ecelinux servers remotely from your own personal workstation. You do not need a special account; you will instead simply use your NetID and Cornell password to log into the ECE computing resources.

- **GitHub** – [http://www.csl.cornell.edu/courses/ece5745/github](http://www.csl.cornell.edu/courses/ece5745/github)
  We will be using GitHub to distribute lab assignment harnesses and as a mechanism for student collaboration on the lab assignments and design project. Students are expected to become familiar with the git version control system and use it effectively for collaboration.

- **TravisCI** – [http://www.csl.cornell.edu/courses/ece5745/travisci](http://www.csl.cornell.edu/courses/ece5745/travisci)
  TravisCI is an online continuous integration service that is tightly coupled to GitHub. TravisCI will automatically run all tests for a students’ lab assignment every time the students push their code to GitHub. We will be using the results reported by TravisCI to evaluate the code functionality of the lab assignments.