Activity

Implement as inverting 2-input multiplexer.

Assume that S and \( \overline{S} \) are available.

\[ f = (S \cdot D_1) + (\overline{S} \cdot \overline{D_0}) \]

\[ PD = (S \cdot D_1) + (\overline{S} \cdot \overline{D_0}) \]

\[ PU = (S \cdot D_1) + (\overline{S} \cdot D_0) \]

\[ = (S \cdot D_1) \cdot (\overline{S} \cdot \overline{D_0}) \]

\[ = (S + D_1) \cdot (\overline{S} + \overline{D_0}) \]
ECE 5745

**SLIDE 21**

**Equivalence of Static CMOS + Tri-state MUX Implementation**

- Pull down network is the same for both implementations. Key difference is in pull up network.

- Let’s first write the equation for the pull up network in the static CMOS implementation and then transform it into the equation for the pull up in the tri-state impl.

### Static CMOS Pullup

\[ PU = \overline{S} \cdot \overline{D_0} \cdot \overline{D_1} \cdot \overline{D_0} \cdot \overline{D_1} \]

\[ = (S + D_0) \cdot (\overline{S} + D_1) \]

\[ = S \cdot (\overline{S} + D_1) + D_0 \cdot (S + D_1) \]

\[ = S \cdot \overline{S} + S \cdot D_1 + D_0 \cdot S + D_0 \cdot D_1 \]

\[ = S \cdot \overline{D_1} + D_0 \cdot \overline{S} + D_0 \cdot \overline{D_1} \]

- Resembling, if \( D_0 \) or \( D_1 \) are one and

\[ \text{the \text{ non-linear term \ not \ impact \ result.} \]

- If some are one then both of the first term cannot be zero.

### Tristate Pullup

\[ PU = (D_0 \cdot \overline{S}) + (D_1 \cdot S) \]

\[ = \overline{S} \cdot \overline{D_0} \cdot \overline{D_1} \cdot \overline{D_0} \cdot \overline{D_1} \]

\[ = (S + D_0) \cdot (\overline{S} + D_1) \]

\[ = S \cdot (\overline{S} + D_1) + D_0 \cdot (S + D_1) \]

\[ = S \cdot \overline{S} + S \cdot D_1 + D_0 \cdot S + D_0 \cdot D_1 \]

\[ = S \cdot \overline{D_1} + D_0 \cdot \overline{S} + D_0 \cdot \overline{D_1} \]

- Same as pullup network for tristate implementation.
ACTIVITY

Implement $F = ABC$ (3 input AND gate) using
pass transistor logic.

Pass transistors can only "pass" if only one of $A, B, C$ or
their complement or a constant $VDD$. Don't use
pass transistors to "pass" a constant $VDD$.

Ensure that output is always driven to $\Phi$ or
$VDD$ and is never floating.

Start with 2 input AND gate

$$A \quad B \quad F = AB$$

But if $B = 0$, output is floating

$$A \quad B \quad \overline{B} \quad F = AB$$

Now output is always driven
high or low

3 input AND gate

$$A \quad B \quad C \quad F = ABC$$