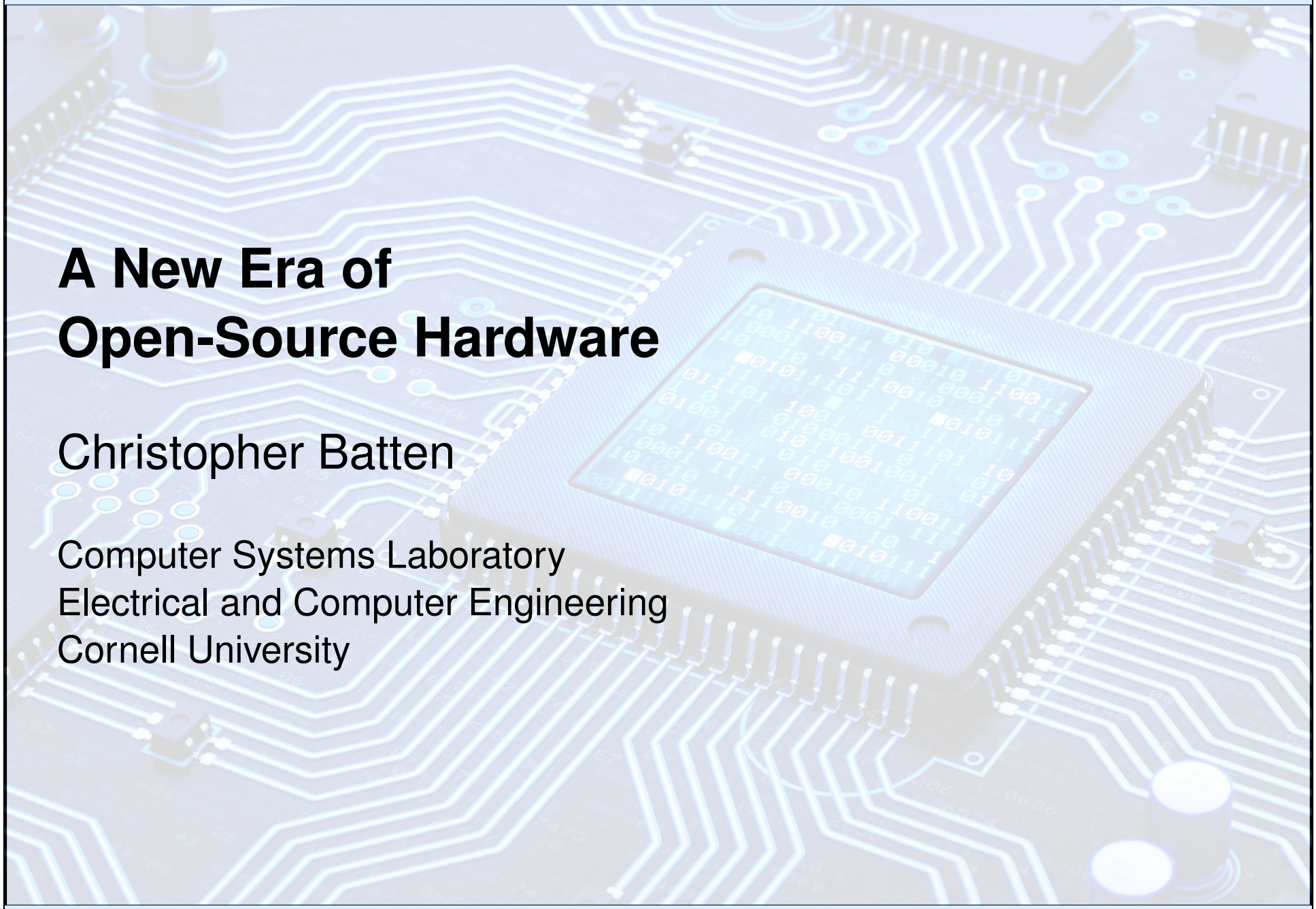
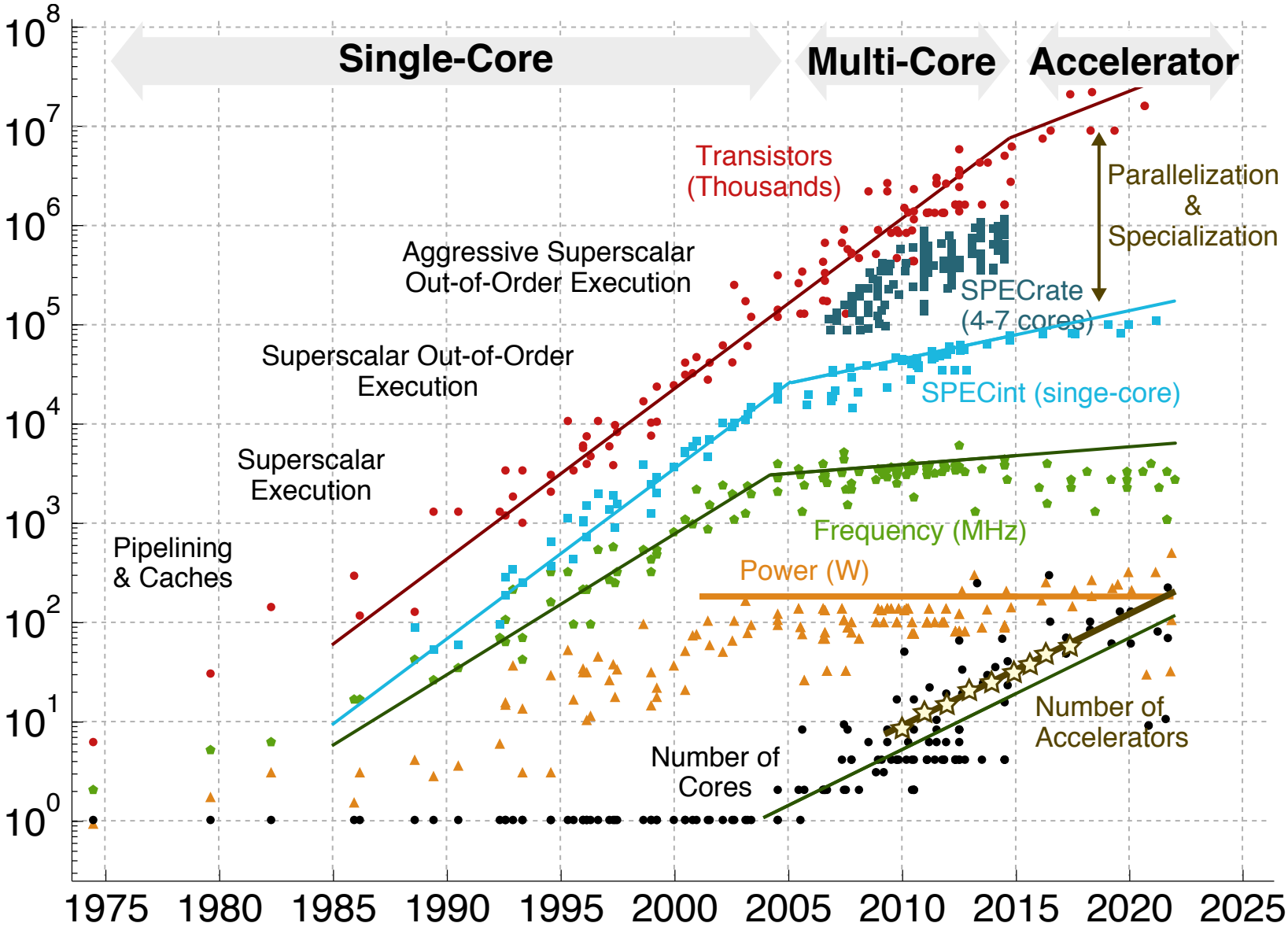


A New Era of Open-Source Hardware

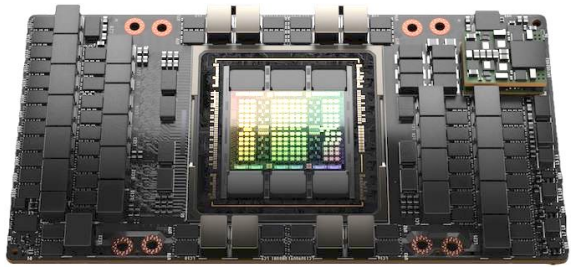
Christopher Batten

Computer Systems Laboratory
Electrical and Computer Engineering
Cornell University



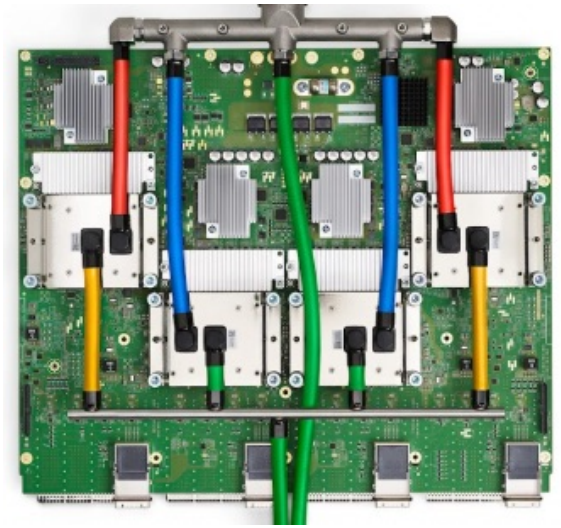
C. Batten, M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, K. Rupp & [Y. Shao, IEEE Micro'15] & [C. Leiserson, Science'20]

Accelerators for Machine Learning in the Cloud



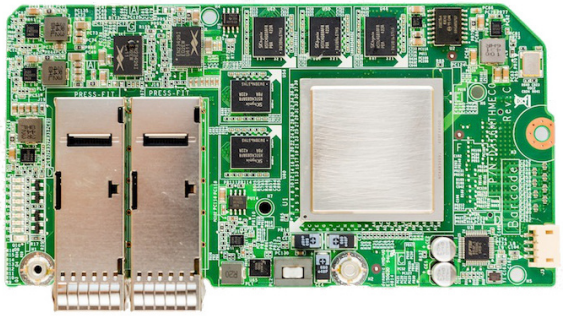
NVIDIA DGX Hopper

- Graphics processor specialized just for accelerating machine learning
- Available as part of a complete system with both the software and hardware designed by NVIDIA



Google TPU v4

- Custom chip specifically designed to accelerate Google's TensorFlow C++ library
- Tightly integrated into Google's data centers



Microsoft Catapult

- Custom FPGA board for accelerating Bing search and machine learning
- Accelerators developed with/by app developers
- Tightly integrated into Microsoft data center's and cloud computing platforms

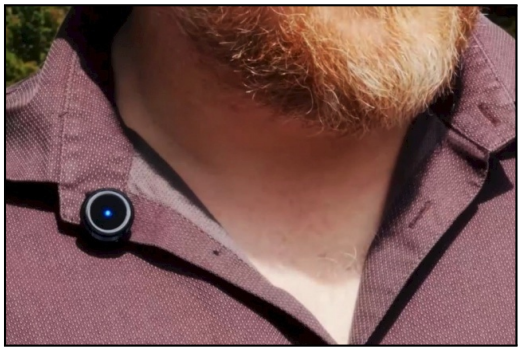
Accelerators for Machine Learning at the Edge

Amazon Echo

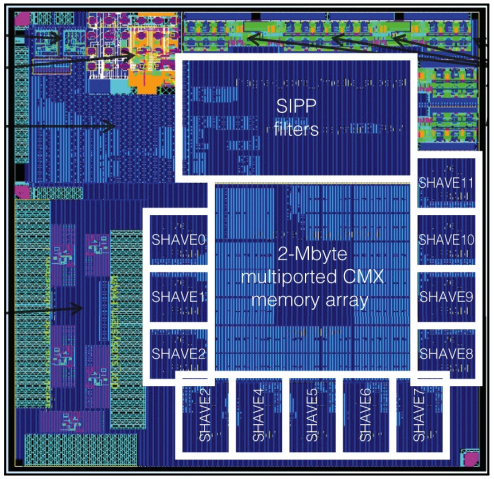
- Developing AI chips so Echo line can do more on-board processing
- Reduces need for round-trip to cloud
- Co-design the algorithms and the underlying hardware

Facebook Oculus

- Starting to design custom chips for Oculus VR headsets
- Significant performance demands under strict power requirements



Movidius Myriad 2



Top-five software companies are all building custom accelerators

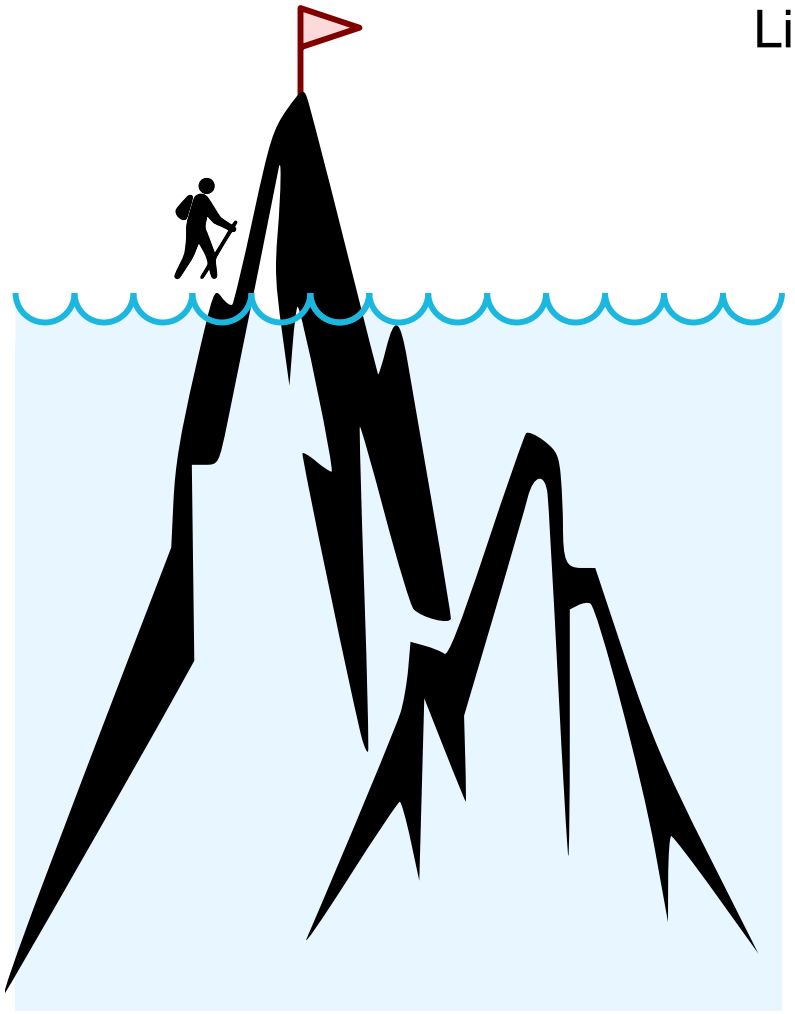
- **Facebook:** w/ Intel, in-house AI chips
- **Amazon:** Echo, Oculus, networking chips
- **Microsoft:** Hiring for AI chips
- **Google:** TPU, Pixel, convergence
- **Apple:** SoCs for phones and laptops

Chip startup ecosystem for machine learning accelerators is thriving!

How can we accelerate innovation in accelerator-centric hardware design?

- **Graphcore**
- **Nervana**
- **Cerebras**
- **Wave Computing**
- **Horizon Robotics**
- **Cambricon**
- **DeePhi**
- **Esperanto**
- **SambaNova**
- **Eyeriss**
- **Tenstorrent**
- **Mythic**
- **ThinkForce**
- **Groq**
- **Lightmatter**

Software Innovation Today



Like climbing an iceberg – much is hidden!

Your proprietary code

- Instagram
- $500K seed with 13 people → $1B

Open-source software

- Python
- Django
- Memcached
- Postgres/SQL
- Redis
- nginx
- Apache, Gnuicorn
- Linux
- GCC

"What Powers Instagram: Hundreds of Instances, Dozens of Technologies" https://goo.gl/76fWrM

Adapted from M. Taylor, “Open Source HW in 2030,” Arch 2030 Workshop @ ISCA’16

Hardware Innovation Today

Like climbing a mountain – nothing is hidden!

What you have to build

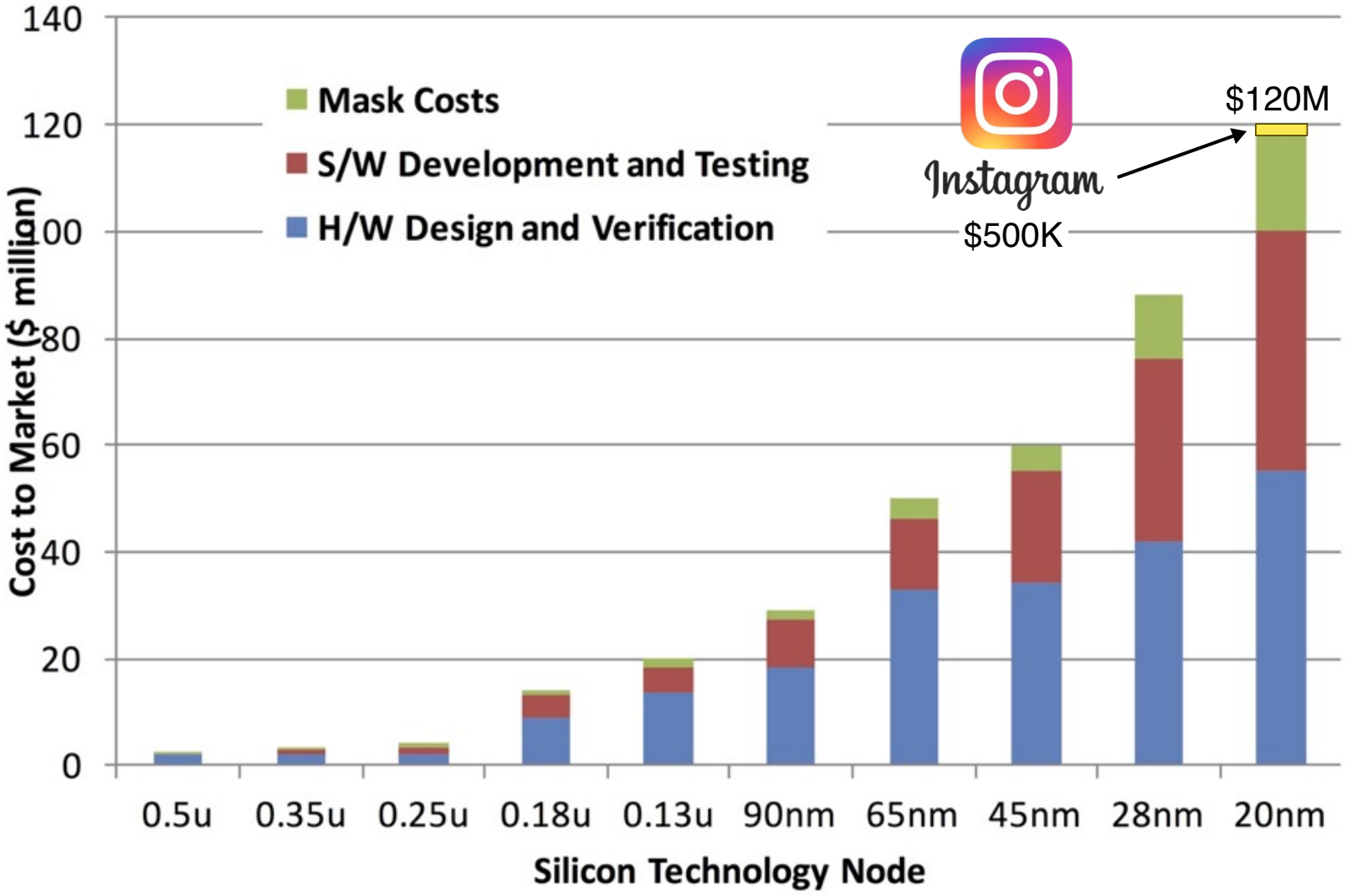
- New machine learning accelerator
- Other unrelated components, anything you cannot afford to buy or for which COTS IP does not do

Closed source

- ARM A57, A7, M4, M0
- ARM on-chip interconnect
- Standard cells, I/O pads, DDR Phy
- SRAM memory compilers
- VCS, Modelsim
- DC, ICC, Formality, Primetime
- Stratus, Innovus, Voltus
- Calibre DRC/RCX/LVS, SPICE

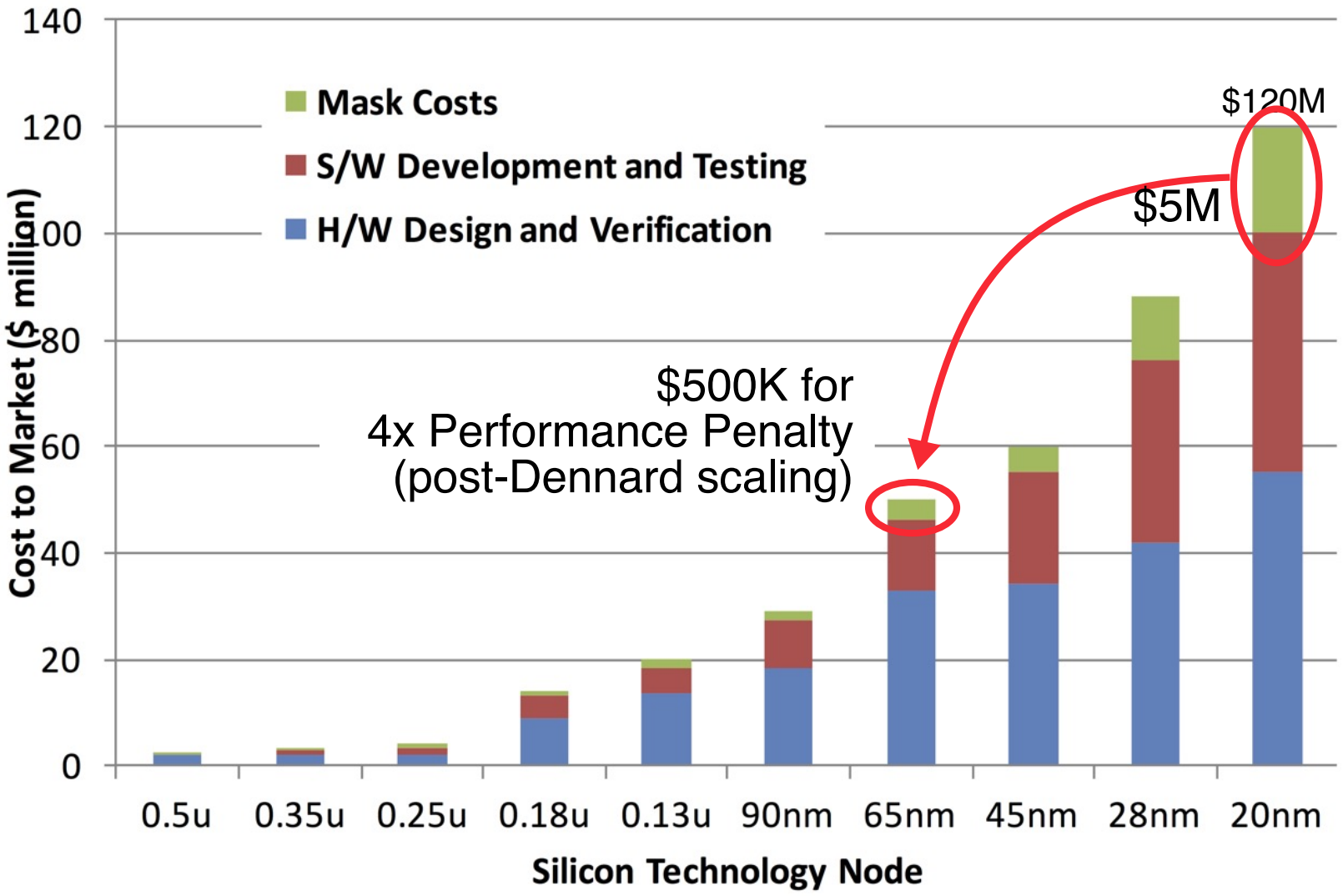
Adapted from M. Taylor, "Open Source HW in 2030," Arch 2030 Workshop @ ISCA'16

Chip Costs Are Skyrocketing



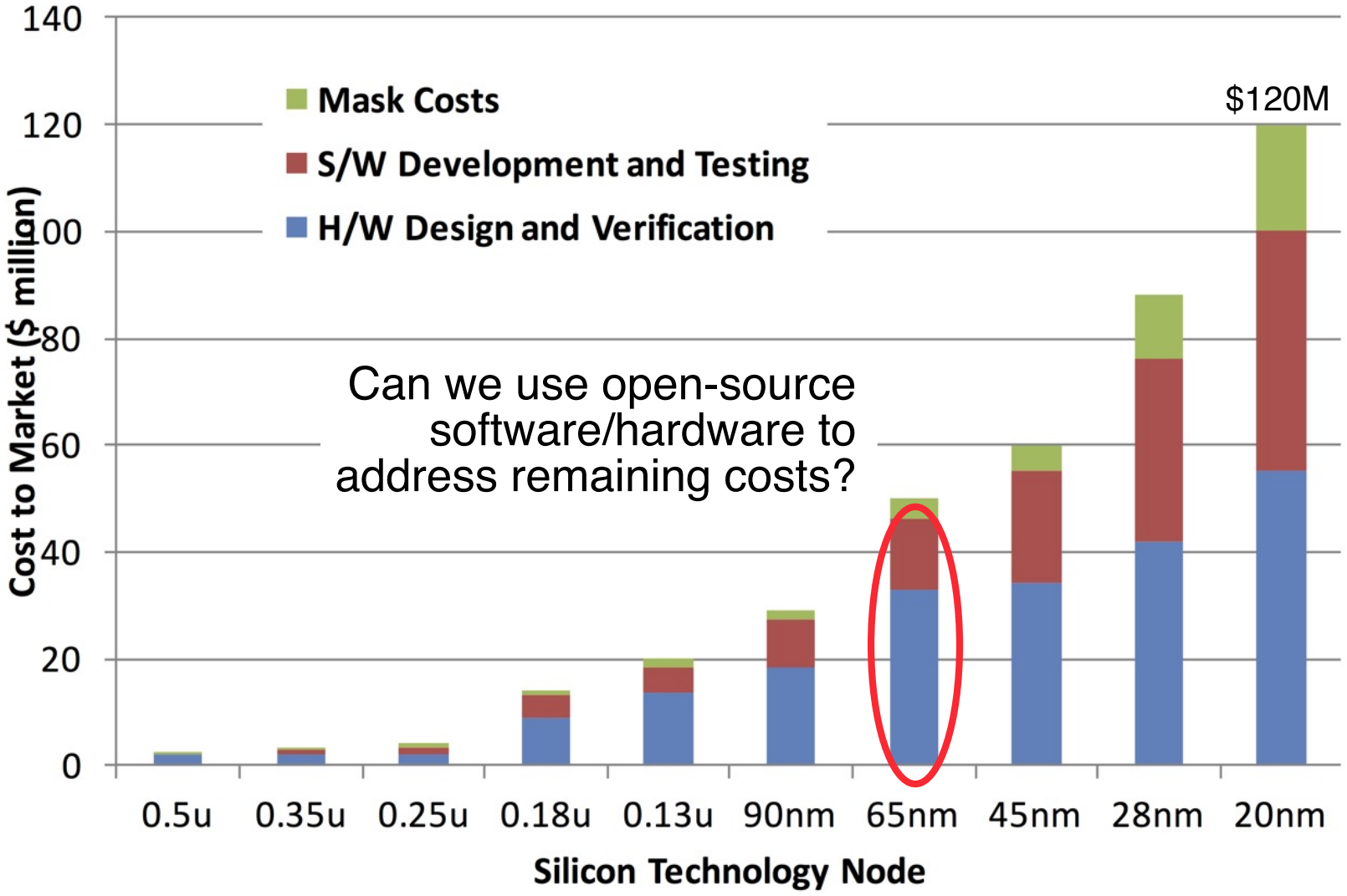
Adapted from M. Taylor, "Open Source HW in 2030," Arch 2030 Workshop @ ISCA'16; original: International Business Strategies & T. Austin.

Minimum Viable Product/Prototype



Adapted from M. Taylor, "Open Source HW in 2030," Arch 2030 Workshop @ ISCA'16; original: International Business Strategies & T. Austin.

Minimum Viable Product/Prototype



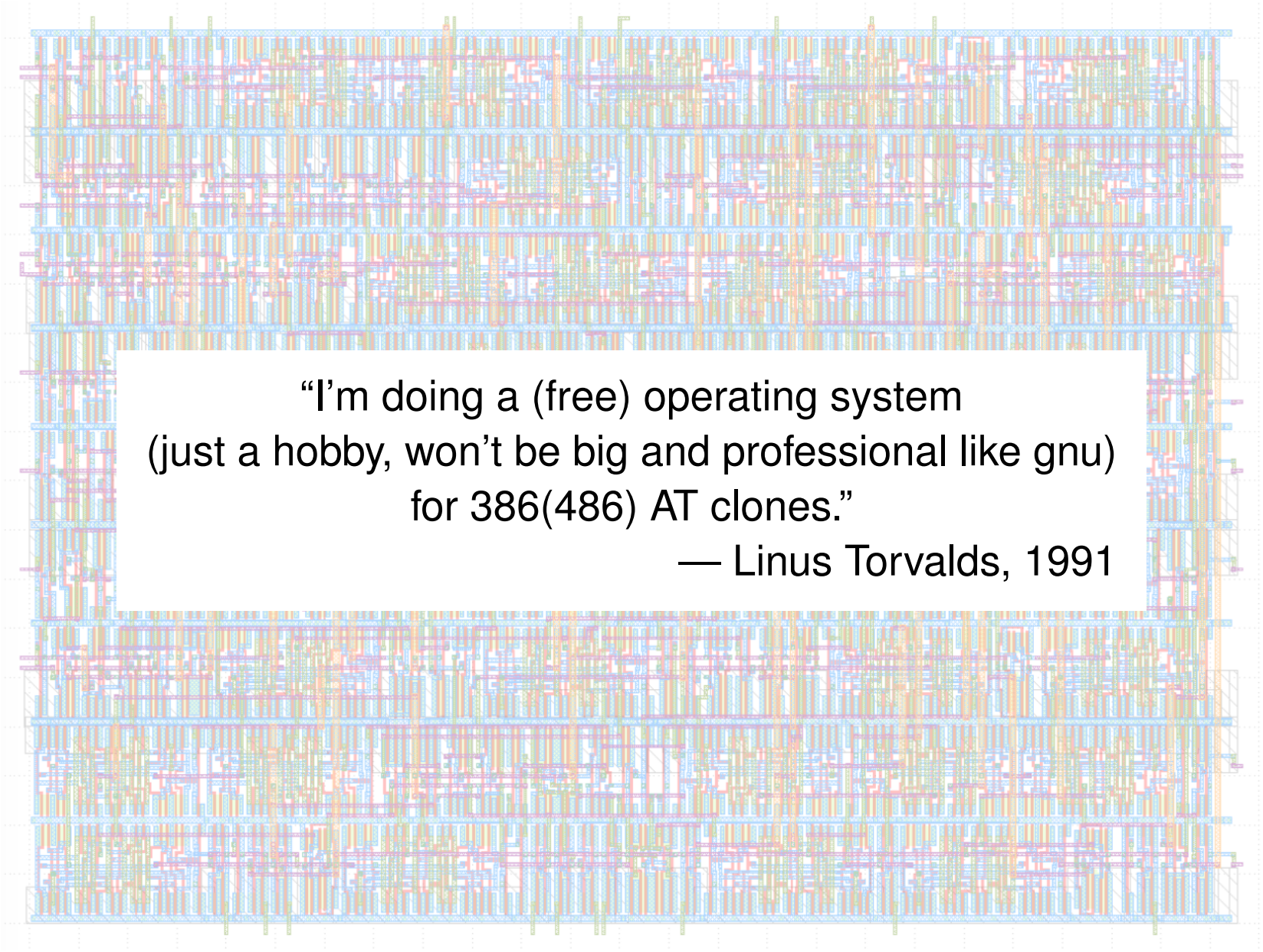
Adapted from M. Taylor, "Open Source HW in 2030," Arch 2030 Workshop @ ISCA'16; original: International Business Strategies & T. Austin.

How can HW design be more like SW design?

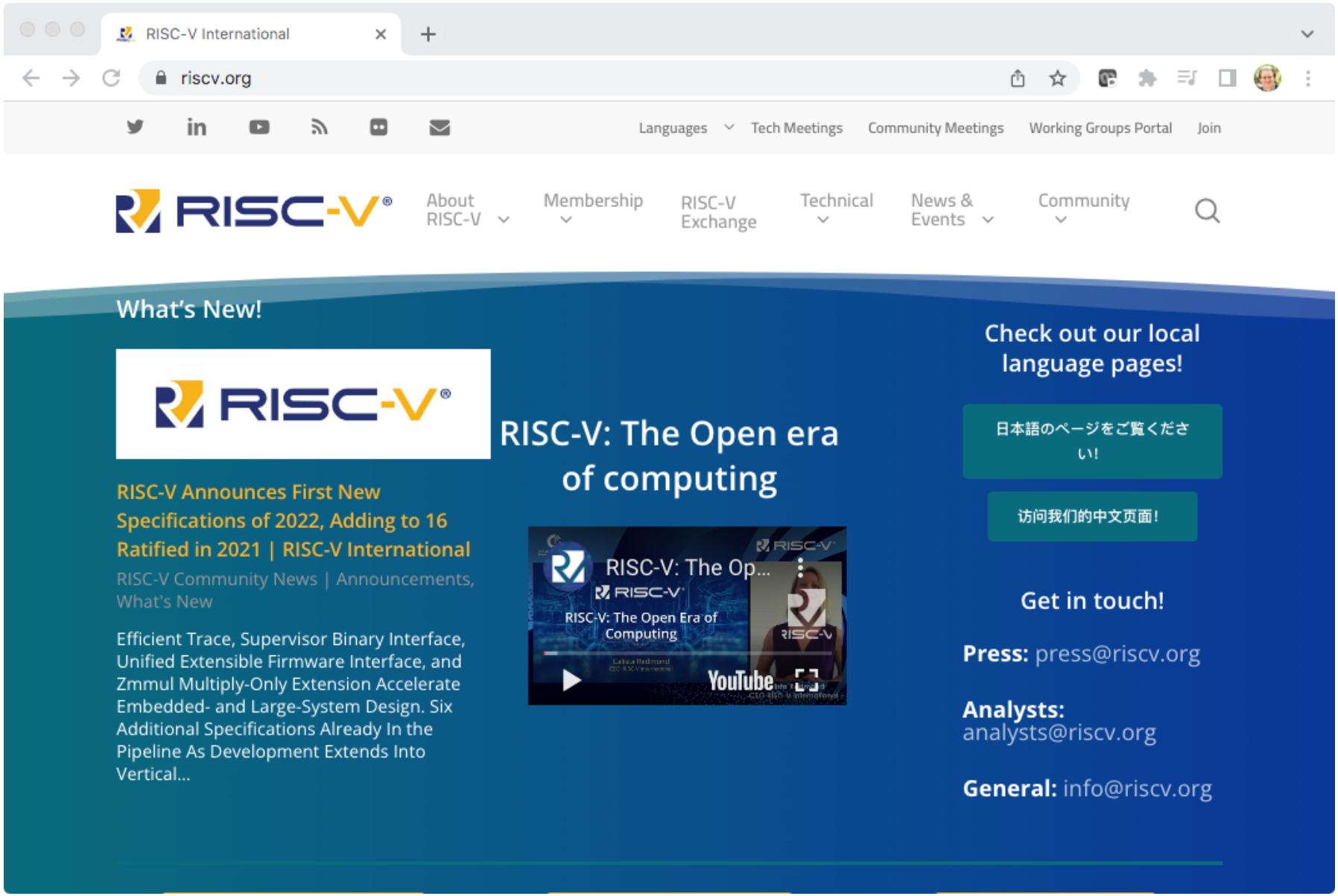
Open-Source	Software	Hardware
high-level languages	Python, Ruby, R, Javascript, Julia	Chisel, PyMTL, PyRTL, MyHDL, JHDL, Cλash, Calyx
libraries	C++ STL, Python std libs	BaseJump
systems	Linux, Apache, MySQL, memcached	Rocket, Pulp/Ariane, OpenPiton, Boom, FabScalar, MIAOW, Nyuzi
standards	POSIX	RISC-V ISA, RoCC, TileLink
tools	GCC, LLVM, CPython, MRI, PyPy, V8	Icarus Verilog, Verilator, qflow, Yosys, TimberWolf, qrouter, magic, klayout, ngspice
methodologies	agile software design	agile hardware design
cloud	IaaS, elastic computing	IaaS, elastic CAD

c. 2018

```
# Ubuntu Server 16.04 LTS (ami-43a15f3e)
% sudo apt-get update
% sudo apt-get -y install build-essential qflow
% mkdir qflow && cd qflow
% wget http://opencircuitdesign.com/qflow/example/map9v3.v
% qflow synthesize place route map9v3 # yosys, graywolf, qrouter
% wget http://opencircuitdesign.com/qflow/example/osu035_stdcells.gds2
% magic                  # design def/lef -> magic format
>>> lef read /usr/share/qflow/tech/osu035/osu035_stdcells.lef
>>> def read map9v3.def
>>> writeall force map9v3
% magic                  # stdcell gds -> magic format
>>> gds read osu035_stdcells.gds2
>>> writeall force
% magic map9v3
>>> gds write map9v3    # design + stdcells magic format -> gds
% sudo apt-get -y install libqt4-dev-bin libqt4-dev libz-dev
% wget http://www.klayout.org/downloads/source/klayout-0.24.9.tar.gz
% tar -xzvf klayout-0.24.9.tar.gz && cd klayout-0.24.9
% ./build.sh -noruby -nopython
% wget http://www.csl.cornell.edu/~cbatten/scmos.lyp
% ./bin.linux-64-gcc-release/klayout -l scmos.lyp ../map9v3.gds
```



"I'm doing a (free) operating system
(just a hobby, won't be big and professional like gnu)
for 386(486) AT clones."
— Linus Torvalds, 1991


RISC-V International
riscv.org
Languages
Tech Meetings
Community Meetings
Working Groups Portal
Join
RISC-V
About RISC-V
Membership
RISC-V Exchange
Technical
News & Events
Community
What's New!
RISC-V Announces First New Specifications of 2022, Adding to 16 Ratified in 2021 | RISC-V International
RISC-V Community News | Announcements, What's New
Efficient Trace, Supervisor Binary Interface, Unified Extensible Firmware Interface, and Zmmul Multiply-Only Extension Accelerate Embedded- and Large-System Design. Six Additional Specifications Already In the Pipeline As Development Extends Into Vertical...
RISC-V: The Open era of computing
RISC-V: The Op...
RISC-V: The Open Era of Computing
YouTube
Check out our local language pages!
日本語のページをご覧ください!
访问我们的中文页面!
Get in touch!
Press: press@riscv.org
Analysts: analysts@riscv.org
General: info@riscv.org

Industry Interest in RISC-V is Growing

RISC-V Hardware *and* Software Ecosystem

Software

Open-source software:
Gcc, binutils, glibc, Linux, BSD, LLVM, QEMU, FreeRTOS, ZephyrOS, LiteOS, SylixOS, …

Commercial software:
Lauterbach, Segger, IAR, Micrium, ExpressLogic, Ashling, AntMicro, Imperas, UltraSoC …

RISC-V Foundation

ISA specification | Golden Model | Compliance

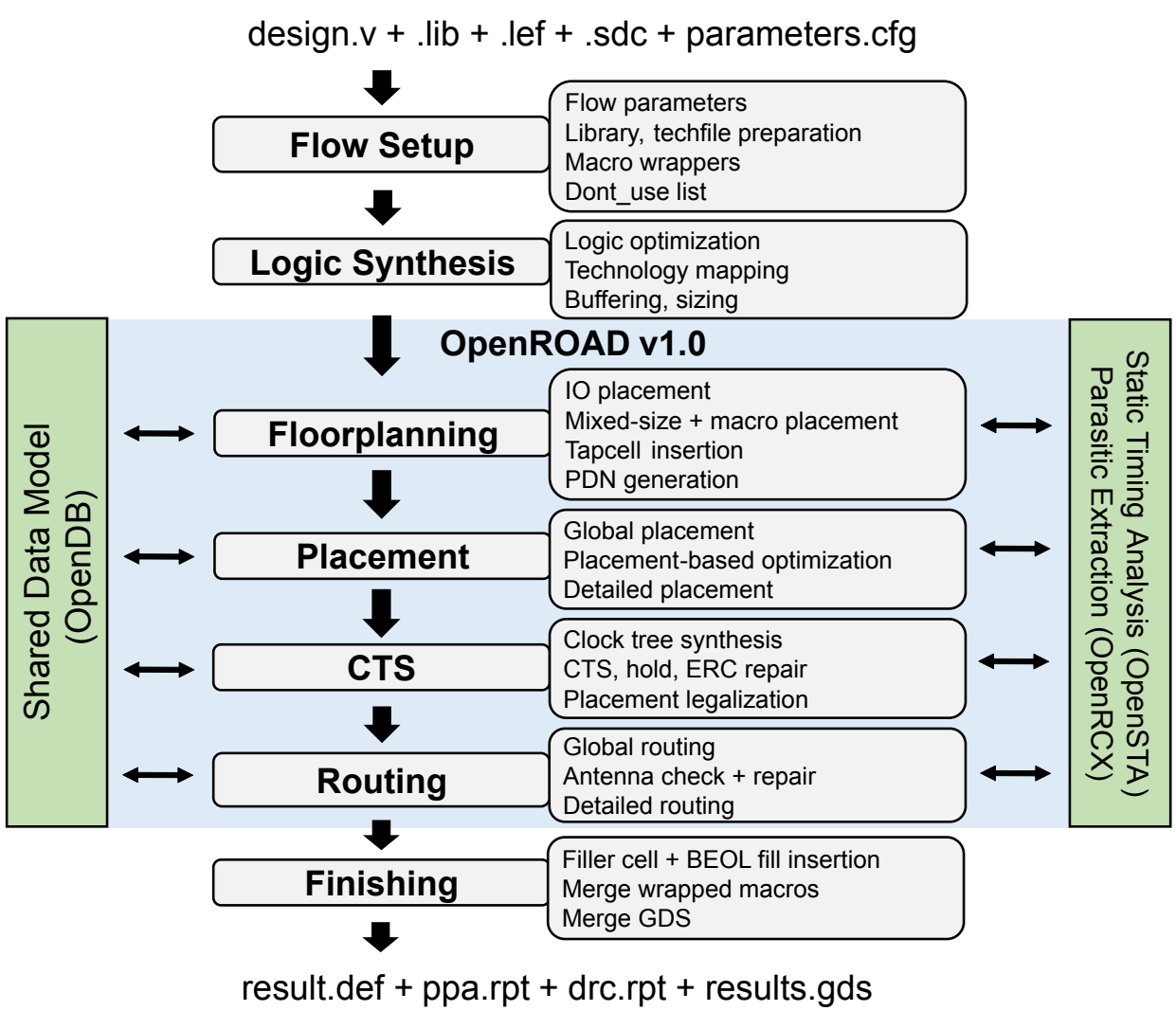
Hardware

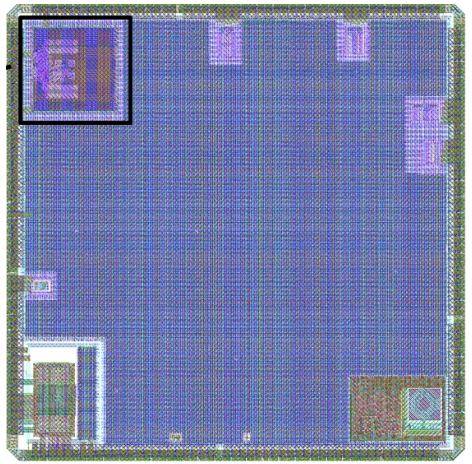
Open-source cores:
Rocket, BOOM, RI5CY, Ariane, PicoRV32, Piccolo, SCR1, Shakti, Swerv, Hummingbird, …

Commercial core providers:
Andes, Bluespec, Cloudbear, Codasip, Cortus, C-Sky, InCore, Nuclei, SiFive, Syntacore, …

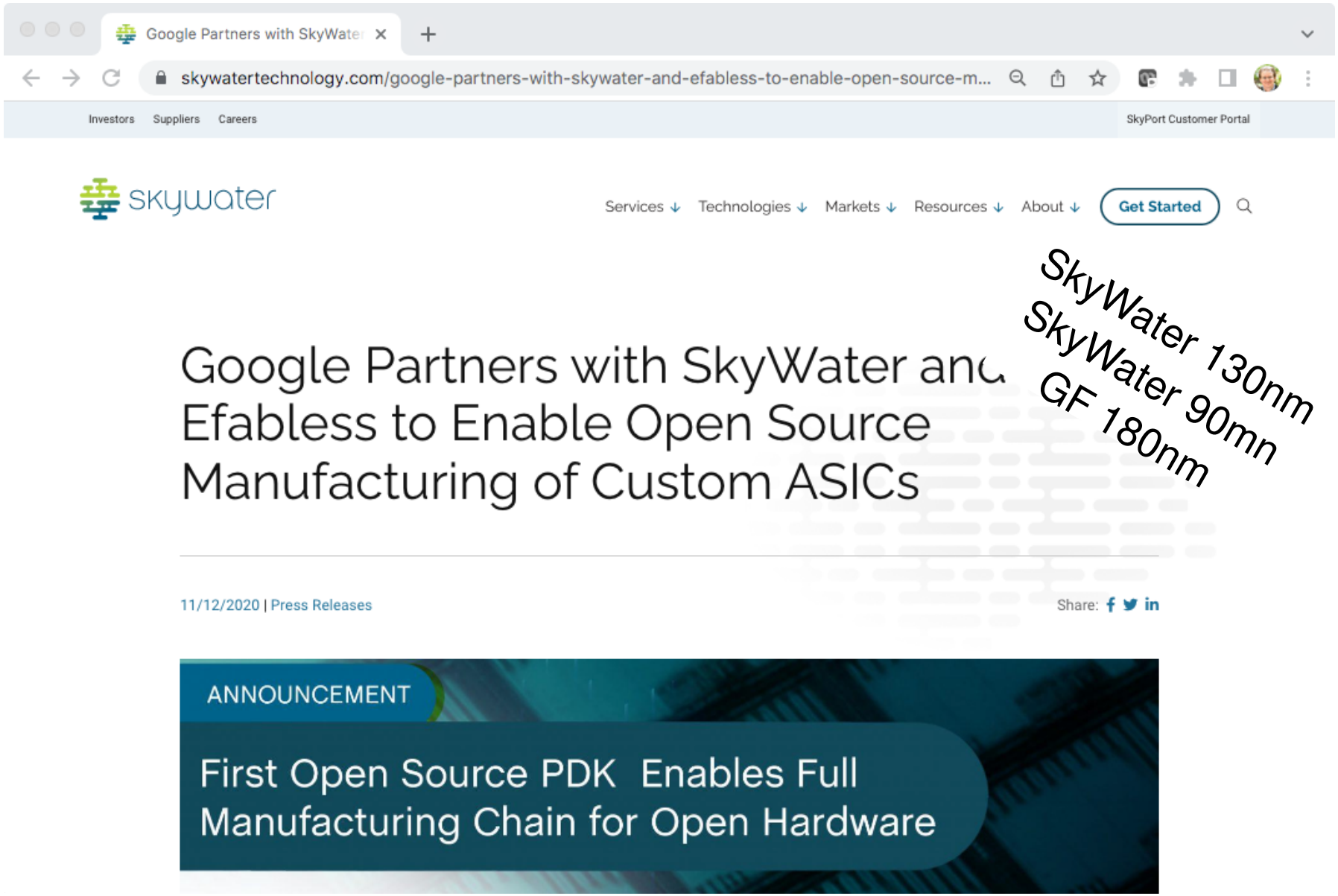
Inhouse cores:
Nvidia, +others

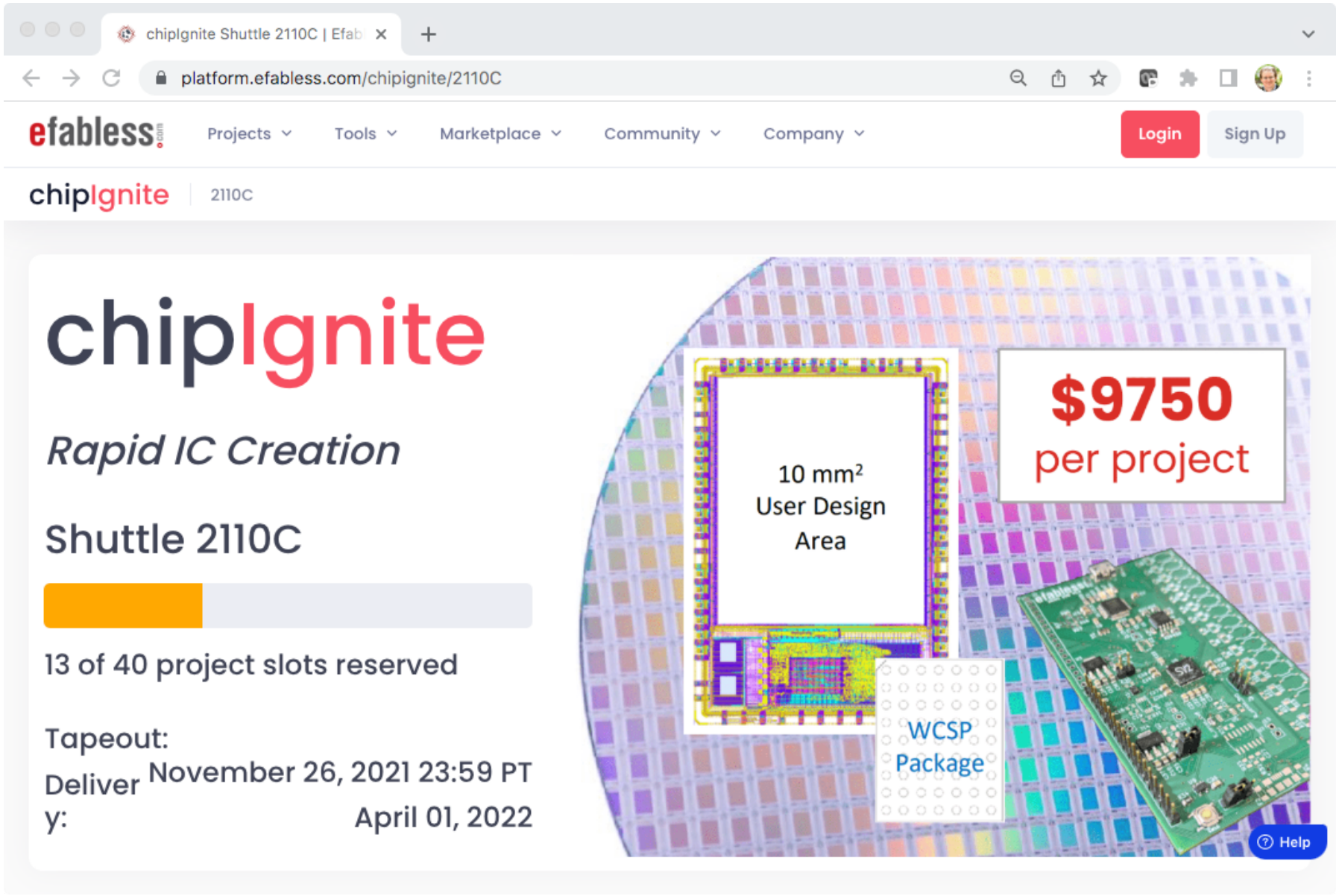
OpenROAD: The Future of Open-Source EDA

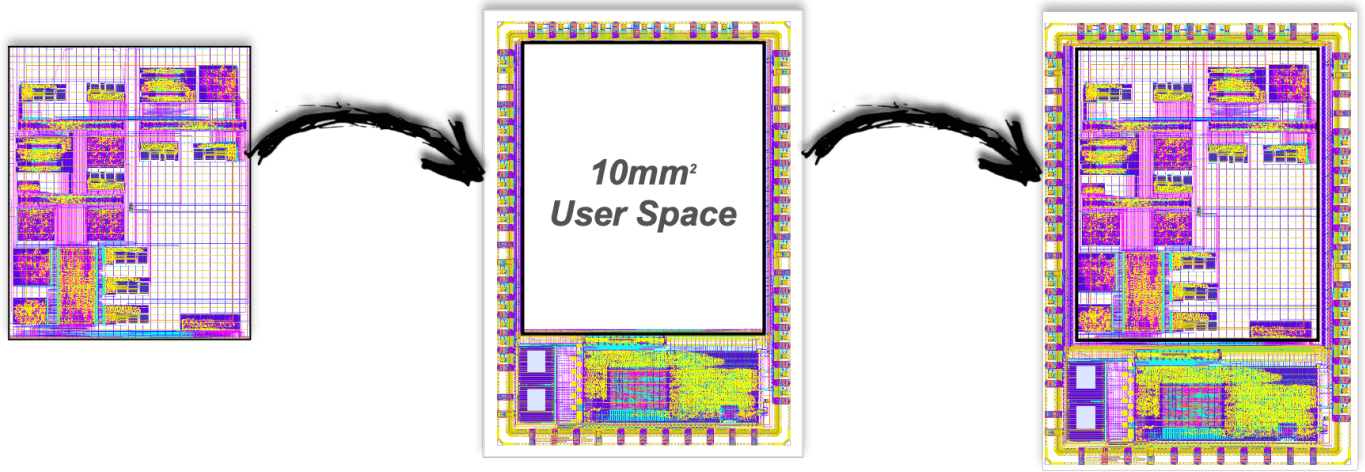


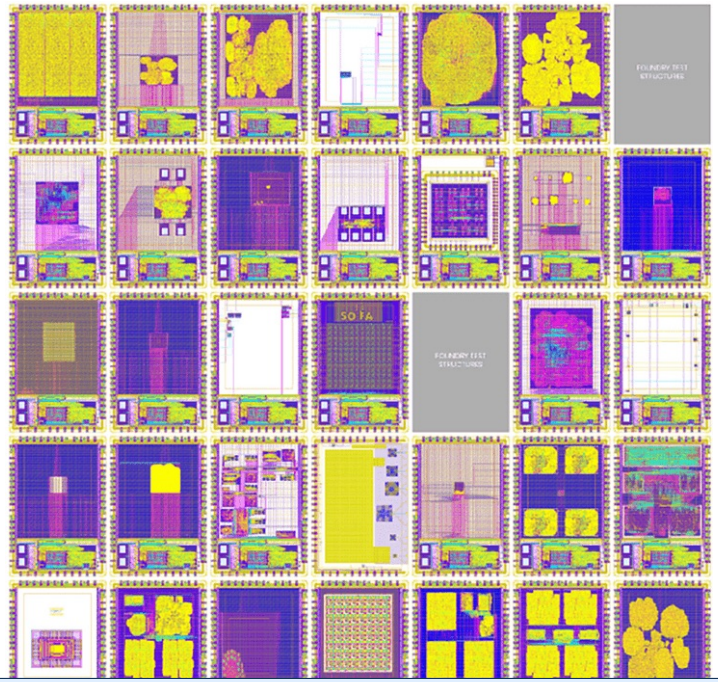


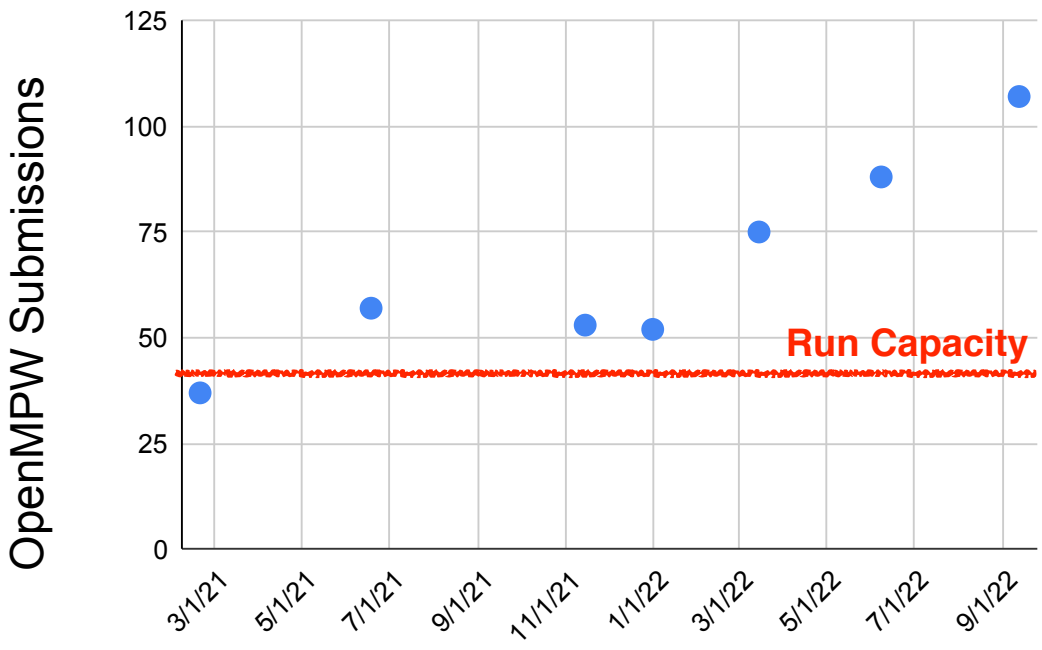
OpenTitan SoC
GF12LP


Google Partners with SkyWater
skywatertechnology.com/google-partners-with-skywater-and-efabless-to-enable-open-source-m...
Investors
Suppliers
Careers
SkyPort Customer Portal
skywater
Services
Technologies
Markets
Resources
About
Get Started
SkyWater 130nm
SkyWater 90mn
GF 180nm
Google Partners with SkyWater and
Efabless to Enable Open Source
Manufacturing of Custom ASICs
11/12/2020 | Press Releases
Share:
ANNOUNCEMENT
First Open Source PDK Enables Full
Manufacturing Chain for Open Hardware


chipIgnite Shuttle 2110C | Efab
platform.efabless.com/chipignite/2110C
efabless
Projects
Tools
Marketplace
Community
Company
Login
Sign Up
chipIgnite
2110C
chipIgnite
Rapid IC Creation
Shuttle 2110C
13 of 40 project slots reserved
Tapeout:
November 26, 2021 23:59 PT
Delivery:
April 01, 2022
10 mm²
User Design
Area
WCSP
Package
$9750
per project
Help


10mm²
User Space
YOUR DESIGN
CARAVEL
INTEGRATED CHIP




OpenMPW Submissions
125
100
75
50
25
0
Run Capacity
3/1/21
5/1/21
7/1/21
9/1/21
11/1/21
1/1/22
3/1/22
5/1/22
7/1/22
9/1/22

Call for new engineering project team proposals — Exchange

Associate Dean for Undergraduate Programs

Archive - Exchange February 22, 2022 at 12:08 PM

Details

Call for new engineering project team proposals

To: ENGRFACULTY-L, ENGRFACULTYINCSANDBEE-L, ENGRACADEMICS-L, Cc: Lauren Stulgis,

Reply-To: Associate Dean for Undergraduate Programs

Colleagues,

Through a generous donor gift creating the **Shen Fund for Social Impact** we have the opportunity to fund multiple new engineering project teams. This program is designed to bring together new student teams under a faculty member's mentorship to address significant social challenges through novel and/or advanced engineering solutions. Falling under the Project Team Umbrella, the program will fund up to three new teams per year, with each supported for a three-year period at $30K/yr. The teams will also be provided space and support to design and implement these projects.

Proposals may be submitted by either faculty looking to guide a group of students, or by students who will engage with a faculty member to form the teams.

Attached to this e-mail are three documents:

- **Shen Fund FAQ Sp22.pdf:** More fully describes the nature of the projects and the goals of the program (also copied to the e-mail below).
- **Shen Fund Proposal Template Sp22.docx:** Short project proposal form.
- **Shen Funded Projects Summary_Sp22.pdf:** A summary document of a currently funded teams.

The ideal project will likely develop through discussions with Lauren Stulgis (as director of the project teams) and me. Feel free to reach out to us with rough ideas and concepts and we can help to try to develop a viable proposal.

Proposals will be considered as they arrive, with discussions to strengthen each within the program constraints. The initial application is a simple document identifying the primary goals, technical challenges and plans, timeline and budget, and currently engaged personnel.

Proposals must be uploaded directly to Box by email to: Proposa.zeuyhp9wqg5p8teo@u.box.com. The first round of decisions will be made based on submissions received by **11:59pm on Sunday, March 13, 2022.**

Again, please feel free to contact me or Lauren Stulgis with any questions or to discuss potential projects.

Prof. Alan Zehnder
Associate Dean for Undergraduate Programs
177 Rhodes Hall
Phone: (607) 255-9181
email: eng_ugdean@cornell.edu

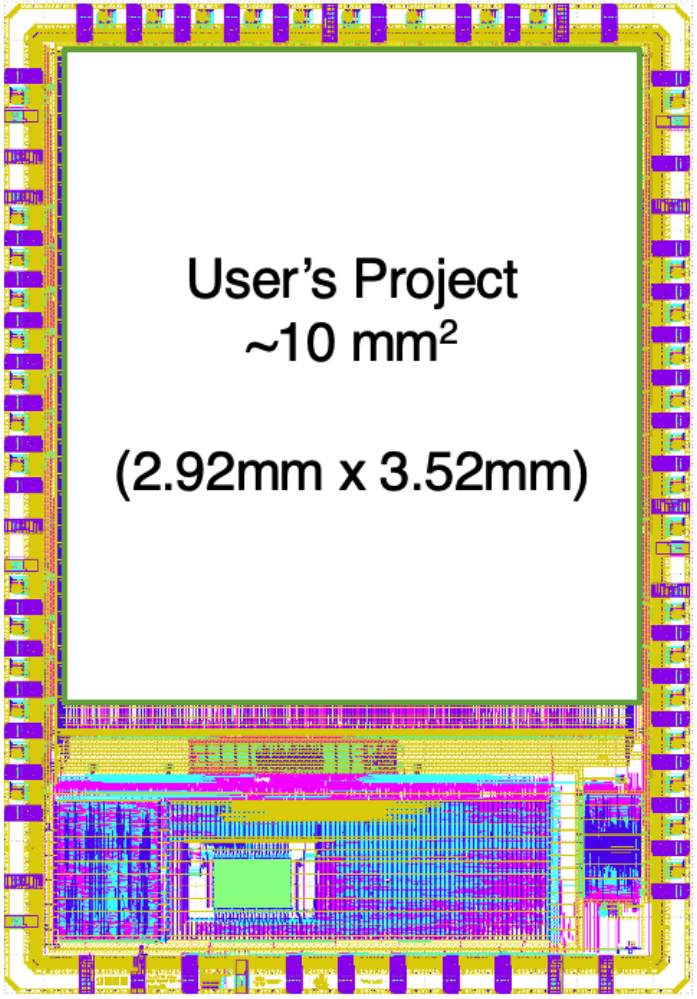
C2S2: Cornell Custom Silicon Systems Project Team

Three-year student-led project team to tapeout a custom chip in SkyWater 130nm to implement a proof-of-concept system for a campus partner

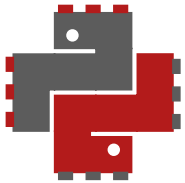
- Open RISC-V ISA
- Open-Source VexRISCV microcontoller
- Open-Source OpenROAD chip flow
- Open PDK for SkyWater 130nm
- OpenMPW + ChipIgnite w/ efabless

100+ applications $\rightarrow$ 25 team members

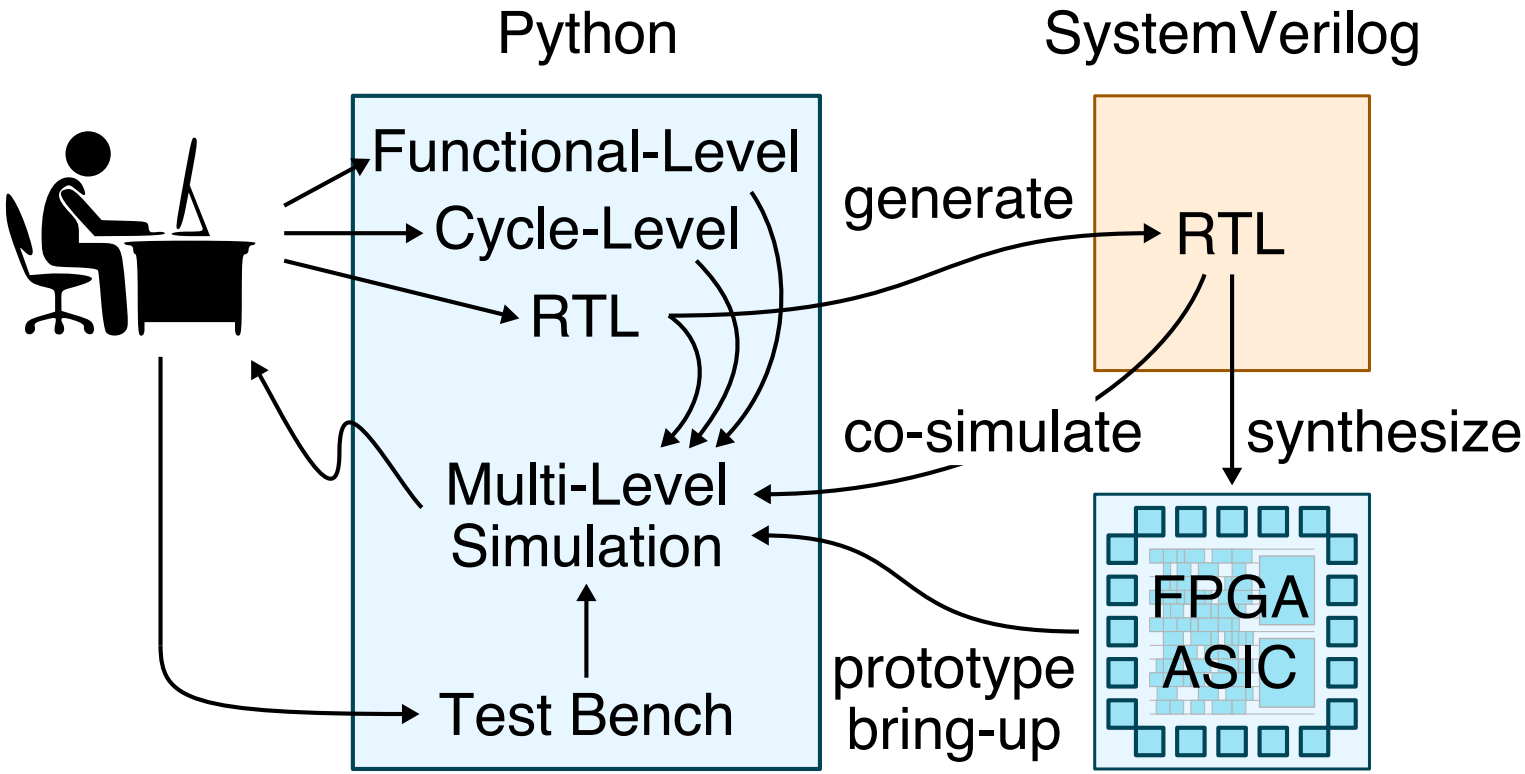
- Digital & Verification Subteam
- Analog Subteam
- Software Subteam
- System Architecture Subteam



PyMTL



Python-based hardware generation, simulation, and verification framework which enables productive RTL design and multi-level modeling



A Call to Action

- Open-source hardware needs developers who
  - ... are idealistic
  - ... have lots of free time
  - ... will work for free
- Who might that be?

  Students!
- Academics have a practical and ethical motivation for using, developing, and promoting open-source electronic design automation tools and open-source hardware designs