ECE 4750 Computer Architecture, Fall 2016
PyMTL Usage Rules

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PyMTL is embedded within Python, which is a fully general-purpose language. Given this, it is very easy to write PyMTL code that does not actually model any kind of realistic hardware. Indeed, we actually need this feature to be able to write clean and productive functional-level models, test harnesses, assertions, and line tracing. **So students must be very diligent in actively deciding whether or not they are writing synthesizable register-transfer-level models or non-synthesizable code. Students must always keep in mind what hardware they are modeling and how they are modeling it!**

Students' design work will almost exclusively use synthesizable PyMTL register-transfer-level (RTL) models. Note that students can use any Python code they like in their elaboration code; the elaboration code is all of the Python code *outside* the PyMTL concurrent blocks (i.e., outside `s.tick_rtl` and `s.combinational` blocks). This is because elaboration code is used to *generate* hardware instead of actually *model* hardware. It is also acceptable to include a limited amount of non-synthesizable code in concurrent blocks for the sole purpose of debugging, assertions, or line tracing. If the student includes non-synthesizable code in their concurrent blocks, they should demarcate this code with comments. This explicitly documents the code as non-synthesizable and aids automated tools in removing this code before synthesizing the design. **If at any time students are unclear about whether a specific construct is allowed in a synthesizable concurrent block, they should ask the instructors.**

The next page includes a table that outlines which Python constructs are allowed in synthesizable PyMTL concurrent blocks, which constructs are allowed in synthesizable PyMTL concurrent blocks with limitations, and which constructs are explicitly not allowed in synthesizable PyMTL concurrent blocks.

Always Allowed in Synthesizable Concurrent Blocks	**Allowed in Synthesizable Concurrent Blocks With Limitations**	**Explicitly Not Allowed in Synthesizable Concurrent Blocks**
`Bits`	accessing Python lists[2]	`* / // % **`
`BitStruct`	writing signals	`+= -= *= /= %= **= //=`[7]
`& | ^ ^~ ~`	`with .value/.next`[3]	`for, while, break, continue`
`and or not`	writing temporary variables[4]	`def, global, class`
`+ -`	reading `reset` signal[5]	`try, except, raise`
`>> <<`	read-modify-write `signal`[6]	`as, is, in`
`== != > <= < <=`		`with, return, yield`
`reduce_and(), reduce_or()`		`import, from`
`reduce_xor()`		`del, exec, pass`
`sext(), zext(), concat()`		`lambda`
`if, else, elif`		`finally`
`s.signal[n], s.signal[n:m]`		constructing Python lists
reading constant variables		constructing/using Python dicts
reading signals[1]		reading/writing non-signals[8]
		writing signals without `.value/.next`[9]
		reading/writing `clk` signal
		writing `reset` signal

1 Signals are instances of `InPort`, `OutPort`, `InValRdyBundle`, `OutValRdyBundle`, or `Wire`. Signals can only communicate bit-specific value types (e.g., `Bits`, `BitStruct`).

2 Accessing lists of signals or lists of models is allowed although students should be careful to keep the indexing logic relatively simple.

3 Signals must only be written using `.value` in `s.combinational` concurrent blocks. Signals must only be written using `.next` in `s.tick_rtl` concurrent blocks.

4 Writing temporary variables is allowed as long as the type of the temporary variable (e.g., the bitwidth) can be reasonably inferred.

5 Reading the special `reset` signal is allowed, but only in a `s.tick_rtl` concurrent block. Reading the `reset` signal in a `s.combinational` concurrent block is not allowed. If you need to factor the reset signal into some combinational logic, you should instead use the `reset` signal to reset some state bit, and the output of this state bit can be factored into some combinational logic. In other words, students should only use synchronous and not asynchronous resets.

6 Reading a signal, performing some arithmetic on the corresponding value, and then writing this value back to the same signal (i.e., read-modify-write) is not allowed within an `s.combinational` concurrent block. This is a combinational loop and does not model valid hardware. Read-modify-write is allowed in an `s.tick_rtl` concurrent block using `.next`, although we urge students to consider separating the sequential and combinational logic. Students can use an `s.combinational` concurrent block to read the signal, perform some arithmetic on the corresponding value, and then write a temporary wire; and use an `s.tick_rtl` concurrent block to flop the temporary wire into the destination signal.

7 These assignment operators essentially perform a read-modify-write of a signal. See the above footnote. Technically, these operators might model valid hardware if used within a `s.tick_rtl`, but this syntax is not currently supported and will result in strange simulator behavior. Therefore, these assignment operators are never allowed in synthesizable concurrent blocks.

8 Students cannot use non-signals (i.e., normal Python variables) to communicate between concurrent blocks. Students must use instances of `InPort`, `OutPort`, `InValRdyBundle`, `OutValRdyBundle`, or `Wire`.

9 Writing a signal without using `.value` or `.next` is not synthesizable and will likely result in strange simulator behavior.