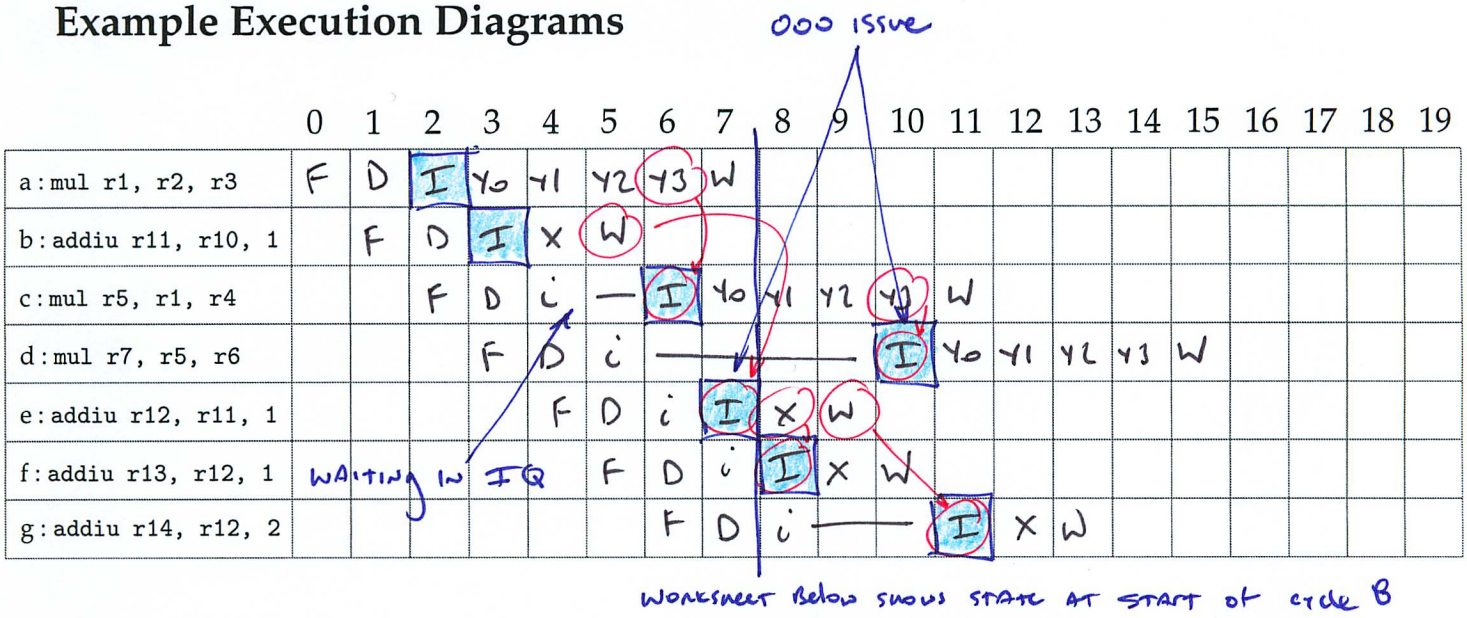
Example Execution Diagrams



Architectural Register File

r1	2
r2	1
r3	2
r4	3
r5	
r6	4
r7	
r8	
r9	
r10	21
r11	22
r12	
r13	
r14	
...	...
r31	

Issue Queue

op	imm	v	rdest	v	p	rsrc0	v	p	rsrc1
~~MUL~~	—	1	r1	1	ϕ	r12	1	ϕ	r3
~~ADDIU~~	1	1	r11	1	ϕ	r10	ϕ		—
~~MUL~~	—	1	r5	1	0	r1	1	ϕ	r4
MUL	—	1	r7	1	1	r5	1	ϕ	r6
~~ADDIU~~	1	1	r12	1	ϕ	r11	ϕ		—
ADDIU	1	1	r13	1	1	r12	ϕ		—
ADDIU	2	1	r14	1	1	r12	ϕ		—

INSTR d IS STILL NOT READY. WAITING FOR INSTR c TO COMPLETE

ON CYCLE 8, INSTR f IS WOKEN UP AND SELECTED VIA AGGRESSIVE BYPASSING

ON CYCLE 6, WITH AGGRESSIVE BYPASSING, INSTR a NOT ONLY BYPASSES DATA TO INSTR C, BUT MUST WAKEUP & NEW I STAGE SELECT C TO MAKE ALL THIS HAPPEN WITHOUT ANY BUBBLES

We can use a table to compactly illustrate how the IQ works.

			IQ Entry		
cycle	D	I	0	1	2
0					
1	a				
2	b	a	r1 | r2 | r3		
3	c	b	r11 | r10		
4	d		r5 | r1* | r4		
5	e			r7 | r5* | r6	
6	f	c			r12 | r11
7	g	e	r13 | r12		
8		f			r14 | r12
9					
10		d			
11		g			
12					
13					
14					
15					
16					
17					
18					
19					

BLANK entry MEANS this entry is free (NOT VALID)

* = pending

WAITING in IQ

g is in issue stage AND is "issuing" so next cycle it will NOT be in IQ