

Example Execution Diagrams

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
a: mul r1, r2, r3	F	D	I	Y0	Y1	Y2	Y3	W	C											
b: addiu r11, r10, 1		F	D	I	X	W	r													
c: mul r5, r1, r4			F	D	I	I	Y0	Y1	Y2	Y3	W	C								
d: mul r7, r5, r6				F	D	D	D	I	I	I	I	Y0	Y1	Y2	Y3	W	C			
e: addiu r12, r11, 1					F	F	F	D	D	D	D	I	X	W	r					
f: addiu r13, r12, 1								F	F	F	F	D	I	X	W	r				
g: addiu r14, r12, 2												F	D	I	I	X	W	r		

Worksheet below shows state at start of cycle 8

Physical Register File		Architectural Register File
r1	2	r1
r2	1	r2
r3	2	r3
r4	3	r4
r5		r5
r6	4	r6
r7		r7
r8		r8
r9		r9
r10	21	r10
r11	22	r11
r12		r12
r13		r13
r14		r14
...
r31		r31

During cycle 8 copy r1 from PAF to ANF

	p	v	rdest
p0	0	1	r1
p1	0	1	r11
p2	1	1	r5
p3	1	1	r7
p4			
p5			
p6			

Entry at head of ROB is now not pending. Commit stage will copy r1 from PAF to ANF and pop this entry off of the ROB

4. I2OL: IO Front-End/Issue, OOO Completion, Late Commit

We can use a table to compactly illustrate how the ROB works.

cycle	D	I	ROB Entry			
			0	1	2	3
0						
1	a					
2	b	a	r1*			
3	c	b		r11*		
4					r5*	
5						
6	d	c		r11		
7						r7*
8			r1			
9						
10	e	d				
11	f	e	r12*			
12	g	f		r13*	r5	
13					r14*	
14		g	r12			
15				r13		
16						r7
17					r14	
18						
19						

BLANK ENTRY MEANS THIS ENTRY IS FREE (NOT VALID)

* = pending

instr 6 writeback (completes) in cycle 5 and this updates the paf but also clears pending bit

instr 6 commits on cycle 9, next cycle this ROB entry is free