Example Execution Diagrams

<table>
<thead>
<tr>
<th>operand</th>
<th>instruction</th>
<th>result</th>
</tr>
</thead>
<tbody>
<tr>
<td>a: mul r1, r2, r3</td>
<td>F D I X Y0 Y1 Y2 Y3 W</td>
<td>000 issue</td>
</tr>
<tr>
<td>b: addiu r11, r10, 1</td>
<td>F D I X W</td>
<td></td>
</tr>
<tr>
<td>c: mul r5, r1, r4</td>
<td>F D i ------- I Y0 Y1 Y2 Y3 W</td>
<td></td>
</tr>
<tr>
<td>d: mul r7, r5, r6</td>
<td>F D i ------- I X W</td>
<td></td>
</tr>
<tr>
<td>e: addiu r12, r11, 1</td>
<td>F D i ------- I X W</td>
<td></td>
</tr>
<tr>
<td>f: addiu r13, r12, 1</td>
<td>F D i ------- I X W</td>
<td></td>
</tr>
<tr>
<td>g: addiu r14, r12, 2</td>
<td>F D i ------- I X W</td>
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</table>

Worksheet below shows state at start of cycle 8

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<th>op</th>
<th>imm</th>
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<th>rdest</th>
<th>v</th>
<th>p</th>
<th>rsrco</th>
<th>v</th>
<th>p</th>
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<td>1</td>
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Architectural Register File

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We can use a table to compactly illustrate how the IQ works.

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</table>

* = pending
Waiting in IQ

Blank entry means this entry is free (not valid)

g is in issue stage and is "issuing" so next cycle it will not be in IQ