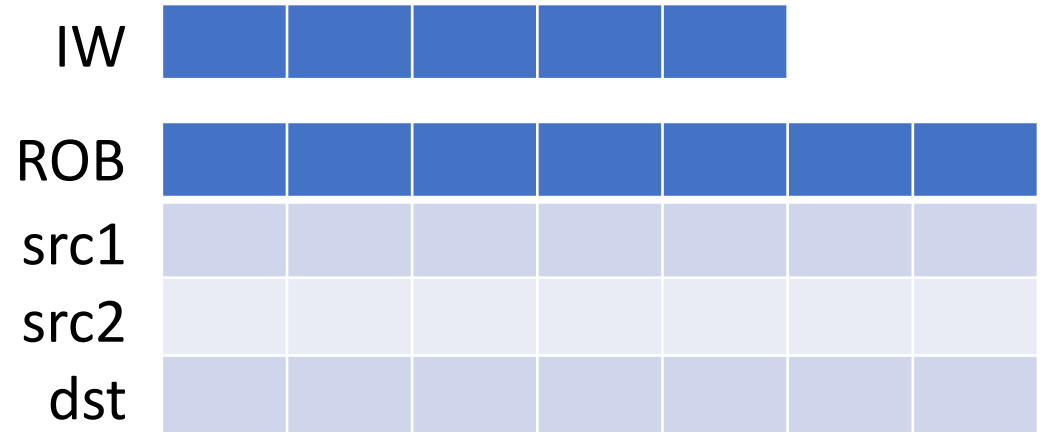
OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	
r2	
r3	
r4	
r5	
r6	

Ret. RAT	
A	P
r1	
r2	
r3	
r4	
r5	
r6	

Physical RF	
p1	
p2	
p3	
p4	
p5	
p6	
p7	
p8	
p9	
pa	
pb	

- Instructions fetched, renamed, and inserted into IW in one cycle
- Consumer instructions wake up the same cycle producer completes
- Selection logic favors older instructions
- Instructions leave IW when they issue



OoO Processing Example (Single-Issue)

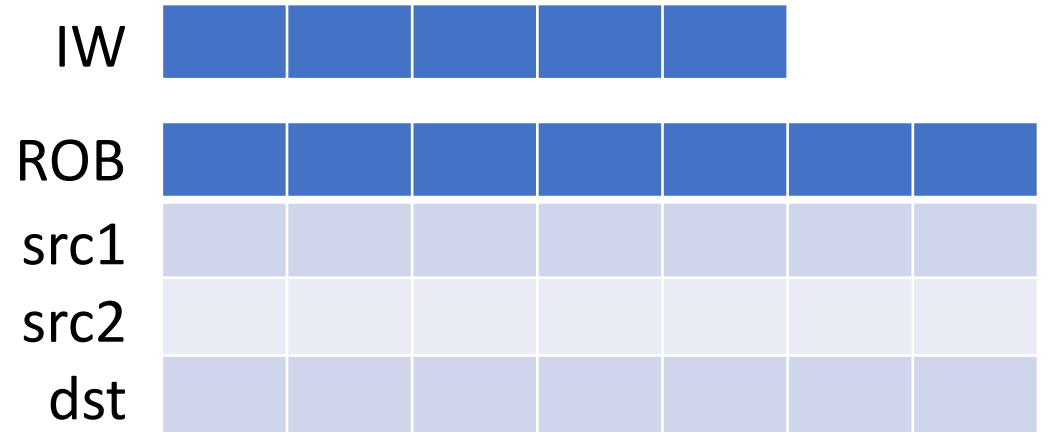
Ren. RAT	
A	P
r1	p3
r2	p7
r3	p9
r4	p1
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p7
r3	p9
r4	p1
r5	pa
r6	p4

Physical RF	
p1	37
p2	
p3	6
p4	11
p5	
p6	
p7	12
p8	
p9	65
pa	8
pb	

Free

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```



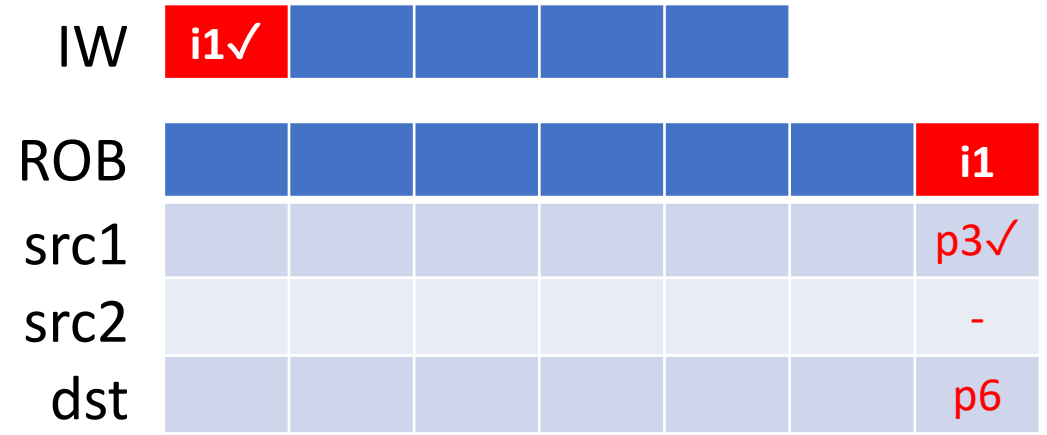
OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p6
r3	p9
r4	p1
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p7
r3	p9
r4	p1
r5	pa
r6	p4

Physical RF	
p1	37
p2	
p3	6
p4	11
p5	
p6	
p7	12
p8	
p9	65
pa	8
pb	

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```



OoO Processing Example (Single-Issue)

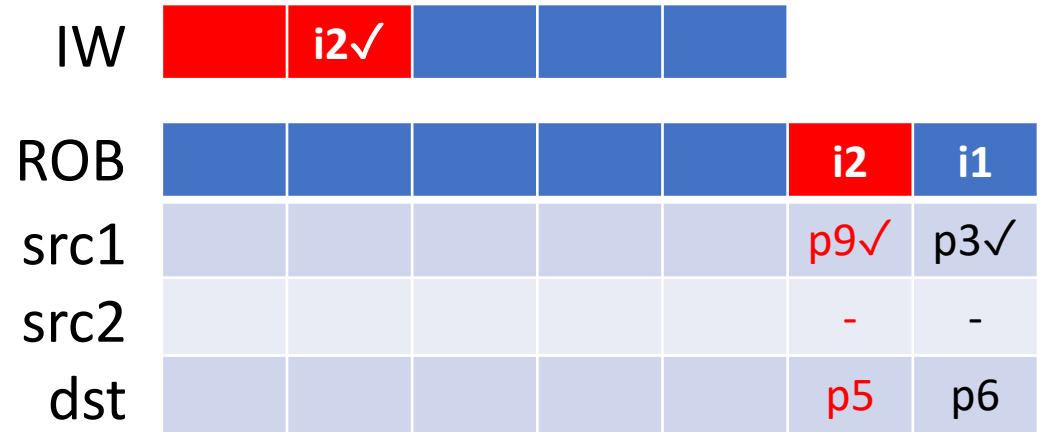
Miss

Ren. RAT	
A	P
r1	p3
r2	p6
r3	p9
r4	p5
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p7
r3	p9
r4	p1
r5	pa
r6	p4

Physical RF	
p1	37
p2	
p3	6
p4	11
p5	
p6	
p7	12
p8	
p9	65
pa	8
pb	

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```



OoO Processing Example (Single-Issue)

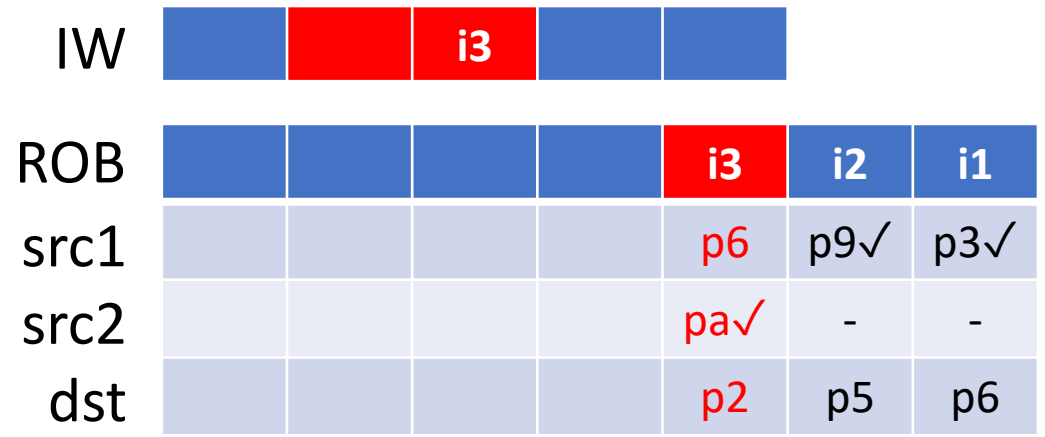
Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	p5
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p7
r3	p9
r4	p1
r5	pa
r6	p4

Physical RF	
p1	37
p2	
p3	6
p4	11
p5	
p6	
p7	12
p8	
p9	65
pa	8
pb	

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```

Hit



OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p7
r3	p9
r4	p1
r5	pa
r6	p4

Physical RF		
p1	37	
p2		
p3	6	
p4	11	
p5	87	i2
p6		
p7	12	
p8		
p9	65	
pa	8	
pb		

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2✓
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```

IW			i3	i4✓		
ROB				i4	i3	i2✓	i1
src1				p5✓	p6	p9✓	p3✓
src2				p4✓	pa✓	-	-
dst				pb	p2	p5✓	p6

OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p7
r3	p9
r4	p1
r5	pa
r6	p4

Physical RF	
p1	37
p2	
p3	6
p4	11
p5	87
p6	
p7	12
p8	
p9	65
pa	8
pb	

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```

IW			i3		i5		
ROB			i5	i4	i3	i2✓	i1
src1			pa✓	p5✓	p6	p9✓	p3✓
src2			p2	p4✓	pa✓	-	-
dst			-	pb	p2	p5✓	p6

OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p7
r3	p9
r4	p1
r5	pa
r6	p4

Physical RF		
p1	37	
p2		
p3	6	
p4	11	
p5	87	
p6	54	i1
p7	12	
p8		
p9	65	
pa	8	
pb	98	i4

```
ld   r2, 0(r1)      ;i1✓
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4✓
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```

IW						
	i6✓		i3✓		i5	

ROB		i6	i5	i4✓	i3	i2✓	i1✓
src1		p4✓	pa✓	p5✓	p6✓	p9✓	p3✓
src2		pb✓	p2	p4✓	pa✓	-	-
dst		-	-	pb✓	p2	p5✓	p6✓

OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p6
r3	p9
r4	p1
r5	pa
r6	p4

Physical RF	
p1	37
p2	
p3	6
p4	11
p5	87
p6	54
p7	
p8	
p9	65
pa	8
pb	98

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```

IW						
	i6✓				i5	

ROB		…	i6	i5	i4✓	i3	i2✓	(i1)
src1		…	p4✓	pa✓	p5✓	p6✓	p9✓	
src2		…	pb✓	p2	p4✓	pa✓	-	
dst		…	-	-	pb✓	p2	p5✓	(p6)

OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p6
r3	p9
r4	p5
r5	pa
r6	p4

Physical RF		
p1		
p2	62	i3
p3	6	
p4	11	
p5	87	
p6	54	
p7		
p8		
p9	65	
pa	8	
pb	98	

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3✓
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6☞
...
```

IW					i5✓		

ROB			...	i6	i5	i4✓	i3✓	(i2)
src1			...	p4✓	pa✓	p5✓	p6✓	
src2			...	pb✓	p2✓	p4✓	pa✓	
dst			...	-	-	pb✓	p2✓	(p5)

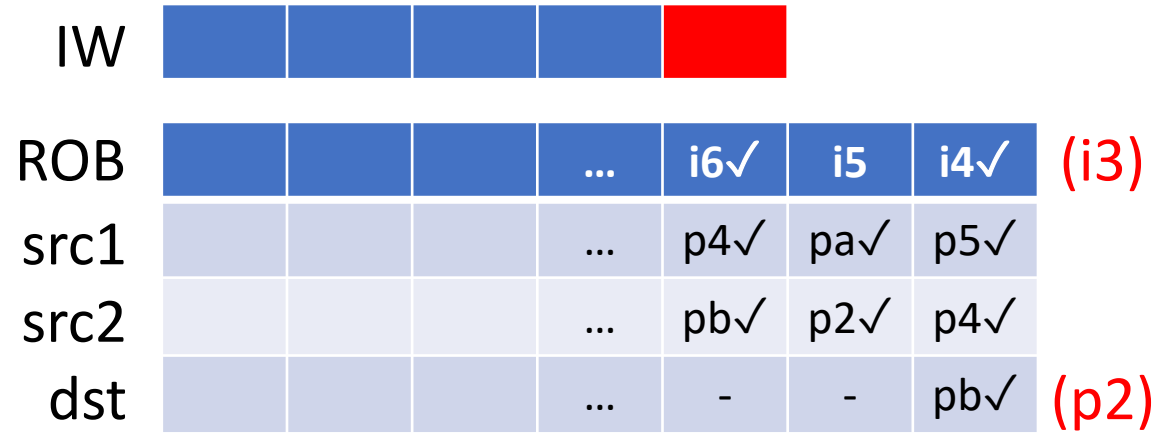
OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	p5
r5	pa
r6	p4

Physical RF	
p1	
p2	1
p3	6
p4	11
p5	87
p6	
p7	
p8	
p9	65
pa	8
pb	98

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5 ☞
st   r4, 0(r6)      ;i6 ✓
...
```



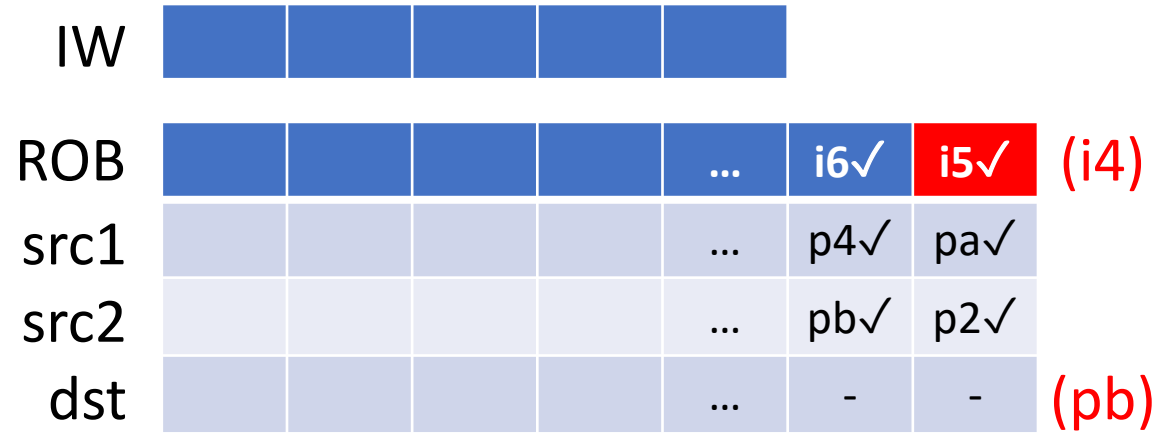
OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Physical RF	
p1	
p2	1
p3	6
p4	11
p5	
p6	
p7	
p8	
p9	65
pa	8
pb	98

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5✓
st   r4, 0(r6)      ;i6
...
```



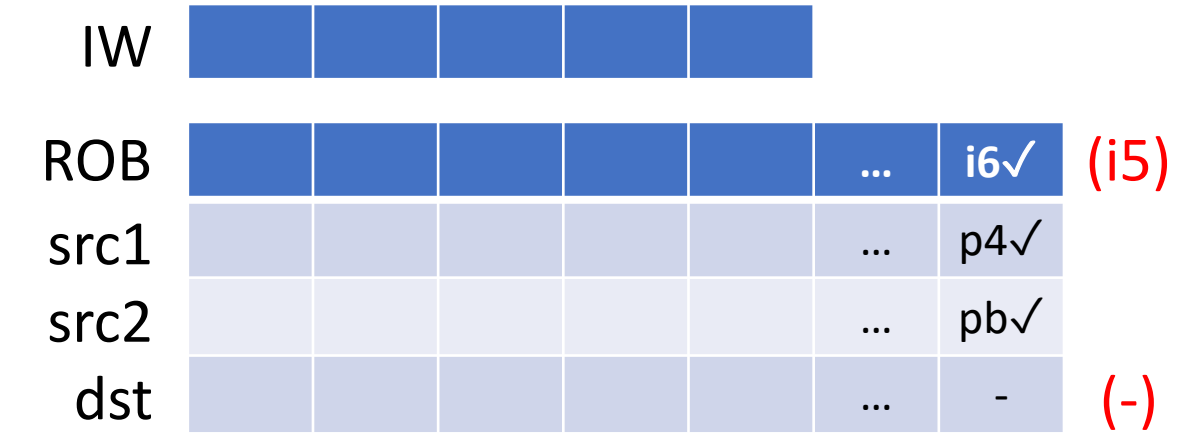
OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Ret. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Physical RF	
p1	
p2	1
p3	6
p4	11
p5	
p6	
p7	
p8	
p9	65
pa	8
pb	98

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```



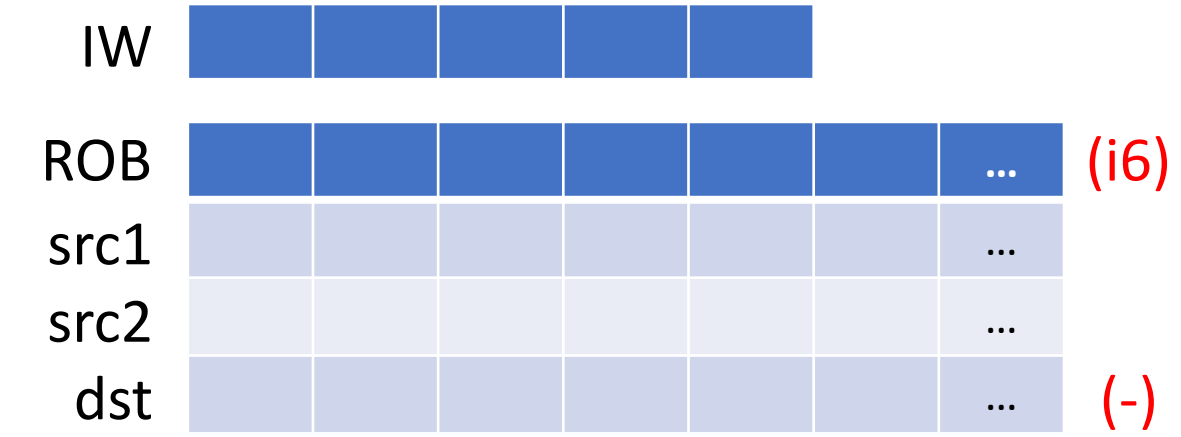
OoO Processing Example (Single-Issue)

Ren. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

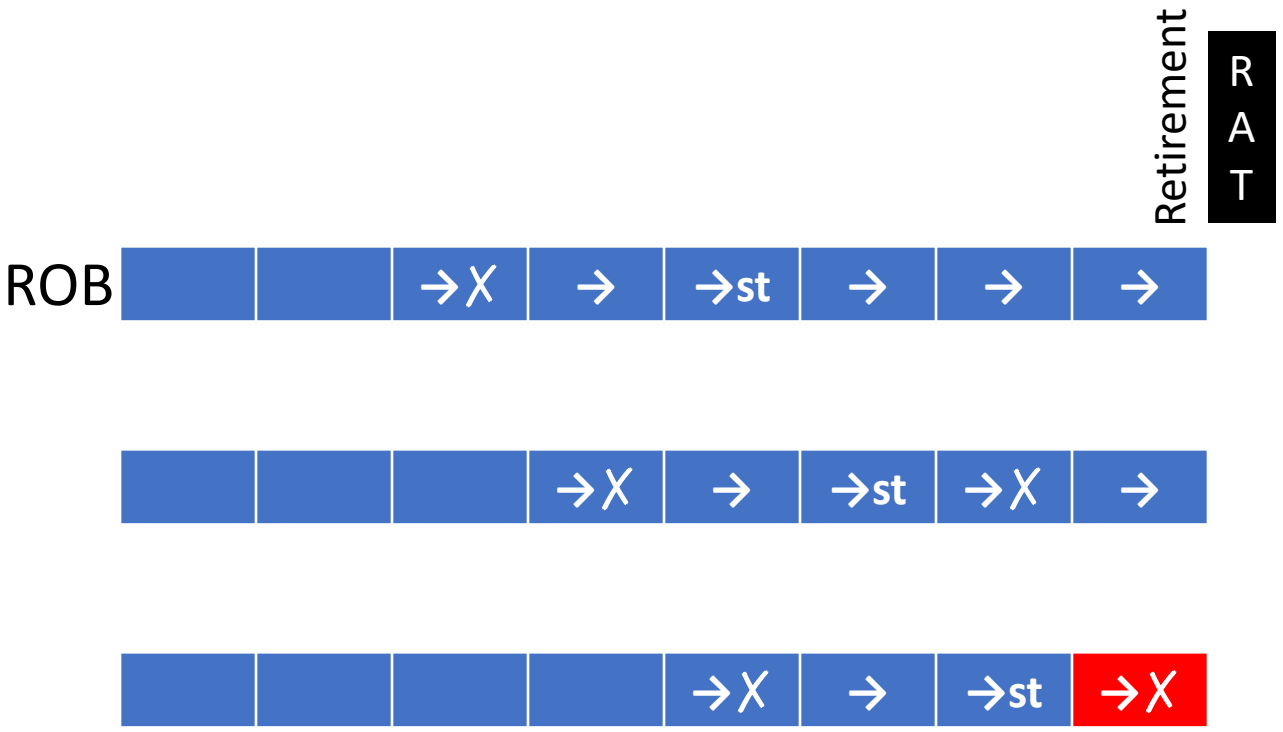
Ret. RAT	
A	P
r1	p3
r2	p2
r3	p9
r4	pb
r5	pa
r6	p4

Physical RF	
p1	
p2	1
p3	6
p4	11
p5	
p6	
p7	
p8	
p9	65
pa	8
pb	98

```
ld   r2, 0(r1)      ;i1
ld   r4, 0(r3)      ;i2
add  r2, r2, r5     ;i3
add  r4, r4, r6     ;i4
st   r2, 0(r5)      ;i5
st   r4, 0(r6)      ;i6
...
```

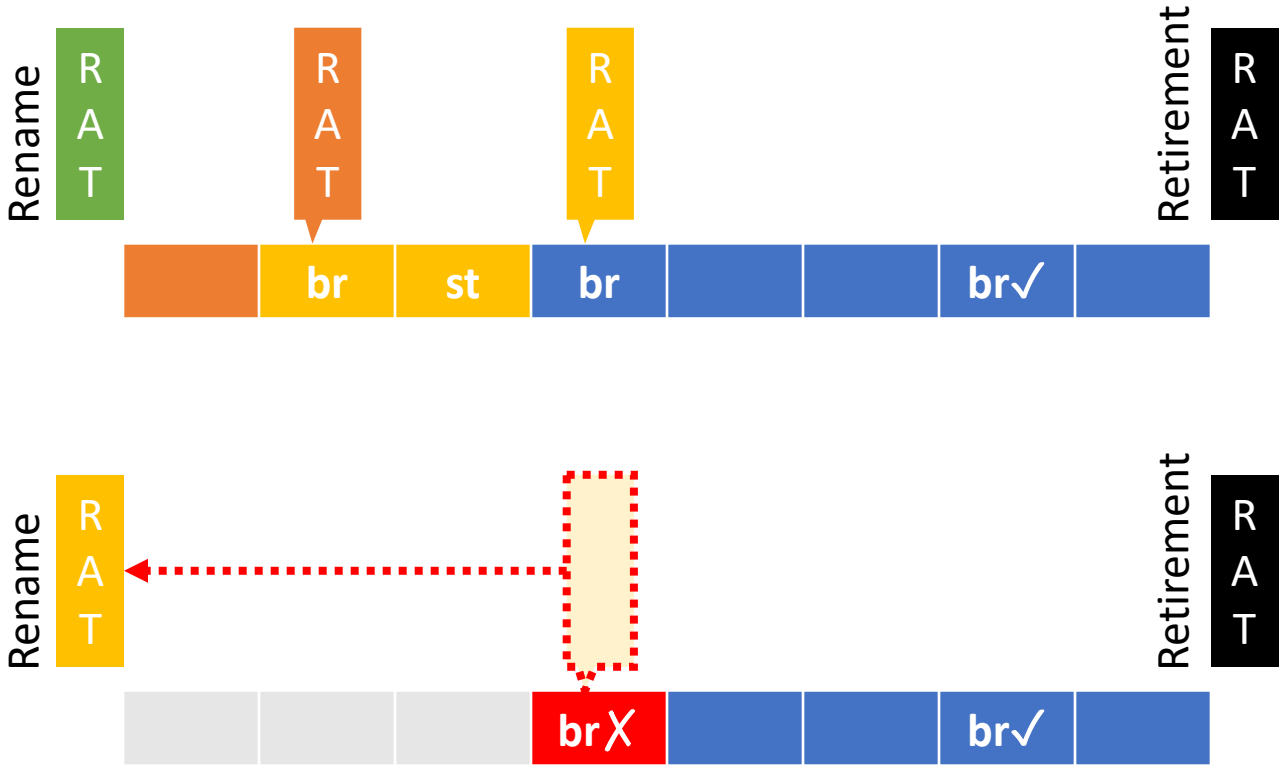


Precise Exceptions



- Wait until instruction w/ raised exception reaches ROB head; continue updating retirement RAT
- If it reaches ROB head, save retirement RAT's context and service exception
- Stores hold values in in-order *write buffer* until commit (but can forward)

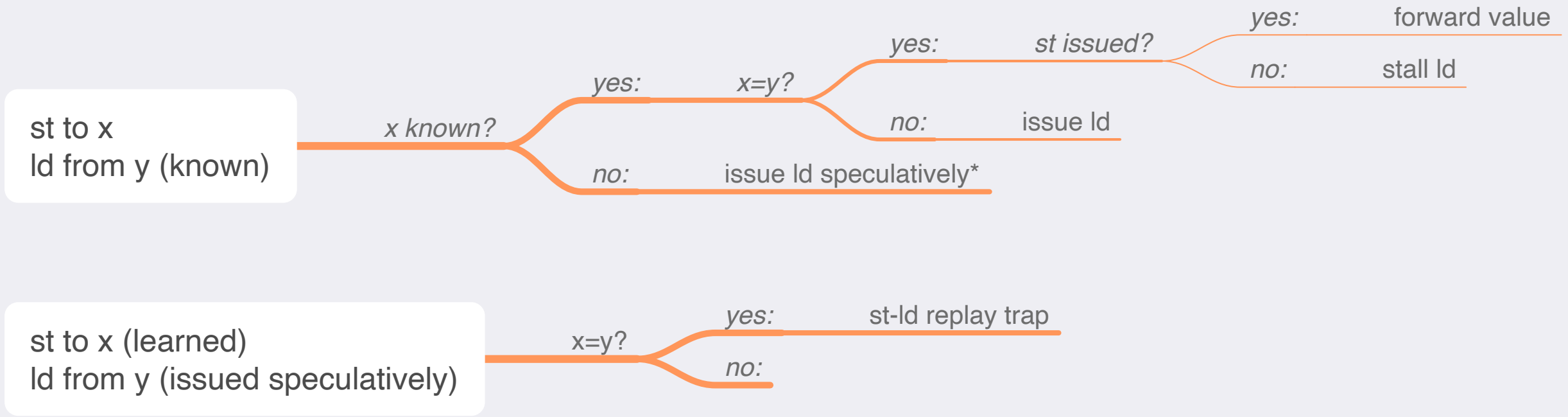
Speculative Execution



- Take Rename RAT snapshot into the ROB of the predicted instruction (e.g., branch)
- On a misprediction
  - Free diffRAT(Rename,Branch)
  - Copy Branch RAT to Rename RAT
  - Squash all instructions that follow mispredicted branch
  - Clear write buffer entries that follow mispredicted branch

Store-Load Reordering

```
st   r2, 0(r1)     ;i1
ld   r4, 0(r3)     ;i2
```



*Could stall instead, or use st-ld predictor

Store-Load Redefinitions

- Resolution of “?” irrelevant to ld
  - If not x, definitely irrelevant
  - If x, newer st x *shields* ld
- Recall: store values preserved in order in write buffer until commit