A 1.9 GS/s 4-bit Sub-Nyquist Flash ADC for 3.8 GHz Compressive Spectrum Sensing in 28 nm CMOS

David Bellasi, Luca Bettini, Thomas Burger, Qiuting Huang
ETH Zürich, Zürich, Switzerland
{bellasi, bettini, burger, huang}@iis.ee.ethz.ch

Christian Benkeser
RUAG Space, Switzerland
christian.benkeser@ruag.com

Christoph Studer
Cornell University, NY
studer@cornell.edu

***Abstract*—Spectral activity detection in wideband radio-frequency (RF) signals for cognitive-radio applications typically necessitates expensive and energy-inefficient analog-to-digital converters (ADCs). In this paper, we present a novel compressive sensing (CS)-based analog front-end, which is able to sample sparse wideband RF signals at low cost and low power. The analog front-end consists of a pseudo-random non-uniform clock generator unit offering the possibility to configure the (average) undersampling factor at run-time, and a low-cost, wideband 1.9 GS/s 4-bit flash ADC. The spectral information acquired at sub-Nyquist rates can be recovered off-line via a novel sparse signal dequantization algorithm. The developed analog front-end is implemented in 28 nm CMOS, and enables the recovery of spectrally sparse RF signals up to 3.8 GHz by means of CS, which corresponds to a Nyquist-equivalent sampling rate of 7.6 GS/s. The ADC and pseudo-random clock generator together occupy less than 0.1 mm^2, and consume an estimated 4.1 mW to 5.4 mW for undersampling factors between 4 and 11.5.**

I. Introduction

Cognitive radio detects active frequency bands in the radio-frequency (RF) spectrum in order to opportunistically re-use unused frequency bands for data transmission [2]. Since the wireless spectrum is a scarce and expensive resource, cognitive radio in combination with spectrum sensing is expected to play a major role in meeting the demand for higher data rates in future wireless systems. Conventional high-rate and high-precision analog-to-digital converters (ADCs) offer a straightforward way for acquiring RF signals in the GS/s regime and detecting the active frequency bands. Such off-the-shelf conversion circuits are, however, energy-inefficient and expensive [3], [4], which prohibits their deployment in low-cost, battery-powered devices. Consequently, the development of novel, low power and low cost wideband spectrum sensing solutions is key in the deployment of cognitive radio in practice.

A number of spectrum-occupancy surveys revealed that the RF spectrum is, in many practical scenarios, sparsely populated (see, e.g., [5]). As a consequence, sampling wideband signals at the Nyquist rate, while only a few RF bands are active at a given time, seems to be an inefficient way of extracting the low-dimensional spectral activity information. Compressive sensing (CS) is a recent sampling paradigm that enables one to acquire frequency-sparse signals at sub-Nyquist rates, while enabling the detection of the active frequency bands [6]. For the considered spectrum-sensing application, CS enables the development of new analog front-ends, which compressively sample sparse wideband signals using inexpensive, energy-efficient analog circuitry, while sophisticated recovery algorithms extract the spectral occupancy information off-line [7], [8] or in dedicated circuits [1].

This paper describes an analog front-end for compressive wideband spectrum sensing. In contrast to the CS-based ADC in [7] that is implemented using an expensive InP HBT technology, our front-end is implemented in a standard 28 nm bulk CMOS technology. The proposed CS-based ADC is illustrated in Figure 1, and is capable of acquiring sparse wideband RF signals at low-complexity and low power. The analog front-end consists of (i) a pseudo-random non-uniform clock generator unit with programmable undersampling rate and (ii) a low-area, low-power 4-bit flash ADC. Both units together enable one to acquire and accurately recover the spectral activity information for a bandwidth up to 3.8 GHz by means of CS signal recovery. To demonstrate the efficacy of the proposed analog front-end, we show implementation results, as well as system-level simulations with synthetic and real measured data.

Parts of this paper appeared in [1]. The present paper describes an improved, configurable pseudo-random clock generation unit and provides additional design details on the 4-bit flash ADC that were omitted in [1].

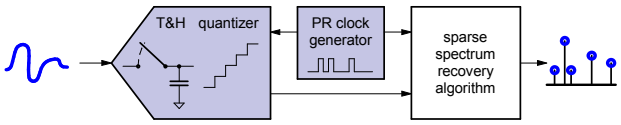


Fig. 1. Schematic diagram of the compressive sensing-based analog front-end consisting of a pseudo-random non-uniform clock generator unit and a low-complexity wideband 4-bit flash ADC. The compressively acquired spectrum can then be recovered via sophisticated sparse signal recovery algorithms.

II. Compressive Spectrum Sensing

A. The Basics

Compressive sensing (CS) enables sampling and reconstruction of signal vectors $\mathbf{y} \in \mathbb{R}^N$ at sub-Nyquist rates, if they admit a sparse representation $\mathbf{x}$ with only $K \ll N$ non-zero entries in a known orthonormal basis $\mathbf{\Psi}$, i.e., $\mathbf{y} = \mathbf{\Psi x}$. More specifically, CS acquires M measurements of the signal vector $\mathbf{y}$ as $\mathbf{z} = \mathbf{\Phi y} + \mathbf{n}$ [6]. Here, $\mathbf{\Phi} \in \mathbb{R}^{M \times N}$ is an sampling matrix with fewer rows than columns ($M < N$) and $\mathbf{n} \in \mathbb{R}^M$ models additive measurement noise. Given that the effective matrix $\mathbf{D} = \mathbf{\Phi\Psi}$, consisting of the sampling matrix and the sparsifying basis, satisfies certain conditions [6], CS enables one to accurately recover the signal vector $\mathbf{y}$ from the compressive measurements in $\mathbf{z}$. For compressive spectrum sensing, the sampling matrix $\mathbf{\Phi}$ and the sparsifying basis $\mathbf{\Psi}$ correspond to a pseudo-random subsampling operator (i.e., a $0/1$ matrix with more columns than rows, where each row only contains a single 1) and to the discrete Fourier transform (DFT) matrix, respectively. This combination enables the acquisition and recovery of spectrally sparse RF signals at sampling rates well-below the Nyquist rate [6].

B. Quantized Compressive Sensing

In virtually all practical applications, the compressive measurements are acquired by an ADC. To take ADC quantization into account, the compressive sensing process is modeled as follows [1]:

$$\mathbf{q} = \mathcal{Q}(\mathbf{z}) = \mathcal{Q}(\mathbf{Dx} + \mathbf{n}), \tag{1}$$

where $\mathcal{Q}(\cdot)\colon \mathbb{R} \to \mathcal{O}$ is a scalar quantizer, which maps a real number x into $Q = |\mathcal{O}|$ ordered labels according to $\mathcal{Q}(x) = q$ if $b_{q-1} < x \leq b_q$, $q \in \mathcal{O}$, with the bin boundaries $-\infty = b_0 < \cdots < b_Q = +\infty$. The goal of quantized CS is to recover the sparse vector $\mathbf{x}$ from the quantized measurements in $\mathbf{q}$. Coarse quantization has the benefit of further reducing the measurement dimensionality (in addition to pseudo-random subsampling); this enables the use of low-precision ADCs that require low area and power.

To recover the sparse representation $\mathbf{x}$ from the quantized measurements $\mathbf{q}$, one can assume that the noise vector $\mathbf{n}$ in (1) is i.i.d. zero-mean Gaussian with variance σ^2; this allows us to compute the likelihood of each measurement q_i as follows [1]:

$$p(q_i \,|\, \mathbf{d}_i^H \mathbf{x}) = \int_{\ell_i}^{u_i} \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{|\nu - \mathbf{d}_i^H \mathbf{x}|^2}{2\sigma^2}\right) d\nu. \qquad (2)$$

Here, $u_i = b_{q_i}$ and $\ell_i = b_{q_i-1}$ are the upper and lower bin boundary positions associated with q_i, respectively, and $\mathbf{d}_i^H$ corresponds to the i^{th} row of $\mathbf{D} = \mathbf{\Phi}\mathbf{\Psi}$. The idea behind the recovery method in [1] is to minimize the negative log-likelihood of (2) together with a sparsity-inducing ℓ_1-norm penalty. The resulting convex optimization problem, referred to as basis pursuit de-quantization (BPDQ), corresponds to

$$\text{(BPDQ)} \qquad \underset{\tilde{\mathbf{x}} \in \mathbb{C}^N}{\text{minimize}} \; \lambda \|\tilde{\mathbf{x}}\|_1 - \textstyle\sum_{i=1}^{M} \log p(q_i \,|\, \mathbf{d}_i^H \tilde{\mathbf{x}}),$$

where the parameter $\lambda > 0$ can be used to trade sparsity of the solution $\hat{\mathbf{x}}$ for consistency to the quantized samples in $\mathbf{q}$. The BPDQ problem can be solved efficiently using the algorithm proposed in [1].

In the following two sections, we detail a novel analog-front end for wideband compressive spectrum sensing in 28 nm CMOS. Our design acquires coarsely quantized samples as in (1), where the sensing matrix $\mathbf{\Phi}$ is a pseudo-random subsampling matrix. The outputs of the proposed CS-based ADC are then used to recover the spectral activity information off-line (see Figure 1 for a system overview).

III. Configurable Pseudo-Random Non-Uniform Clock Generator

Sub-Nyquist wideband signal acquisition using the proposed approach requires a pseudo-random non-uniform sampling clock at high rates to implement the sampling operator $\mathbf{\Phi}$.

In existing CS-based ADC designs, the methods for generating the non-uniform sampling clock either provide only very short sequences [9], are complex and energy inefficient [10], or generate the clock off-chip using expensive equipment [7], [10]. In this paper, we develop a low-area and low-power clock-generation unit that derives a high-rate non-uniform clock on-chip from an external Nyquist clock with period T_{clk}. Our circuit is able to continuously generate a pseudo-random sampling pattern of 23548 bits at high rates, and the undersampling rate is configurable at run-time.

The architecture of the proposed sub-Nyquist clock generator unit is shown in Figure 2. The circuit is built solely from digital standard-cells and consists of a linear feedback shift register (LFSR), and a circular shift register with variable length formed by a pipelined multiplexer tree and a shift register (SR). A single logical 1, initially set by the RST signal in the first flip-flop (FF) of the SR, is propagated by the input clock signal through this circular shift register whose length is pseudo-randomly changed via the multiplexer's selection bits B'_0–B'_3. The state of the multiplexer output represents the non-uniform sampling clock signal ϕ_{nus}. The pseudo-random sampling period T_{rnd} is an integer multiple of the uniform input clock period and is given by $T_{\text{rnd}} = T_{\text{min}} + N_{\text{rnd}}\, T_{\text{clk}}$, where the minimum sampling period T_{min} is equal to the time required by the logical 1 to propagate through the pipeline registers of the multiplexer tree and the first FF of the SR.

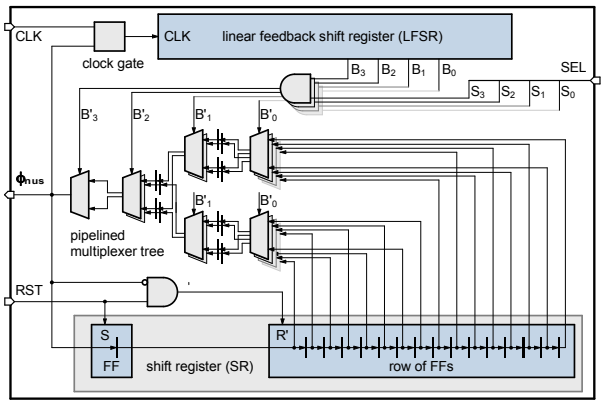


Fig. 2. Circuit diagram of the pseudo-random, non-uniform clock generator with configurable undersampling factor. The clock generator is implemented with digital standard-cells only and achieves up to 7.8 GHz at only 0.65 mW.

N_{rnd} is the pseudo-random binary number coded by B'_0–B'_3, that are the 4 least significant bits of the LFSR masked by the undersampling configuration signal SEL.

In the present design, the minimum sampling period is $4\,T_{\text{clk}}$, which corresponds to the four operating phases of the ADC (see Section IV) and allows us to optimally pipeline the multiplexer tree. The maximum sampling period T_{max} can be configured via the SEL signal by restricting the maximum length of the circular shift register. With this, we can configure the undersampling factor at run-time to 11.5, 7.5, 5.5, 4.5, or 4. Every time the logical 1 reaches the multiplexer output the LFSR is triggered to generate a new pseudo-random number. The LFSR has a length of 11 and is structured such that all generated sampling periods occur nearly equally often. The proposed clock generation circuit achieves a maximum clock frequency of 7.8 GHz and consumes only 0.65 mW.[1]

IV. 4-bit Flash ADC

To be able to compressively acquire large bandwidths at low cost and low power, we designed a low-resolution 4-bit flash ADC running at a maximum sampling rate of 1.9 GS/s.

A schematic diagram of the 4-bit flash ADC is depicted in Figure 3 (a). Fifteen identical comparators $\mathsf{Q}_1, \ldots, \mathsf{Q}_{15}$ compare the input voltage to 15 equally spaced reference voltages $\mathsf{V}_{\text{ref1}}, \ldots, \mathsf{V}_{\text{ref15}}$ generated by a resistor ladder. The resulting thermometric code is then converted to the standard binary number representation. Each comparator is composed of a static differential-difference preamplifier (DDPA), followed by a double-tail latch (DTL) and by an SR-latch, as shown in Figure 3 (e). Sampling is performed directly by the preamplifier itself at the input of the quantizer, thereby avoiding a dedicated track-and-hold (T&H) stage. More specifically, a single sampling switch is shared by all the comparators, while the total gate capacitance of the input transistors of the DDPA, approximately equal to 500 fF, serves as sampling capacitance. Driving the switch with a bootstrapped clock phase ϕ_{nus} directly derived from the non-uniform clock signal effectively eliminates any signal-dependent modulation of the sampling switch on-resistance. The ADC operates in four phases depicted in Figure 3 (d). In particular, ϕ_{nus} is the bootstrapped sampling clock, ϕ_{r} resets the comparators input prior to starting a new acquisition cycle, ϕ_{c} disconnects the DDPA from the DTL to

[1]The estimated power consumption was obtained from transistor-level simulations at the nominal supply voltage of 1.0 V and under standard conditions using Cadence Spectre.

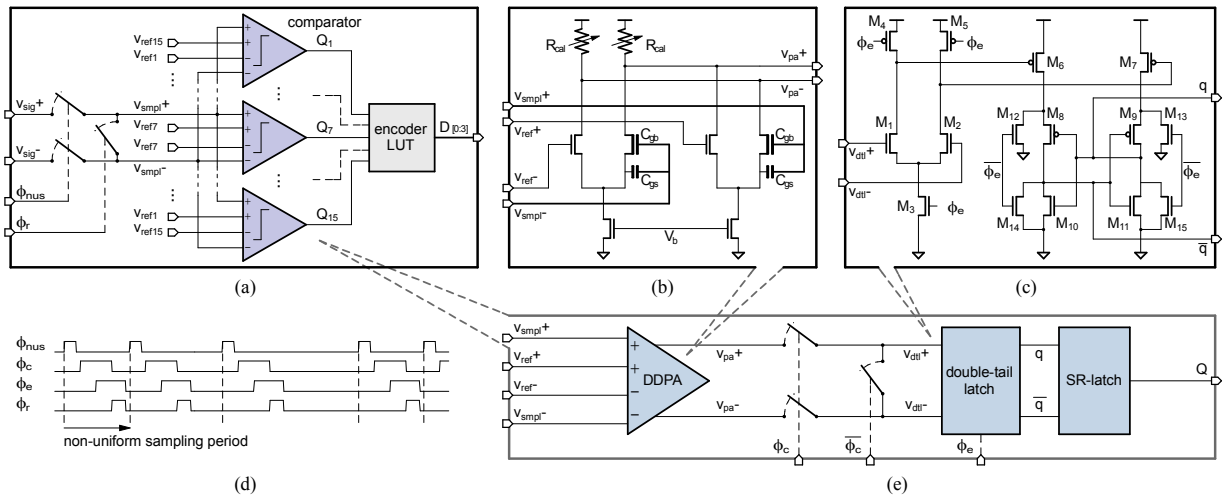


Fig. 3. Circuit diagram of the proposed 4-bit flash ADC for compressive spectrum sensing: (a) converter circuit; (b) differential difference pre-amplifier; (c) double-tail latch; (d) clock signals; (e) comparator circuit.

reduce kick-back noise and, in its inverted phase, shorts the outputs of the preamplifier to ensure fast overdrive recovery and finally ϕ_e defines the latching instant.

The DDPA shown in Figure 3 (b) consists of two NMOS differential pairs combined with two trimmable resistive loads to ensure fast operation. The resistors can be digitally calibrated to assume values between $770\,\Omega$ and $5\,\mathrm{k}\Omega$, in order to compensate for comparator mismatch. The output common mode voltage of the DDPA is set to the optimal operating point of the input pair of the successive latch, i.e., to $750\,\mathrm{mV}$. The matching requirements of the DTL are relaxed by the gain of the preamplifier, approximately $3\,\mathrm{dB}$, which allows us to employ small and fast transistors in the latch. The latch stage itself is a modified version of the double-tail voltage sense amplifier reported in [11] (see Figure 3 (c)). In our design, the drain of the input transistors M_1–M_2 directly controls the gate of M_6–M_7, in order to inject the differential signal into the latch and to trigger it. M_6 and M_7 are large enough to ensure sufficient driving current to toggle at high speed, whereas minimum sizing is adequate for M_{12}–M_{15}. Connecting the large transistors to the output of the first stage minimizes the contribution to the input-referred offset. The reset switches are driven by the phase $\overline{\phi}_e$ and reset the DTL at the end of each comparison.

The main drawback of the chosen topology is the kick-back noise generated by the toggling of ϕ_e at the beginning of each comparison and when resetting the latch. While the common mode component of the kick-back noise is usually not large enough to alter the operating point of the circuit, the differential noise can propagate back toward the input pair and the reference ladder, affecting the ADC's precision. In our design, the corruption of the next sample value by the falling edge of ϕ_e is avoided by completely disconnecting the DTL from the DDPA by means of a pair of switches controlled by ϕ_c. During the rising edge of ϕ_e, the static nature of the DDPA is able to attenuate the differential kick-back noise sufficiently.

The entire analog front-end was designed in a $28\,\mathrm{nm}$ 1P7M bulk CMOS technology with a single $1.0\,\mathrm{V}$ supply. We note that the layout of the analog front-end is part of ongoing work. Nevertheless, by comparing our design with a structurally similar 3.5-bit flash ADC in $130\,\mathrm{nm}$ CMOS [12], we can extract a conservative area estimate of $0.1\,\mathrm{mm}^2$ in $28\,\mathrm{nm}$ CMOS for the entire analog front-end (i.e., including the ADC and the clock generator).

V. Simulation Results

A. Nyquist-Rate Simulation Results

The performance of the 4-bit flash ADC has been characterized by means of Cadence Spectre simulations. Tests in uniform sampling mode at $1.5\,\mathrm{GS/s}$ with a $400\,\mathrm{mV_{pp}}$ full-scale sinusoidal input at $f_{\mathrm{in1}} = 2.741\,\mathrm{GHz}$ showed the adequate settling of the sampling circuitry for input signals far above the Nyquist limit. Figure 4(a) shows the corresponding output spectrum with the expected alias of the super-Nyquist input signal at $259\,\mathrm{MHz}$.

The effect of the mismatch-induced offset of the preamplifier input pair has been assessed by means of Monte-Carlo simulations. Specifically, the use of small but fast transistors in the preamplifier results in an input offset with standard-deviation $\sigma(v_{\mathrm{os}}) = 4.6\,\mathrm{mV}$. This offset degrades the ADC performance, but can be compensated partially in the sparse signal recovery algorithm.

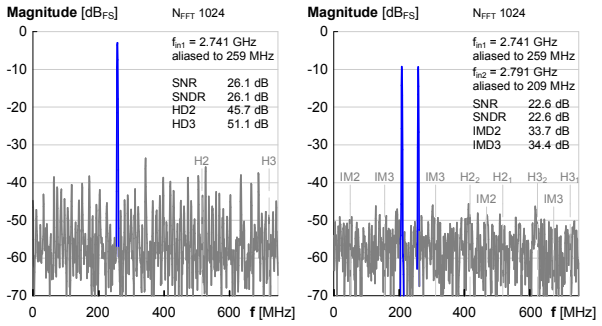
A full-scale two-tone test, shown in Figure 4(b), demonstrates the absence of any third-order intermodulation product (IM3) in the output spectrum once the comparator mismatch has been calibrated. Transistor level simulations reveal the entire analog front-end consumes an estimated power of $5.4\,\mathrm{mW}$ at $1.9\,\mathrm{GS/s}$ from the $1\,\mathrm{V}$ supply, 67% of which is due to the static consumption in the DDPAs.

B. System Simulations with Real-World Data

We next show Matlab simulations, in which we use real-world RF signals acquired by a $2.1\,\mathrm{GHz}$ spectrum analyzer, a $6\,\mathrm{GHz}$ main clock and an undersampling factor of 5.5 in our analog front-end; this corresponds to an average sampling rate of $1.09\,\mathrm{GHz}$. Thus, the average sampling rate is $3.85\times$ below the Nyquist frequency of $4.2\,\mathrm{GHz}$. The acquired input spectrum (the ground truth) is shown in light gray in Figure 5; the result of the BPDQ solver is shown in blue. We see that the dominant frequency peaks are recovered using the proposed approach, while active frequencies with too low a magnitude remain undetected; the detection performance for such weak signals could be improved resorting to more sophisticated sparse spectrum recovery methods, such as the ones detailed in [7].

C. Design Results of the CS-based ADC

The design results are summarized in Table I. The analog front-end is capable of acquiring wideband signals of up to $3.8\,\mathrm{GHz}$ at an average sampling rate as low as $660\,\mathrm{MS/s}$ using sampling frequencies ranging



(a) (b)

Fig. 4. Nyquist-rate output spectra: (a) single-tone test with a $0\,\mathrm{dB_{FS}}$ input signal at $f_{\mathbf{in1}} = 2.741\,\mathrm{GHz}$; (b) two-tone test with two input signals of $-3\,\mathrm{dB_{FS}}$ at $f_{\mathbf{in1}} = 2.741\,\mathrm{GHz}$ and $f_{\mathbf{in2}} = 2.791\,\mathrm{GHz}$.

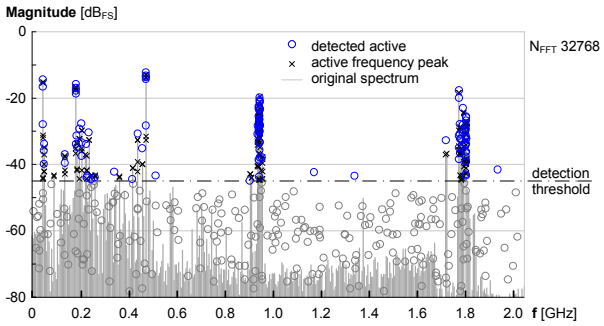


Fig. 5. Recovered real-world RF spectrum using a Matlab model including the analog front-end and the BPDQ solver for spectrum recovery of [1].

TABLE I
IMPLEMENTATION RESULTS IN 28 NM CMOS

Max. uniform sampling rate	[GS/s]	1.9
Non-uniform sampling rates	[GS/s]	0.4–1.9
Undersampling factors		4, 4.5, 5.5, 7.5, 11.5
ADC max. power cons.[a]	[mW]	4.7
ADC idle power cons.[a]	[mW]	3.0
Clock generator power[a]	[mW]	0.65
Energy efficiency	[pJ/S]	2.9
Circuit area[b]	[mm^2]	~ 0.1

[a]Data obtained from transistor-level simulations with Cadence Spectre at maximum uniform clock frequency, $V_{dd} = 1\,\mathrm{V}$, and 300 K.
[b]Conservative estimate.

TABLE II
COMPARISON TO EXISTING CS-BASED ADCS

Publication	[7]	[10]	This Work
Technology	0.45 µm InP	90 nm CMOS	28 nm CMOS
S&H	custom	custom	custom
ADC	off-chip	10-bit 9.5 MS/s	4-bit 1.9 GS/s
Clock gen.	off-chip	off-chip	on-chip
Bandwidth	2.4 GHz	100 MHz	3.8 GHz
Power	5.8 W	550 µW	5.4 mW

from 0.4 GS/s to 1.9 GS/s maximum. The non-uniform pseudo-random clock generator is capable of running at a maximum clock frequency of 7.8 GHz, but is operated at 7.6 GHz due to the maximum speed limitation of the ADC. We emphasize that the clock generator allows us to configure the undersampling factor up to 11.5, which renders the analog front-end power efficient in comparison to conventional Nyquist rate ADCs with the same reconstruction bandwidth. The effective recoverable spectral bandwidth is 3.8 GHz and is—in the present design—limited by the maximum speed of the ADC.

VI. CONCLUSIONS

We have developed a new compressive sensing (CS)-based signal acquisition front-end for wideband spectrum sensing. The proposed design is implemented in 28 nm CMOS and includes a 1.9 GS/s signal acquisition stage built from a 4-bit flash ADC that samples the time-domain signals at sub-Nyquist rates using a non-uniform sampling clock generated directly on-chip. The non-uniform sampling-based CS scheme effectively extends the conversion bandwidth of the ADC by a factor of 4 and enables us to acquire spectrally sparse signals up to 3.8 GHz at undersampling factors of up to 11.5. Circuit simulations with synthetic and real-world data have shown that the proposed design enables the accurate detection of sparse spectral activity information at low power and low implementation cost.

We would like to emphasize that the design proposed in this paper avoids the need for external pseudo-random clock generation and is capable of acquiring higher bandwidths compared to that of existing designs at more than three orders of magnitude lower power consumption. See Table II for a detailed comparison of our design with existing CS-based ADCs for wideband spectrum sensing.

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